Module – 4 CMOS Circuit and Logic Design

INTRODUCTION, CMOS LOGIC STRUCTURES, CMOS COMPLEMENTARY LOGIC, PSEUDO N-MOS LOGIC, DYNAMIC CMOS LOGIC, CLOCKED CMOS LOGIC, CASCADE VOLTAGE SWITCH LOGIC, PASS TRANSISTOR LOGIC, ELECTRICAL AND PHYSICAL DESIGN OF LOGIC GATES, THE INVERTER, NAND AND NOR GATES, BODY EFFECT, PHYSICAL LAYOUT OF LOGIC GATES, INPUT OUTPUT PADS.

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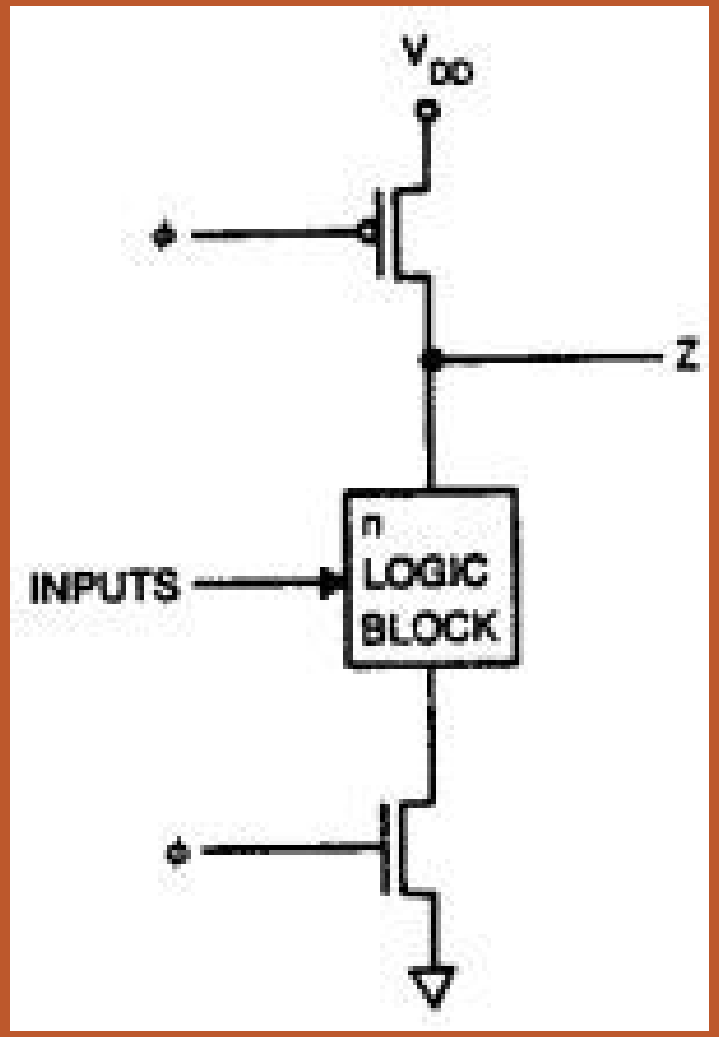
CMOS Logic structures

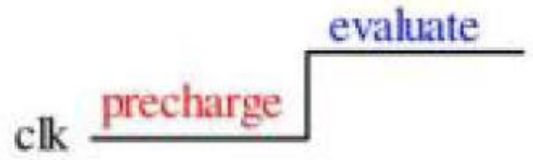
- CMOS Complementary Logic
- Pseudo-nMOS Logic
- Dynamic CMOS Logic
- Clocked CMOS Logic (C2MOS)
- CMOS Domino Logic
- Cascade Voltage Switch Logic (CVSL)
- Pass Transistor Logic

Dynamic CMOS Logic



Simple single phase dynamic CMOS:

- Precharge phase : Clk (ϕ) = 0
- Evaluate Phase : Clk (ϕ) = 1



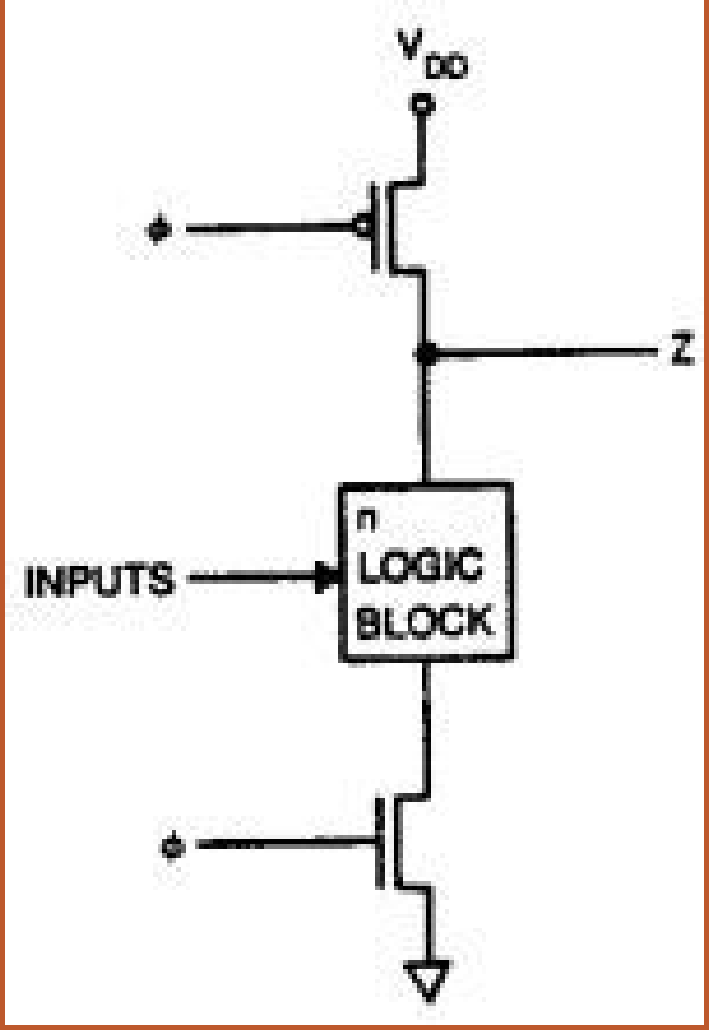
Input Capacitance : only one gate unit

Problem:

- Inputs can only change during the precharge phase.
- If they change during evaluate, charge redistribution can corrupt output voltage.

- Pull-up time improved by virtue of the active switch (p-transistor
- can be much larger).
- Pull-down time increased due to the ground switch.

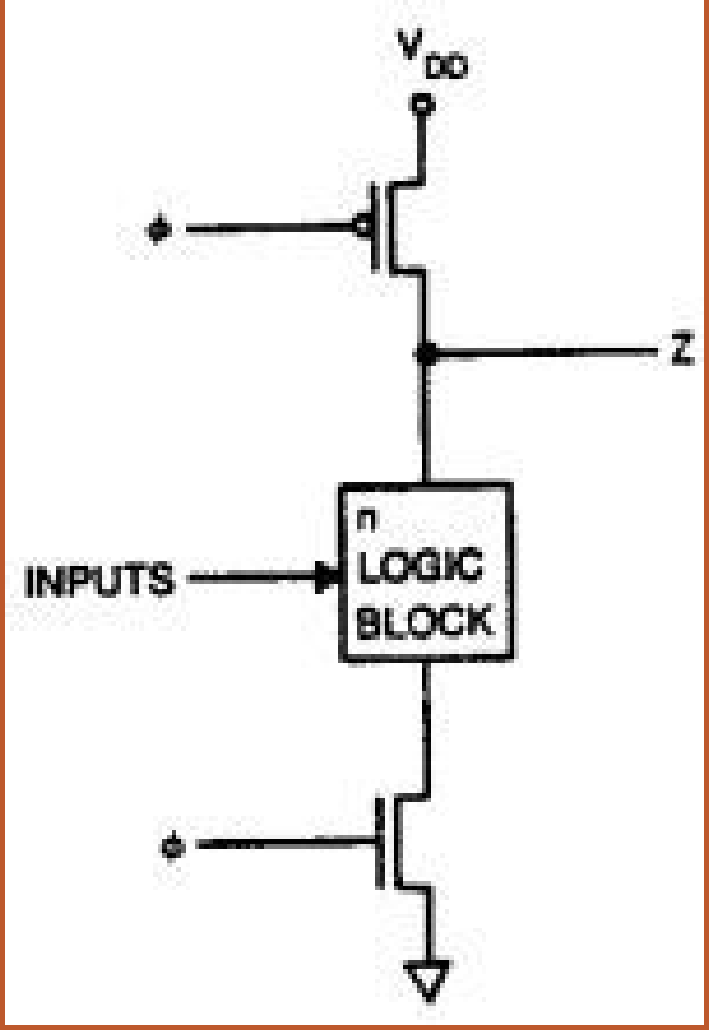
Dynamic CMOS Logic



Basic Concept

- Dynamic CMOS gate uses:
  - **n-transistor logic structure**.
  - **Precharge** to V_{DD} using a p-transistor.
  - **Conditional discharge** to V_{SS} using an n-transistor.
- Single phase clock (φ) controls the logic:
  - **φ = 0**: Precharge phase – output node charged to V_{DD}.
  - **φ = 1**: Evaluate phase – output may discharge based on input.

Dynamic CMOS Logic



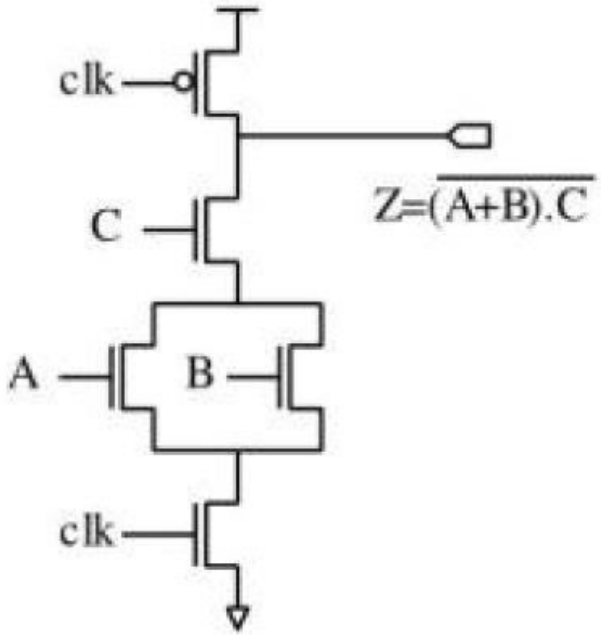
Operation Details

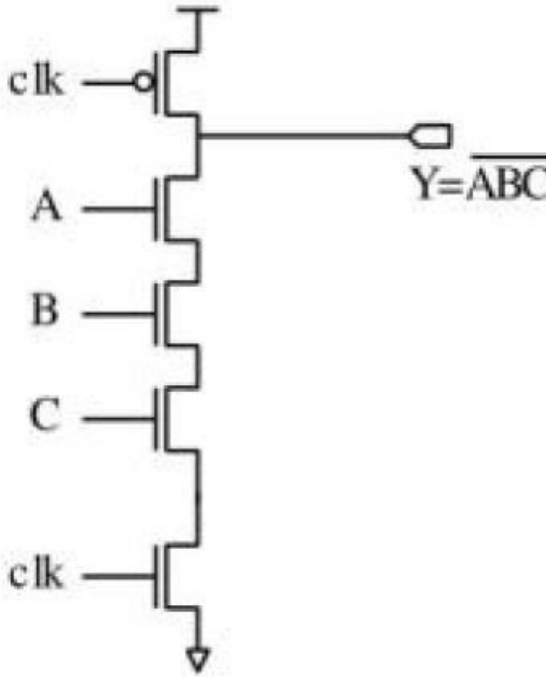
- The output load is charged during the **precharge** phase.
- During **evaluation**, the output may discharge based on inputs.
- The **input capacitance** is same as pseudo-nMOS logic.
- Pull-up time is longer due to the use of a **ground switch**.

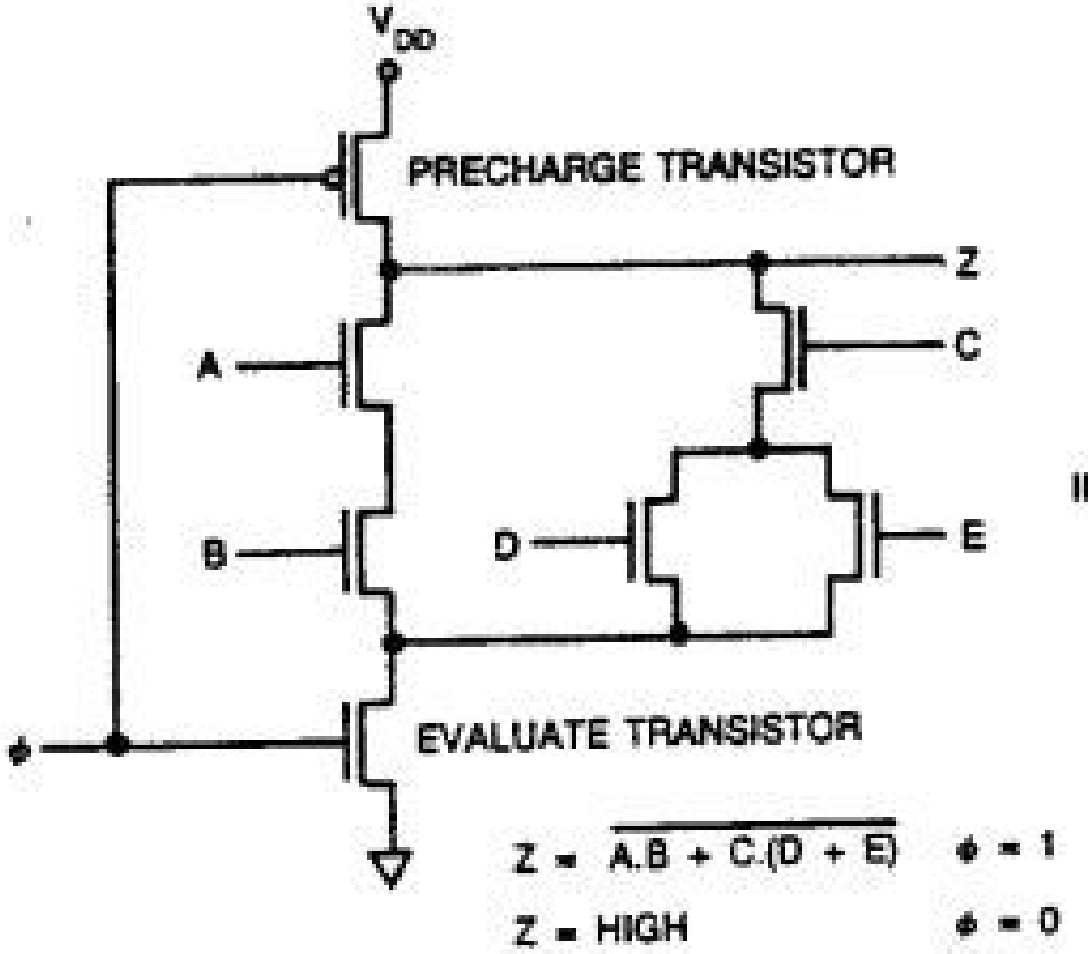
Challenges

1. **Inputs must switch before evaluation**, else:
    1. Charge sharing may corrupt output.
2. **Cascading is difficult**:
    1. Output of one gate may affect the next before full evaluation.
3. **Clocking constraints**:
    1. Fast gates must wait for slowest gates.
    2. Leads to clock synchronization challenges.

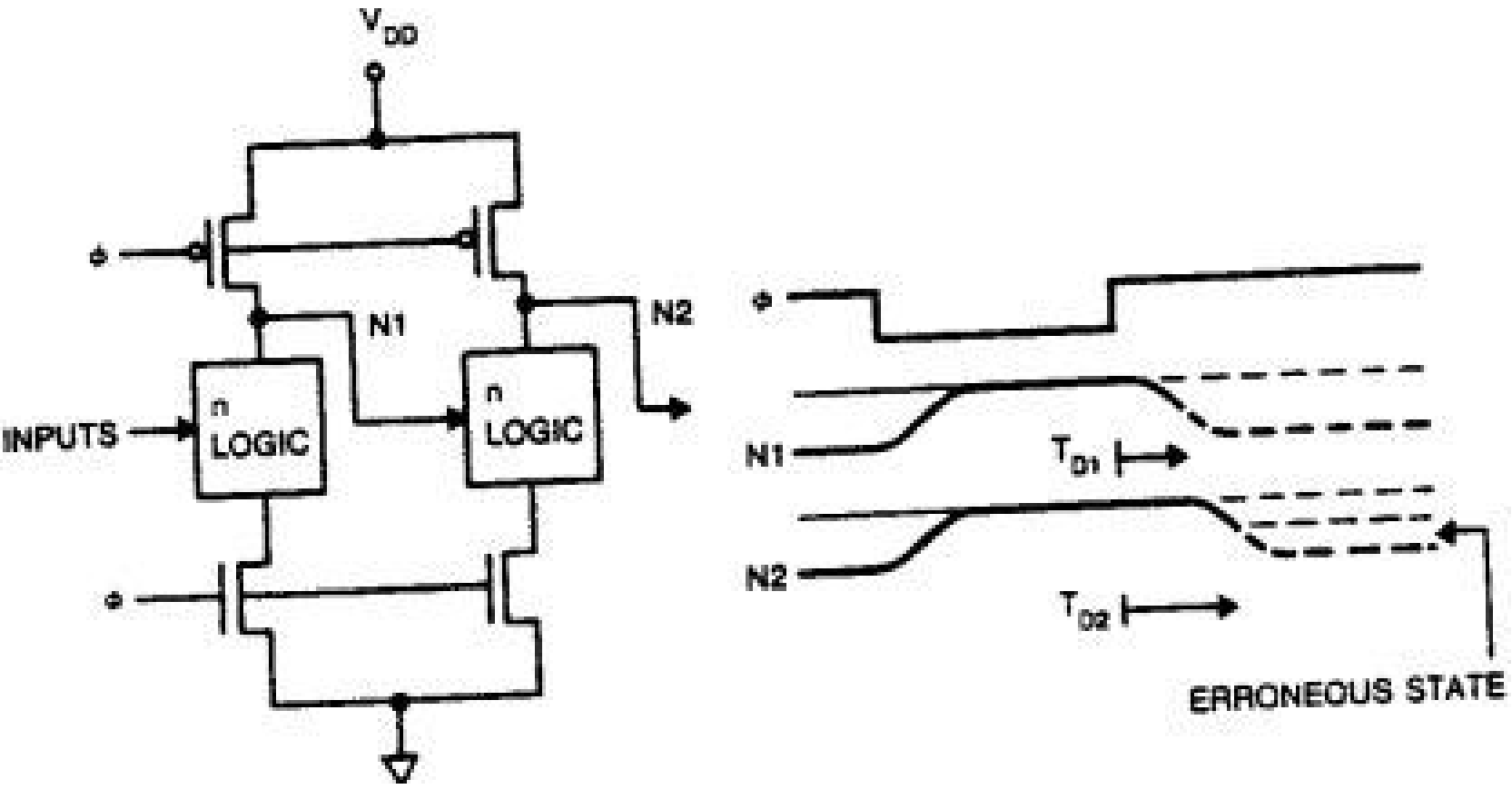
Example


clk
C
A
B
clk
Z=(A+B).C

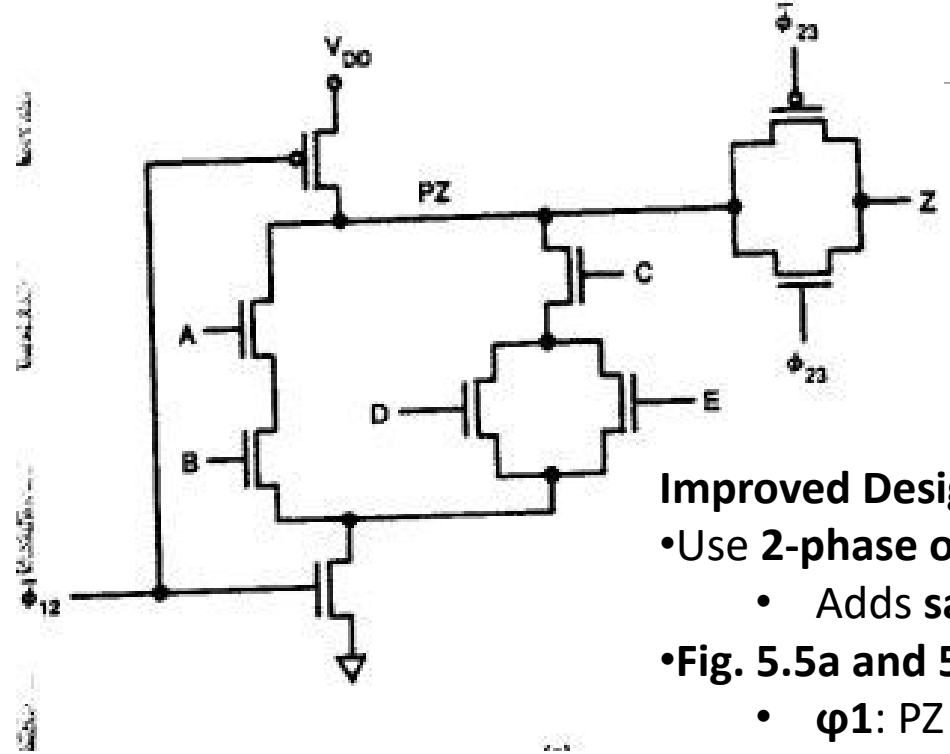

clk
A
B
C
clk
Y=ABC

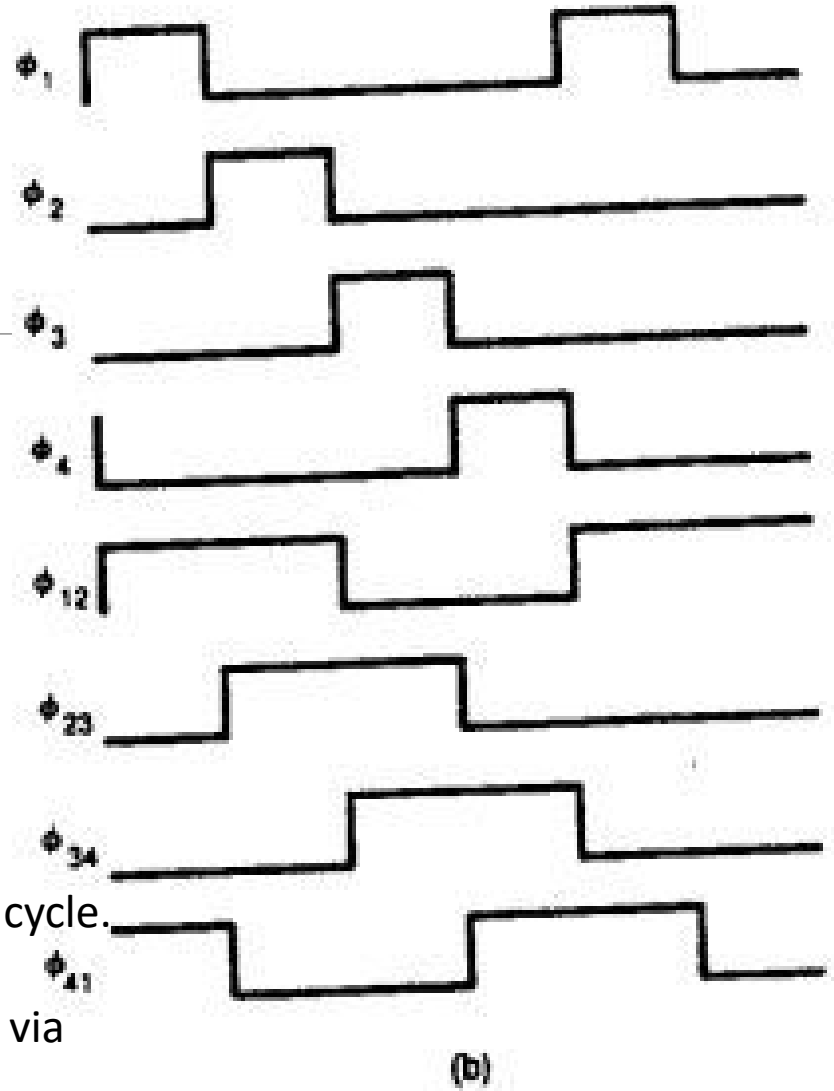

V DD
PRECHARGE TRANSISTOR
Z
C
A
B
D
E
EVALUATE TRANSISTOR
Z = A.B + C.(D + E)
Z = HIGH
= 1
= 0

Cascaded dynamic logic



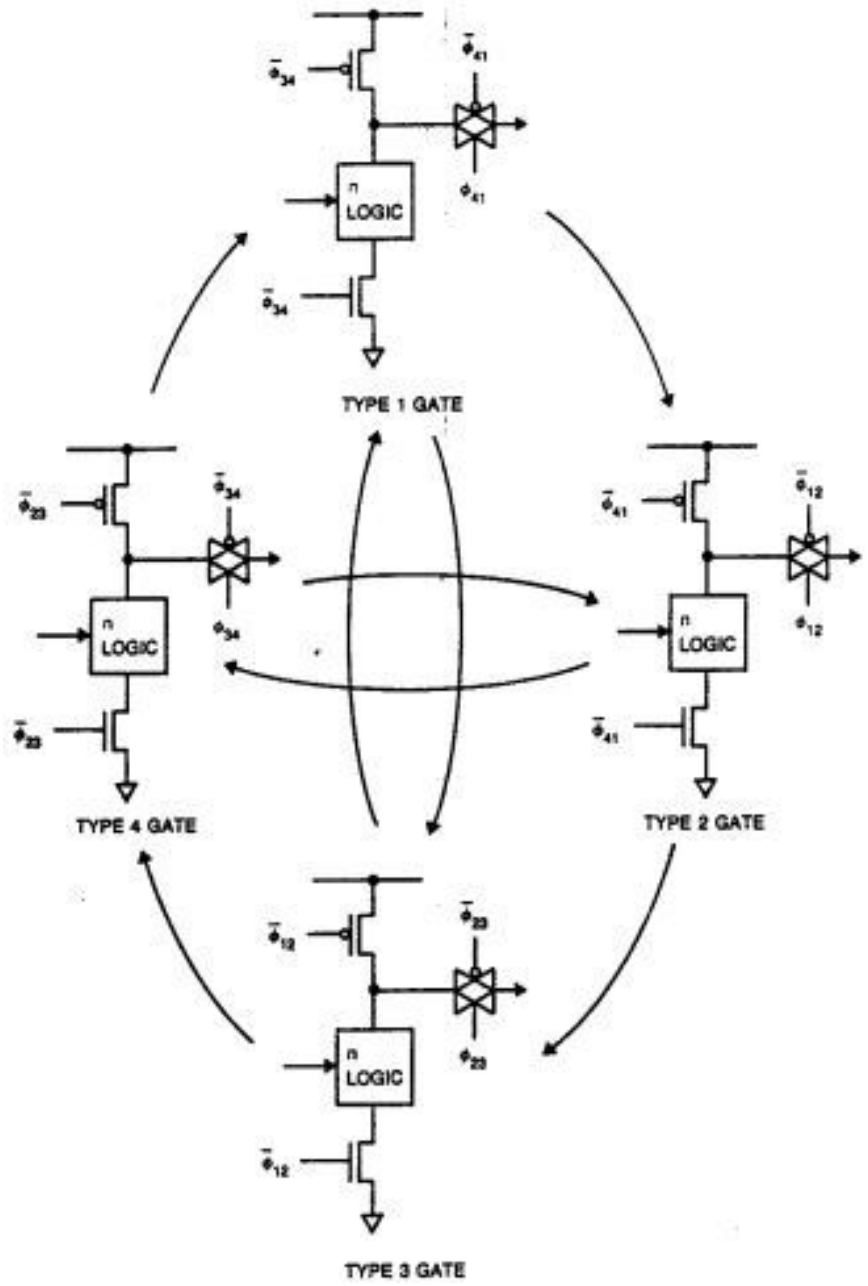
4-phase logic – type A





Improved Designs

- Use **2-phase or 4-phase** clocking:
  - Adds **sample and hold** phase.
- **Fig. 5.5a and 5.5b**: Gate precharge and evaluate cycle.
  - **φ1**: PZ precharged, Z held.
  - **φ2**: PZ remains precharged; Z precharges via transmission gate.
  - **φ3**: Gate evaluates; PZ discharges conditionally.
  - **φ4**: Z held in evaluated state.



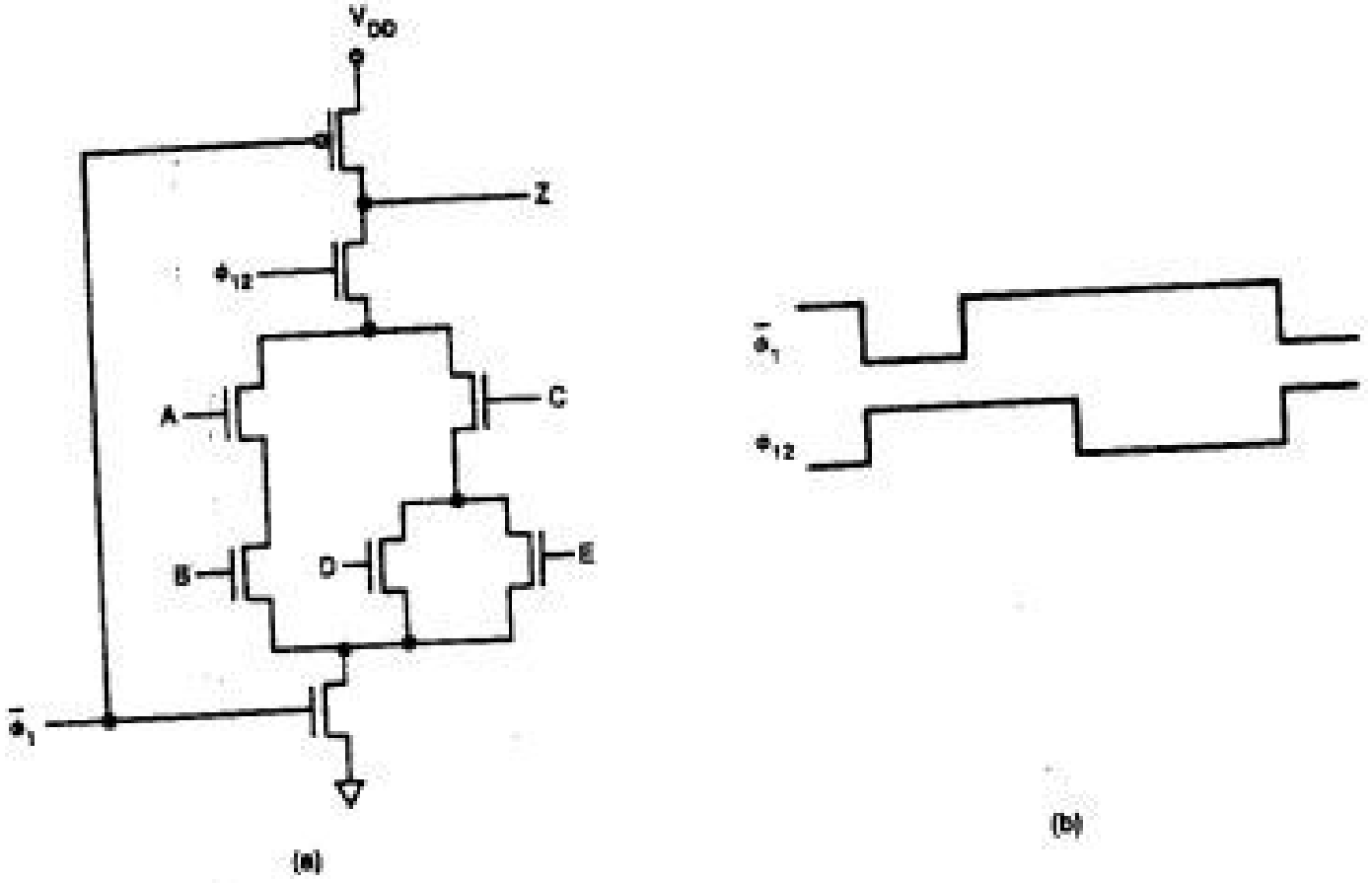
Logic Gate Typing

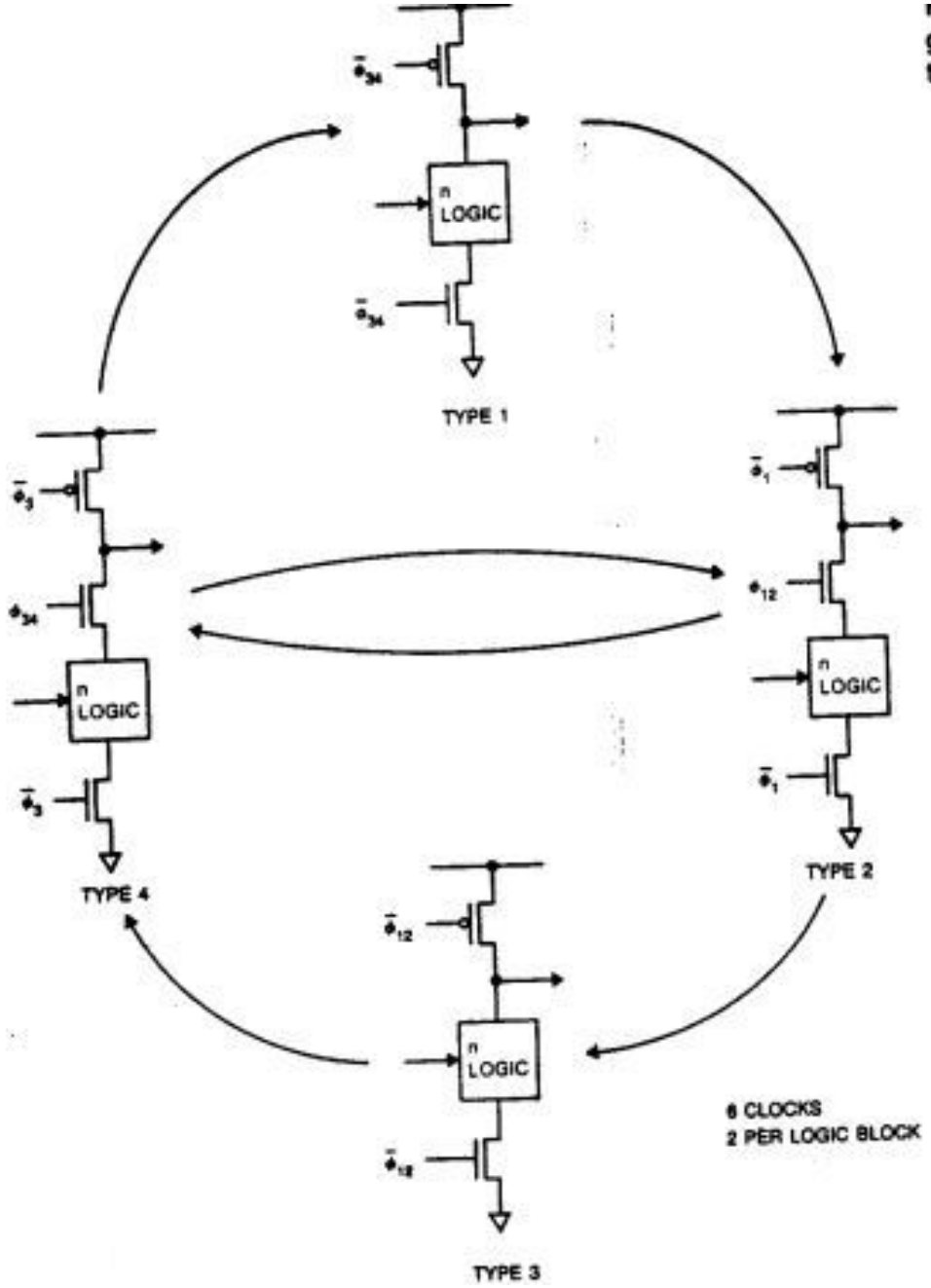
- Four types of gates exist based on evaluation phase.
- Must be sequenced correctly for reliable operation.

Clocking Schemes

- Alternate **4-phase system**
  - Simpler layout, fewer clocks.
  - Restrictions on gate interconnects
- **2-phase system**:
  - Uses gate types 2 and 4.
  - More compact but restrictive.

4 – phase logic – type B

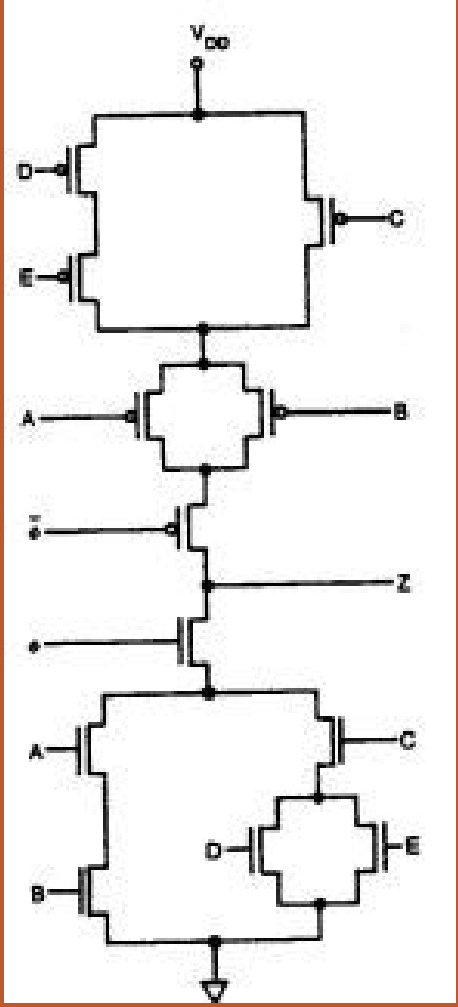




Transistor Count & Performance

- For n-input gate:
  - Transistors needed = **n + 4** or **n + 3**.
- **Clock frequency** must suit slowest gate:
  - Fast gates waste time waiting ("dead time").
- Distributing 4+ clocks is a challenge on large chips.

Clocked CMOS Logic



Clocked CMOS Logic (C^2MOS)

- **Purpose:** C^2MOS logic was originally designed to achieve low power dissipation in CMOS circuits.
- **Usage:** It's often used to construct latches or interface with other dynamic structures that incorporate latches.
- **Characteristics:**
  - It has the same input forms of logic as regular complementary gates.
  - It has larger rise and fall times compared to regular CMOS gates due to the series clocking transistors.
  - The gates have the same input capacitance as regular complementary gates.
- **Power Dissipation:** The reduced dynamic power dissipation is a key advantage. The text mentions this stems from metal gate CMOS layout considerations.

C^2MOS is a type of CMOS logic that prioritizes low power consumption, often used in circuits with latches. However, it comes with a tradeoff of slower switching speeds (larger rise and fall times) compared to standard CMOS logic.

CMOS Domino Logic

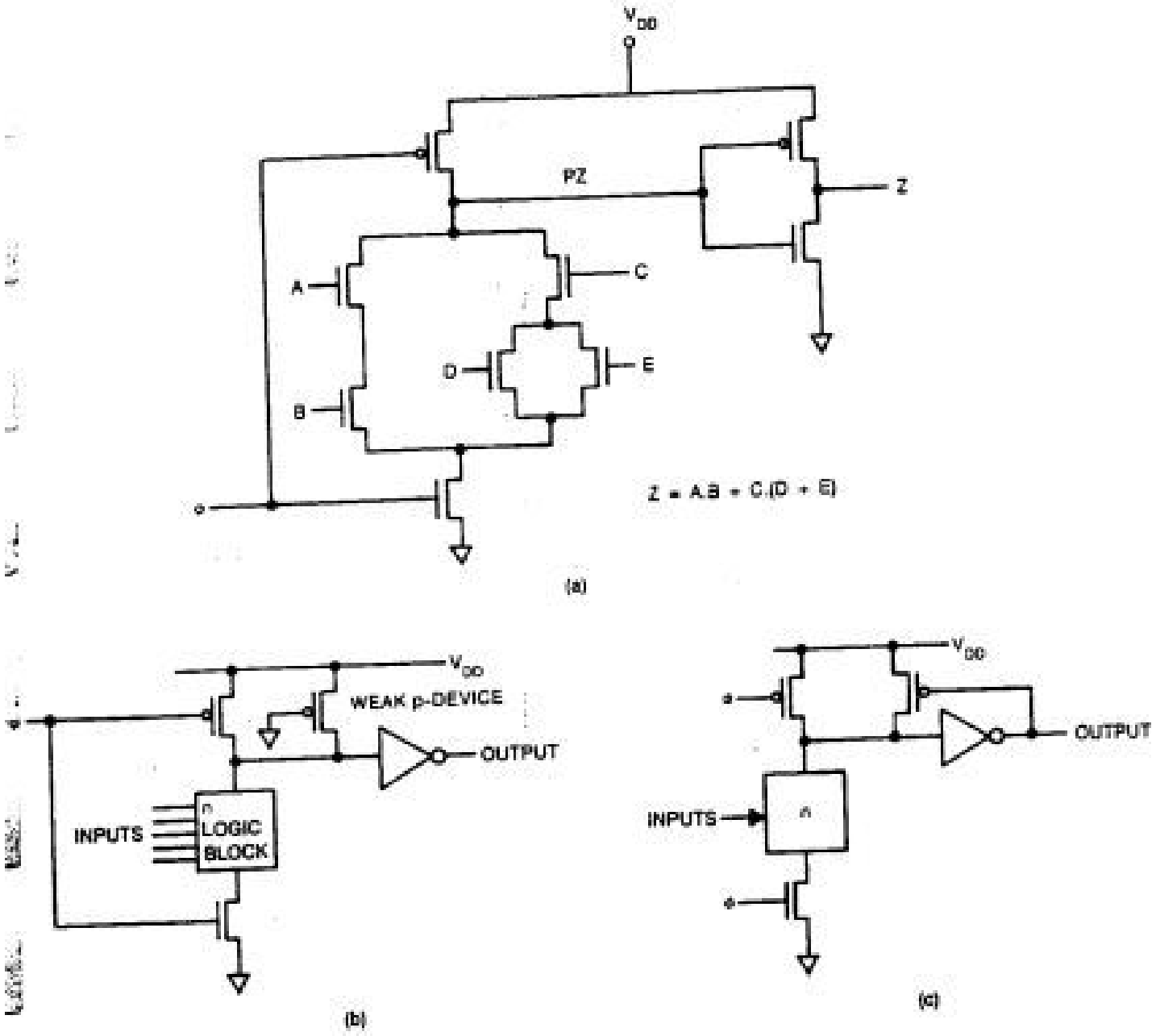


FIGURE 5.10. CMOS domino logic (a) basic gate, (b) static version (low frequency), and (c) latching version

CMOS Domino Logic

•**Modification:** Domino logic is a modification of clocked CMOS logic.

•**Operation:** It allows a single clock to precharge and evaluate a cascaded set of dynamic logic blocks. This involves a static CMOS buffer in each logic gate.

•**Precharge Phase (Clock = 0):**

- The output node of the dynamic gate is precharged high.
- The output of the buffer is low.

•Transistors in subsequent logic blocks are turned off. **Evaluation Phase (Clock = 1):**

- The gate conditionally discharges, causing the output of the buffer to conditionally go high.
- Each gate in the sequence can make at most one transition (1 -> 0).
- The buffer can only make a transition from (0 -> 1).

•**Cascading:** Each state evaluates and causes the next state to evaluate, similar to a stack of dominoes falling. Any number of logic stages may be cascaded. The sequence can evaluate within the evaluation clock phase.

•**Limitations:**

- Only non-inverting structures are possible.
- Each gate must be buffered.
- Charge redistribution can be a problem (similar to clocked-CMOS).

•**Static Domino Logic:** A weak p-transistor can be included to make the domino gate static. This helps balance the effects of leakage and stabilize the output when the clock is held high. However, it can slow down the pull-up time.

•**Advantages:**

- A single clock can precharge and evaluate all logic gates within a block.

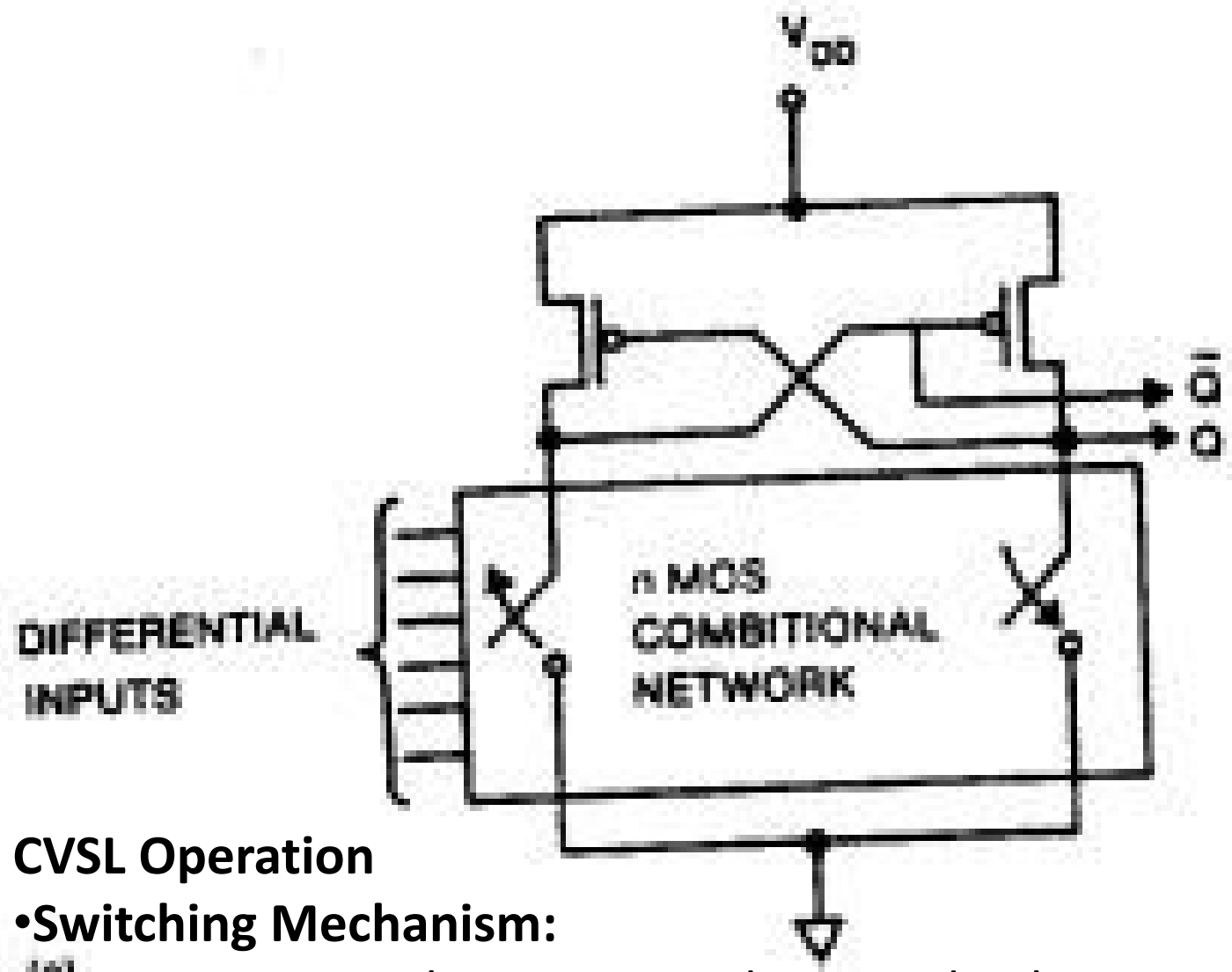
•**Disadvantages:**

- Complex logic circuits (e.g., arithmetic logic units) requiring XOR gates may be implemented conventionally (as complementary gates) due to the limitations of domino logic.

Domino logic uses a precharge and evaluation scheme with buffers to create a fast, cascaded logic structure. It's efficient for certain types of logic but has limitations regarding inverting structures and complexity. The static version addresses some leakage issues at the cost of speed.

Cascade Voltage Switch Logic (CVSL)

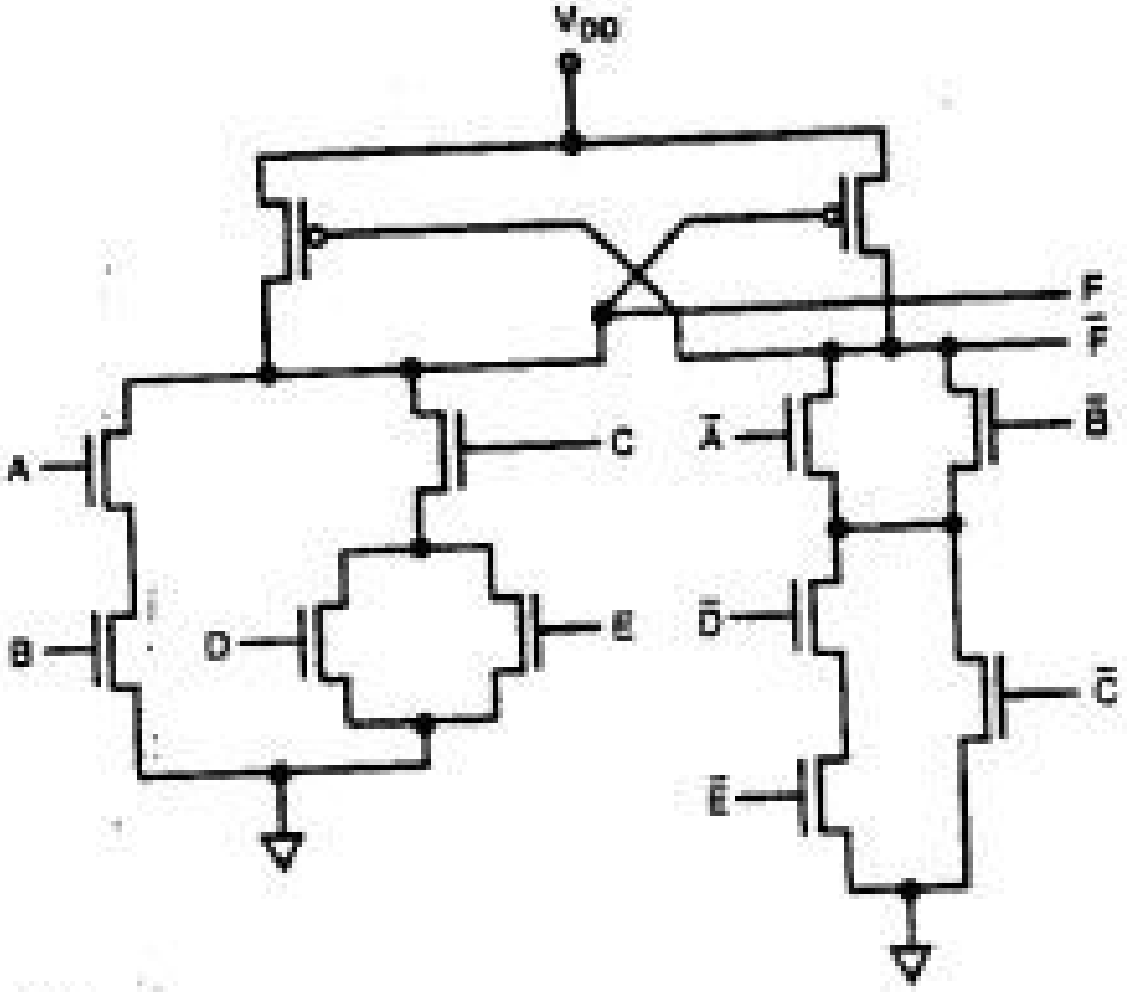
- **What is CVSL?**
- A differential CMOS logic style.
- Requires both true and complement input signals.
- **Key Components:**
- Complementary nMOS switch structures.
- Cross-coupled p pull-up transistors.



CVSL Operation

- **Switching Mechanism:**
  - Inputs switch, causing nodes Q and Q-bar to be pulled high or low.
  - Positive feedback from p pull-ups accelerates the switching.

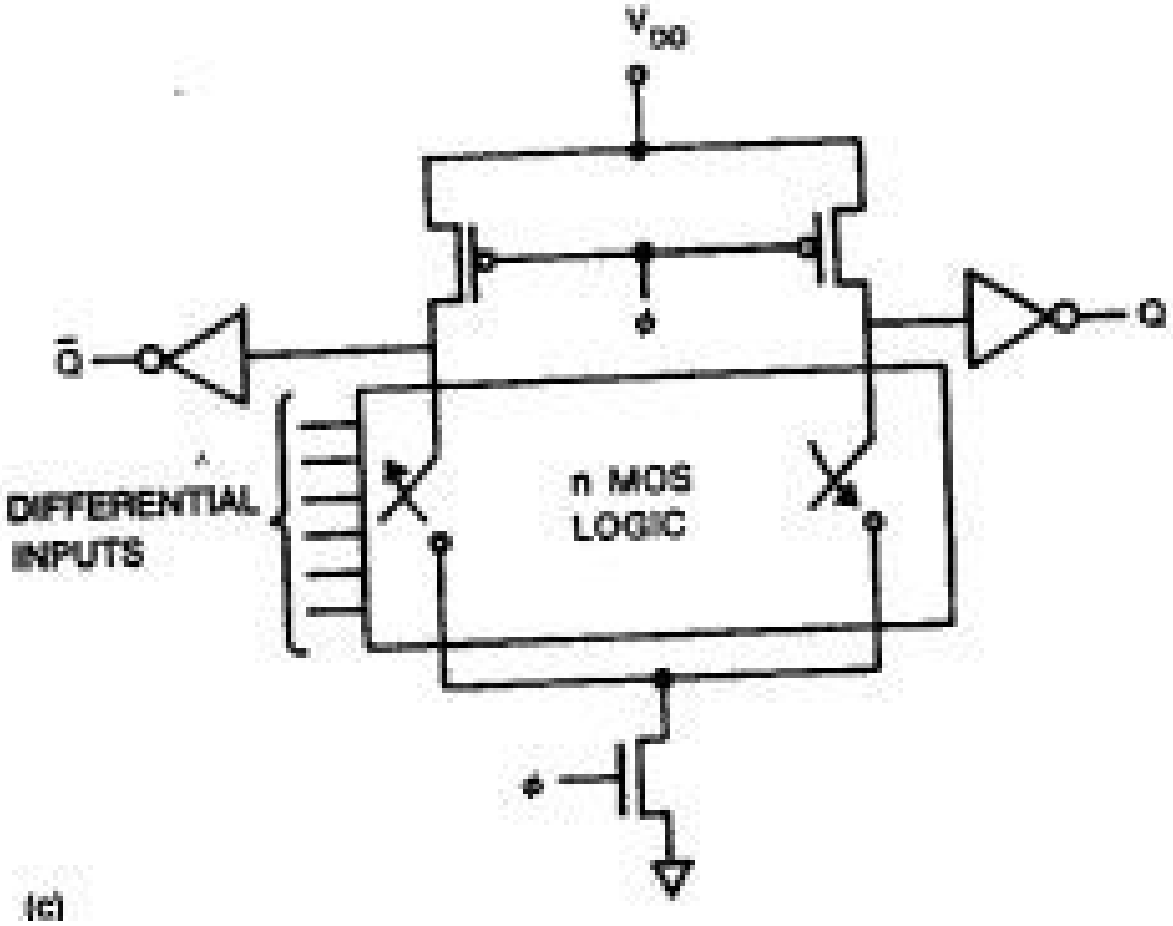
Examples of Static Version



Static CVSL (A "Slower" Version)

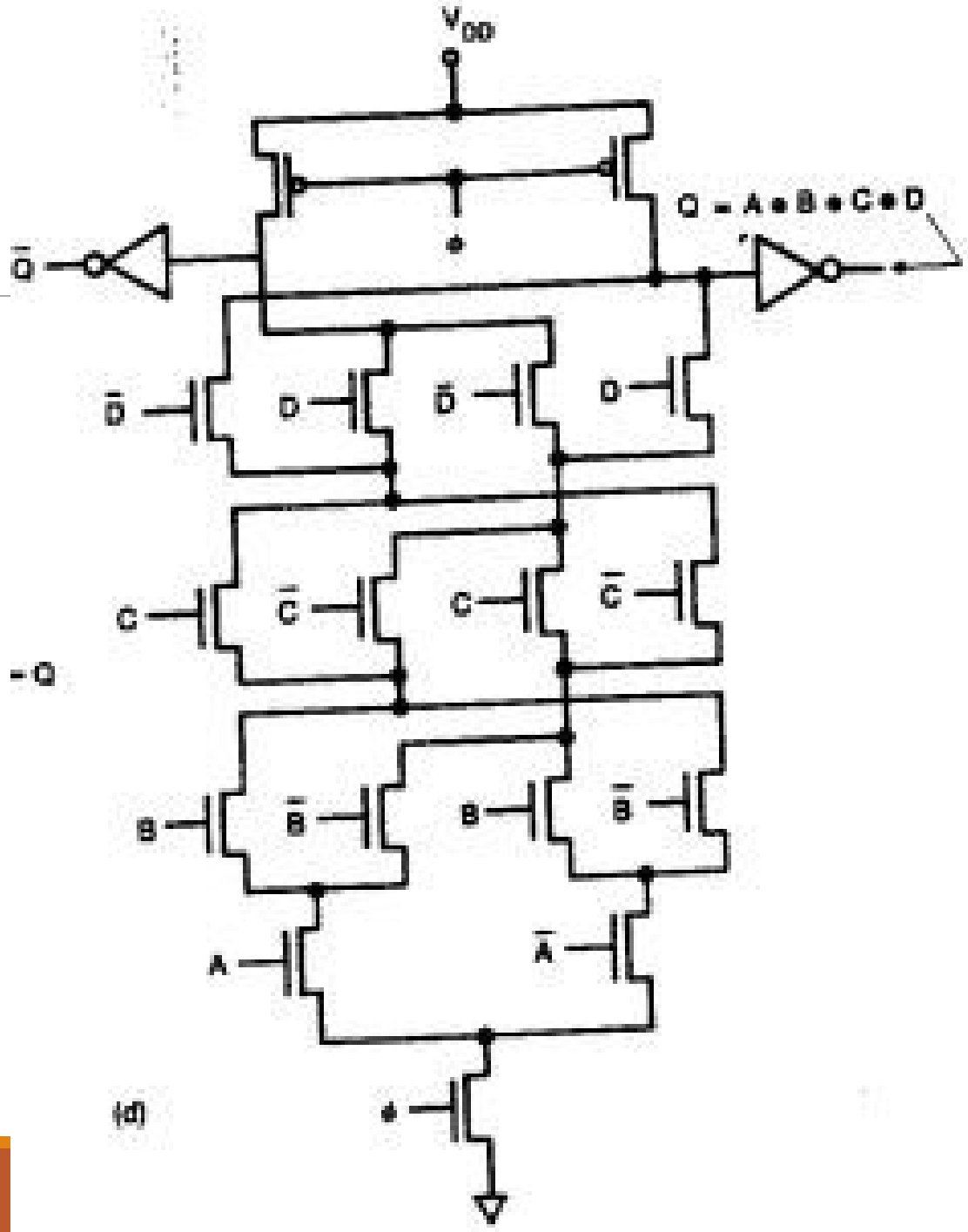
- **Description:** A "static" implementation of CVSL.
- **Disadvantage:** Slower than conventional CMOS gates.
- **Reason:** p pull-ups "fight" the n pull-down trees during switching.

Clocked / Dynamic CVSL (Improved Version)



- **Description:** Essentially two domino gates operating on true and complement inputs.
- **Logic Tree:** Uses a minimized logic tree.

4input Xor CVSL logic

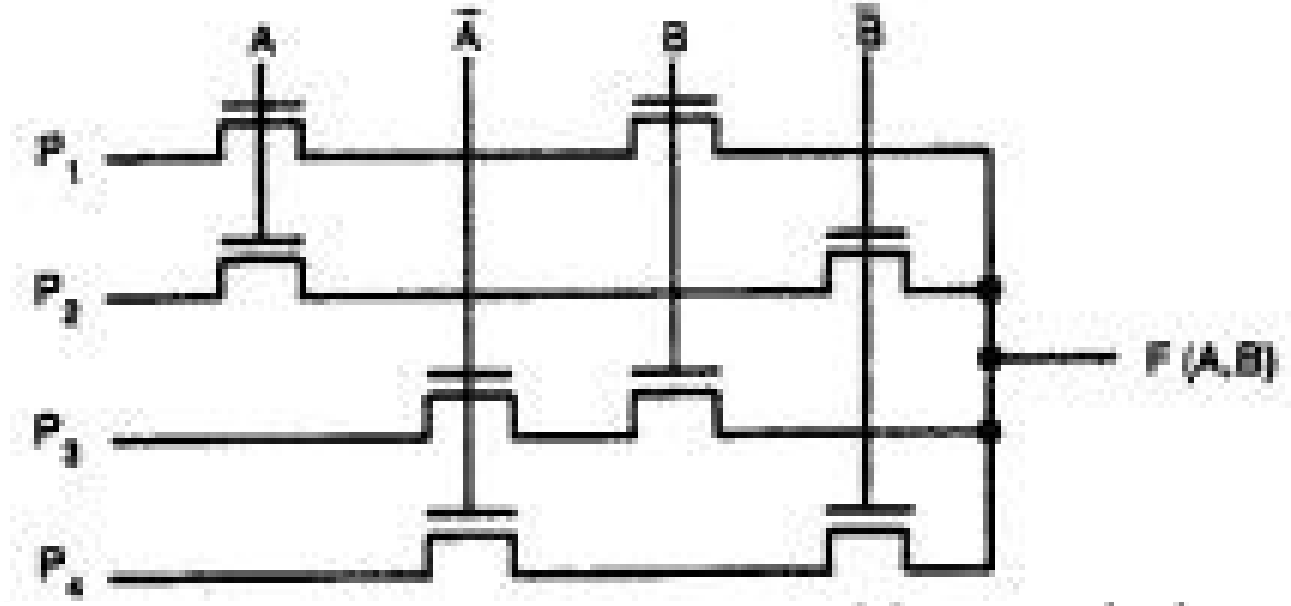


Advantages of Clocked CVSL / Applications

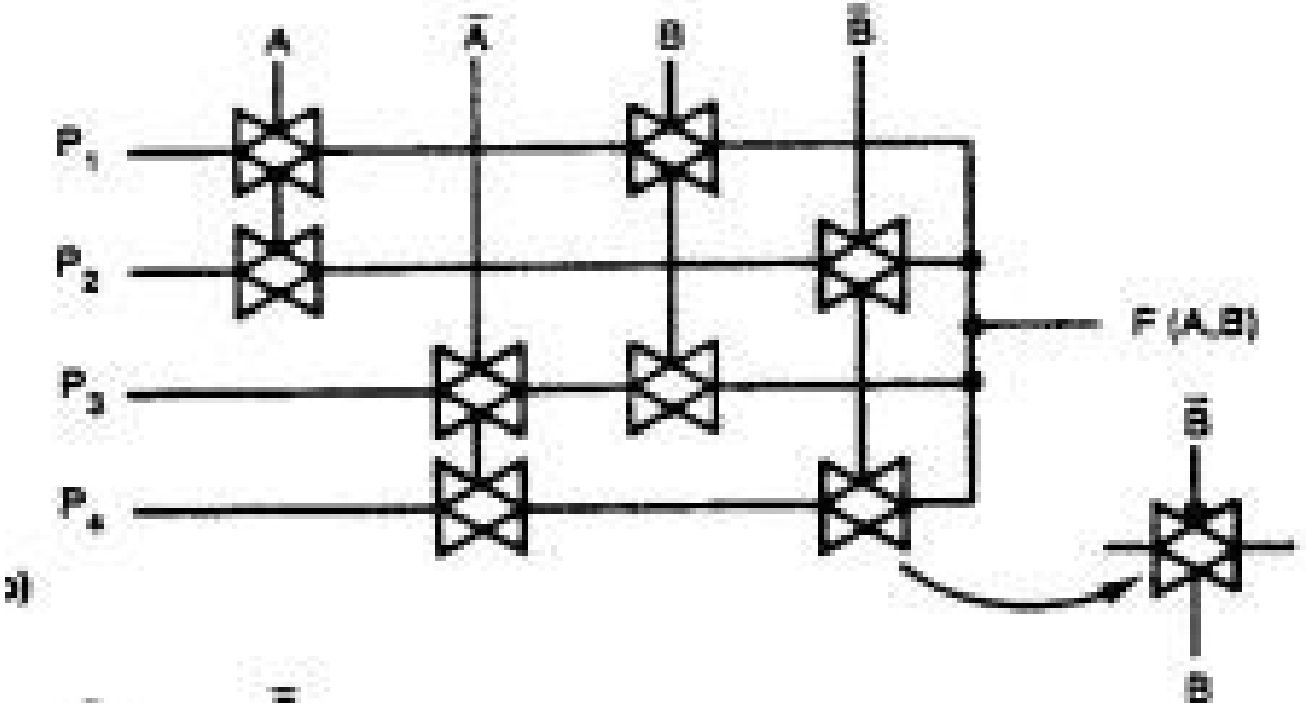
- **Over Domino Logic:**
  - Ability to generate any logic expression.
  - Makes it a complete logic family.
- **Trade-offs:**
  - Extra routing.
  - Increased active area.
  - Greater complexity (due to double-rail logic).

- **Automated Logic Synthesis:**
  - Ability to generate any logic function is advantageous.
- **Example:**
  - Four-way XOR gate implementation.

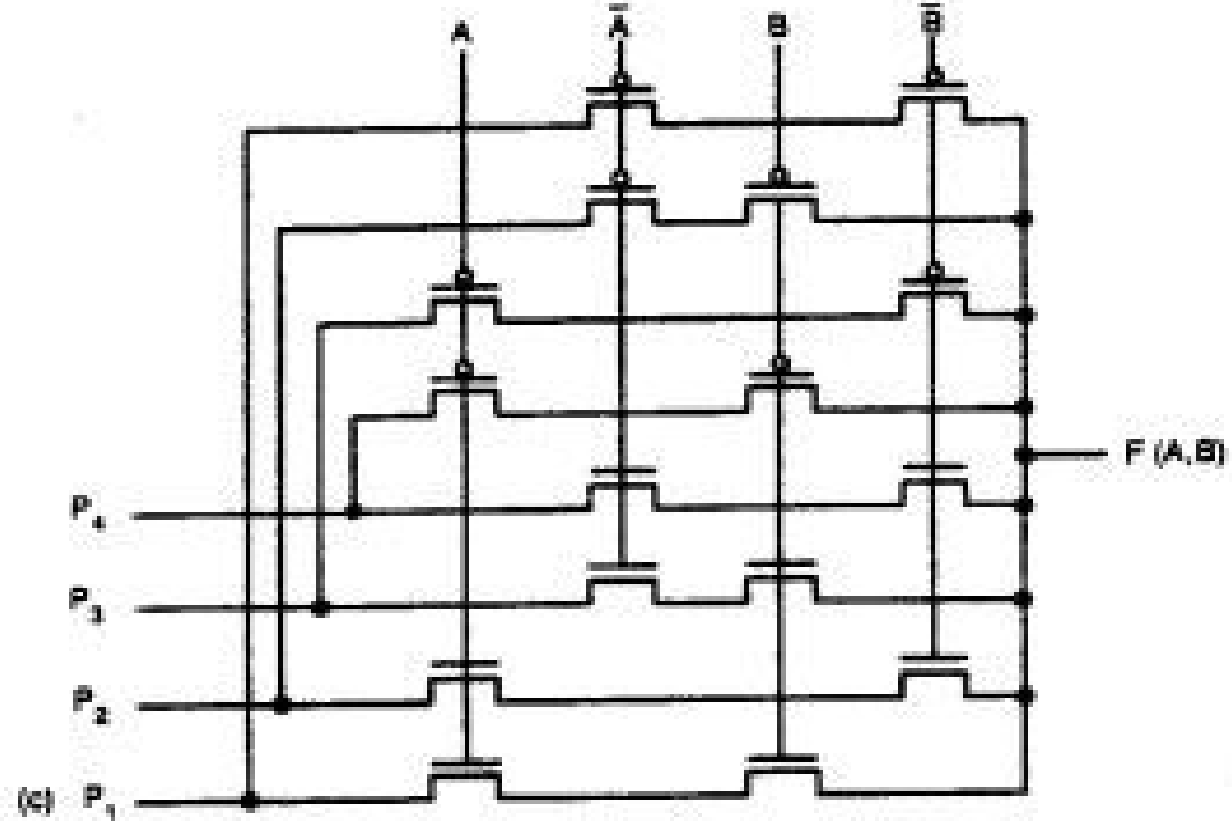
Pass Transistor Logic

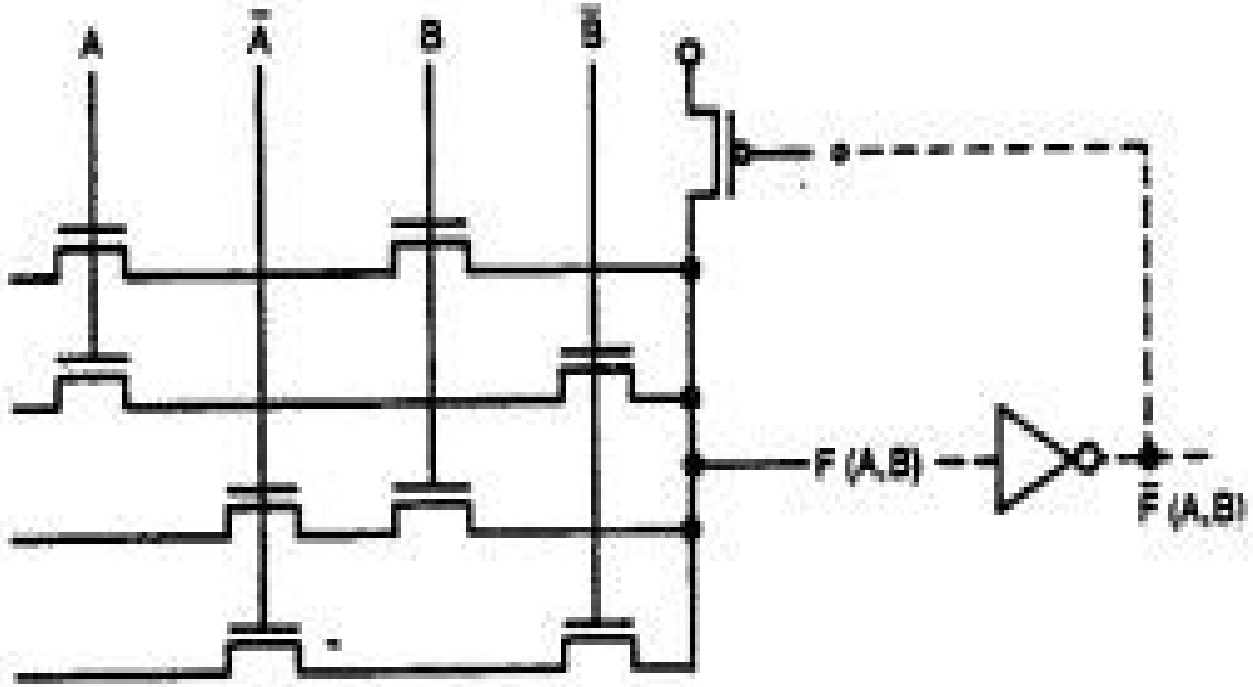


Pass logic function unit (a) nMOS, (b) full CMOS transmission gates, (

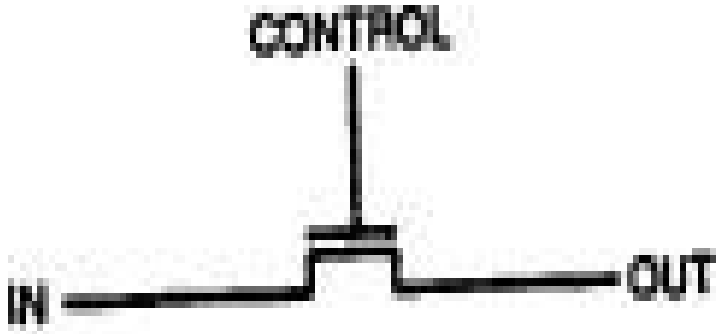


Modified CMOS for Better Layout

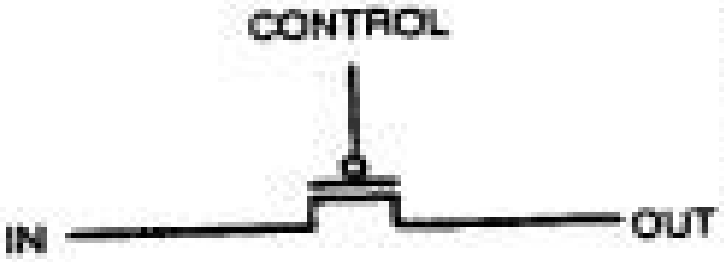




P-Pull Version



IN	CONTROL	OUT
0	0	X
1	0	X
0	1	0
1	1	1



IN	CONTROL	OUT
0	0	0
1	0	1
0	1	x
1	1	x

FIGURE 5.14. Pass transistor logic model. Re-

TABLE 5.1. XOR truth table

A	B	A ⊕ B	PASS FUNCTION
0	0	0	$A + B$
0	1	1	$\overline{A} + B$
1	0	1	$A + \overline{B}$
1	1	0	$\overline{A} + \overline{B}$

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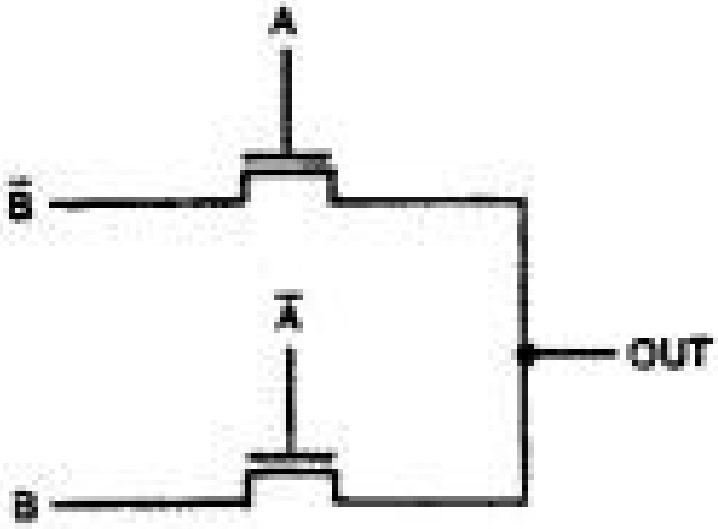
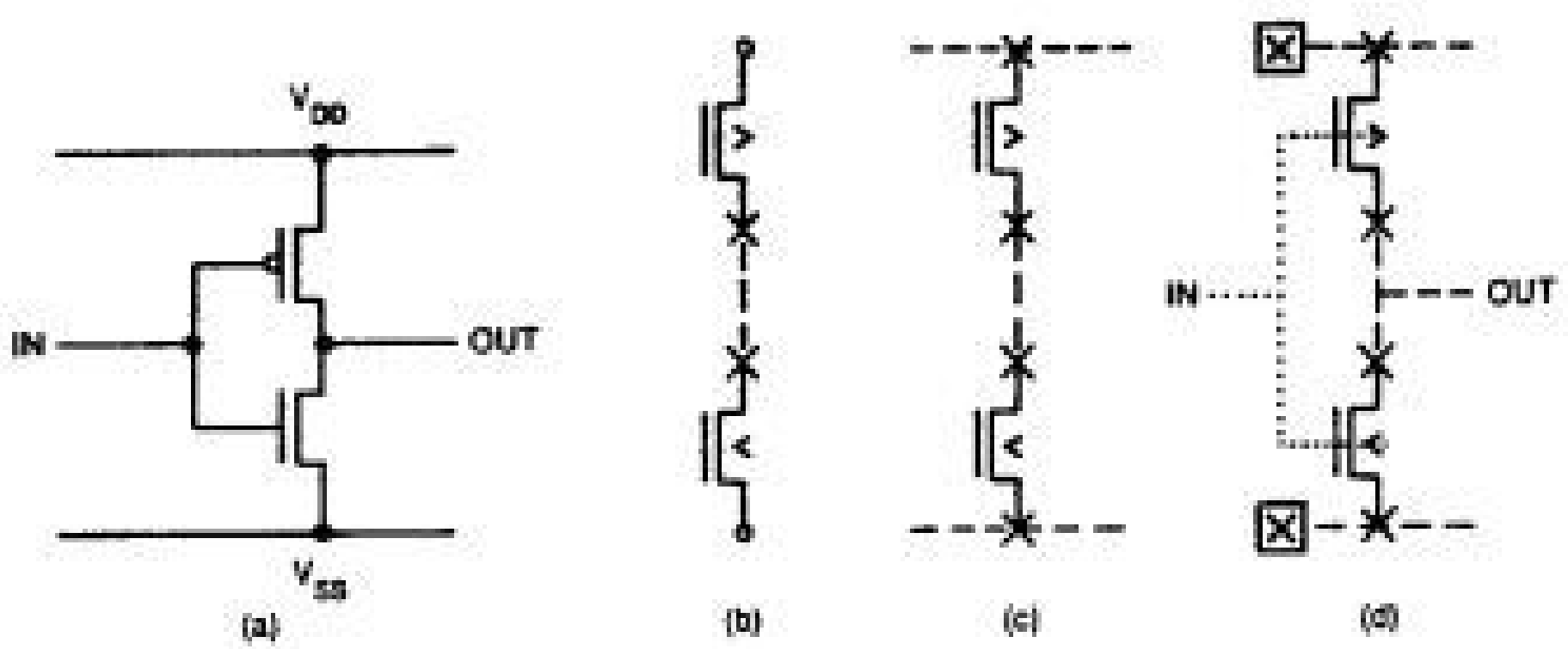
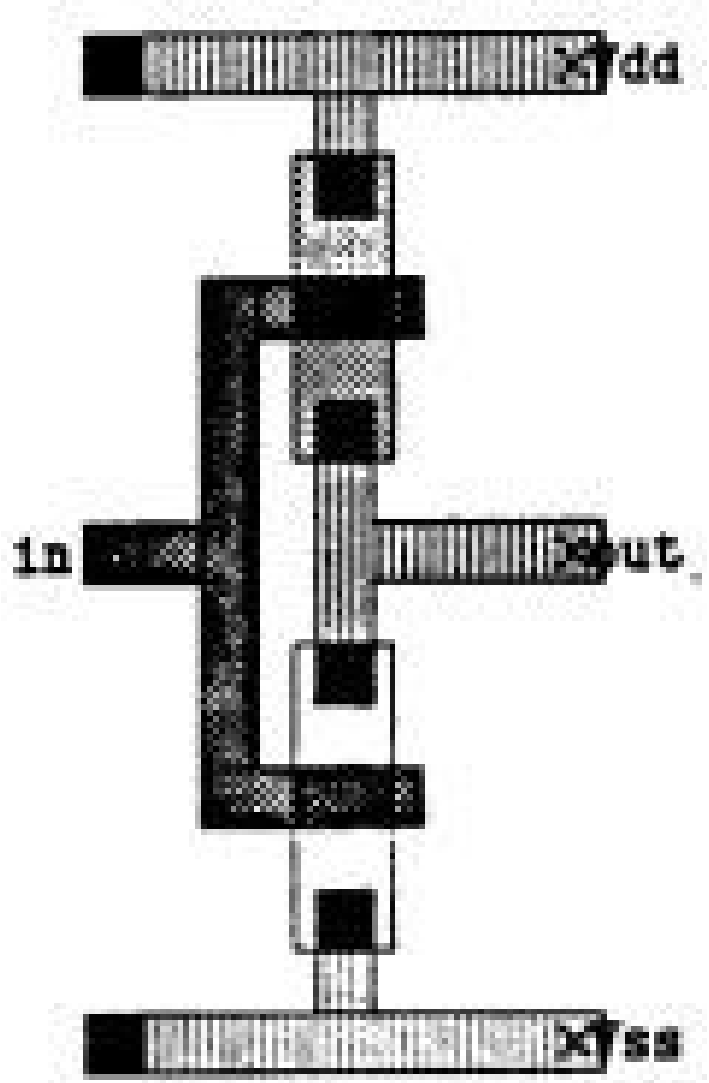


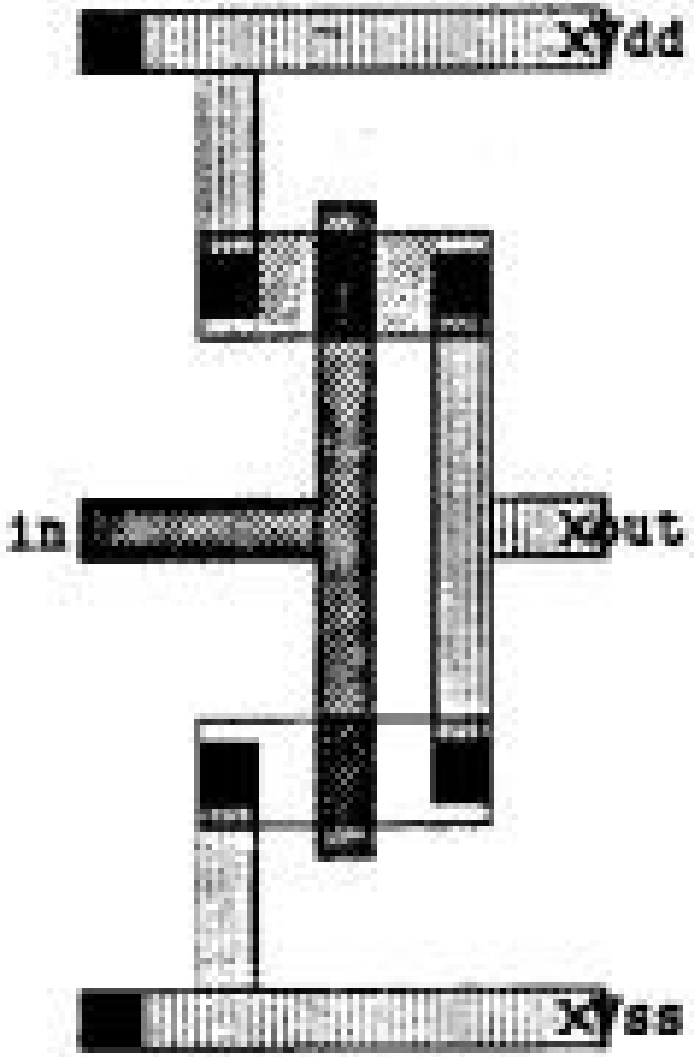
FIGURE 5.15. Pass transistor structure for XOR function. Reprinted from

Electrical and Physical Design of Logic Gates

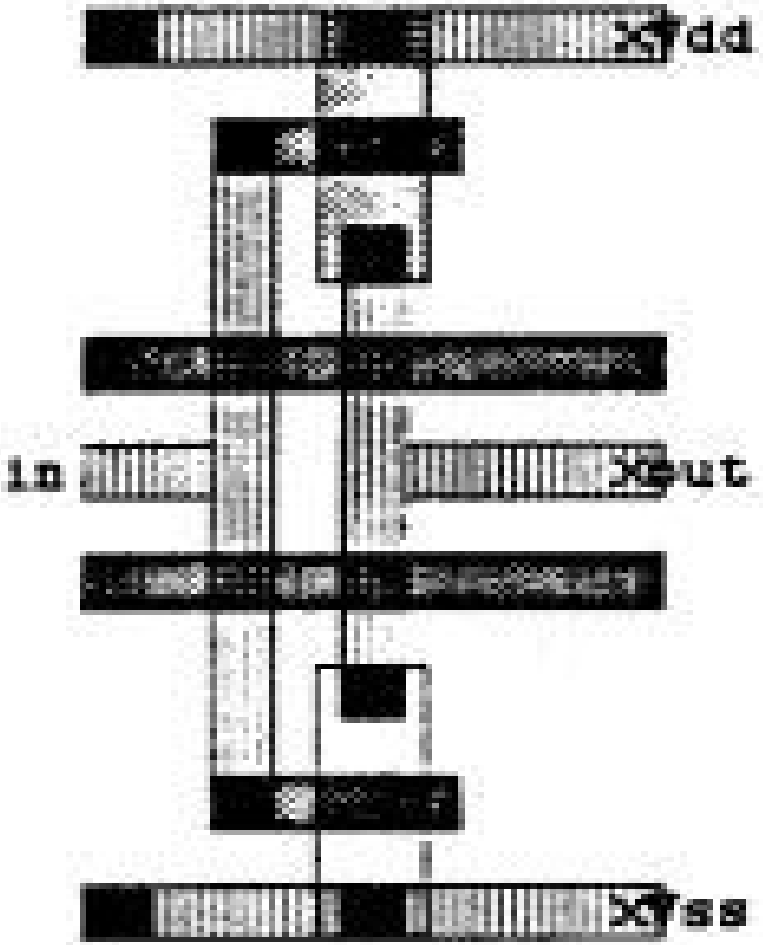
- Inverter





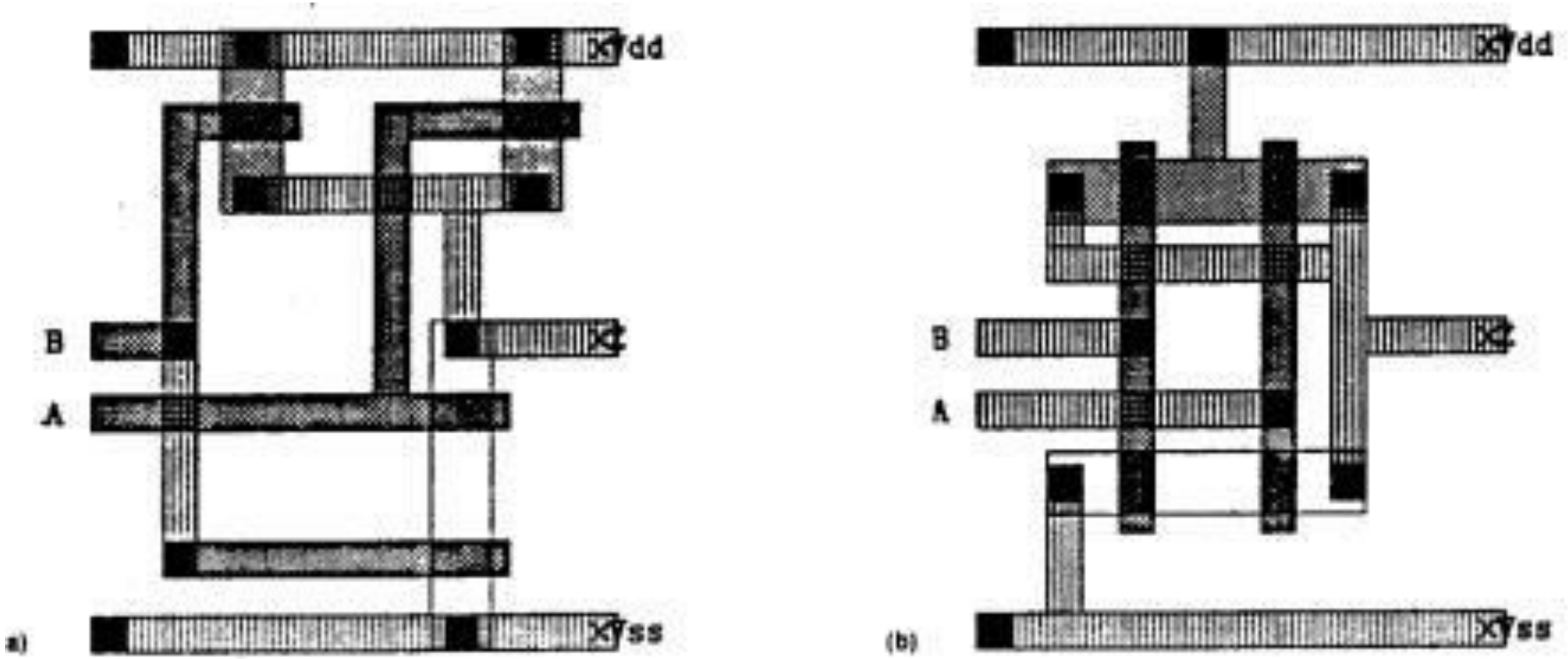


(b)



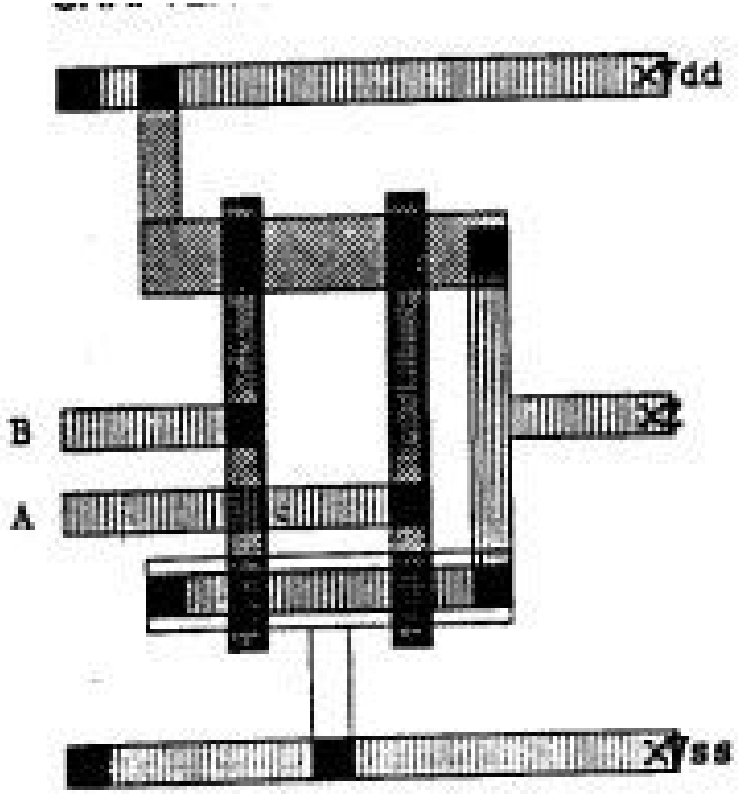
Electrical and Physical Design of Logic Gates

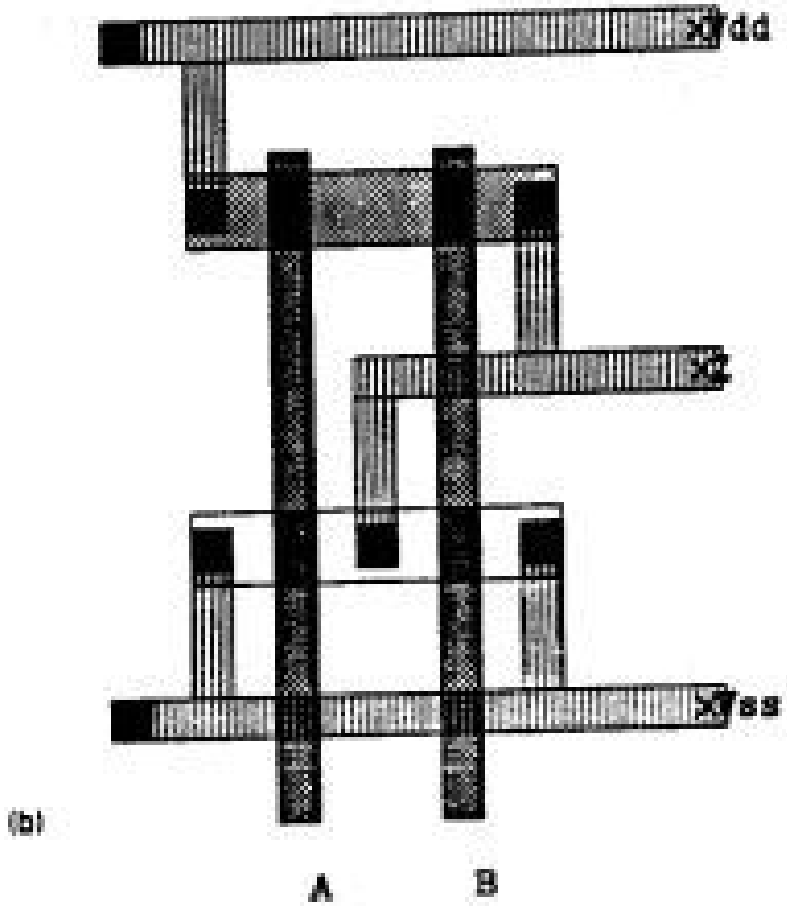
- NAND gates



Electrical and Physical Design of Logic Gates

- NOR Gate





Electrical and Physical Design of Logic Gates

❖ *Body Effect*

- **Definition:** Change in threshold voltage (Vt) due to source-substrate voltage difference.
- Occurs when source ≠ substrate potential.
- Increases threshold voltage → slows down switching.
- Affects nMOS more prominently in series-connected transistors.

•Body effect expressed as:

$$V_t = V_{to} + \gamma(\sqrt{(|V_{sb} + 2\phi_f|)} - \sqrt{(2\phi_f)})$$

•V_{sb} = Voltage between source and body

•ΔV_t = Change in threshold voltage due to $V_{sb} > 0$

NAND Gate Example

•nMOS transistors A-C initially at 0V.

•Input D turns ON, charges internal node C1.

•When all inputs HIGH, output node discharge through D.

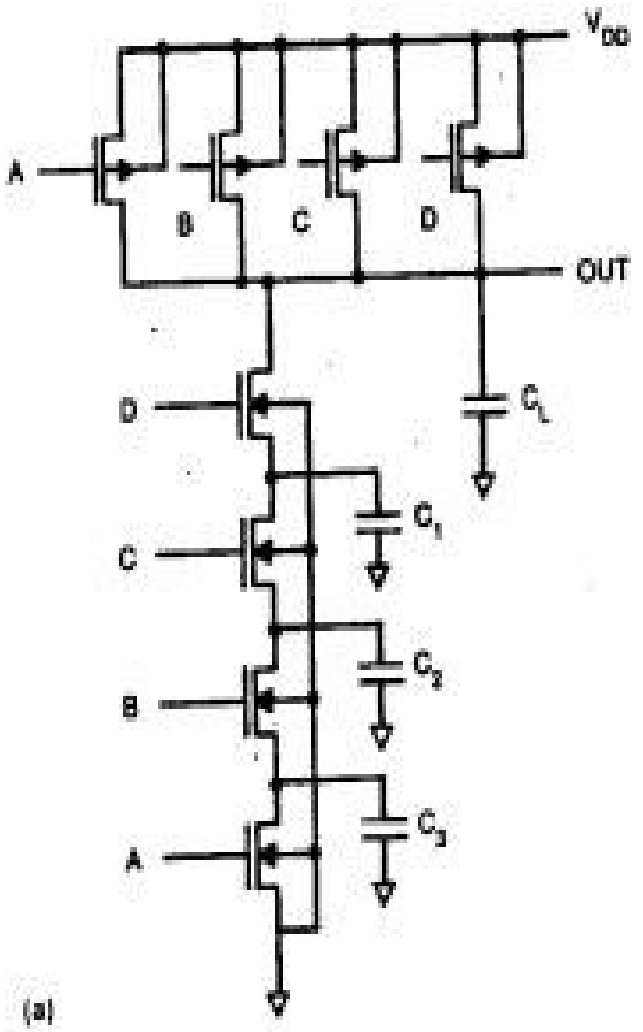
•D experiences higher Vsb → higher Vt → slowe switching.

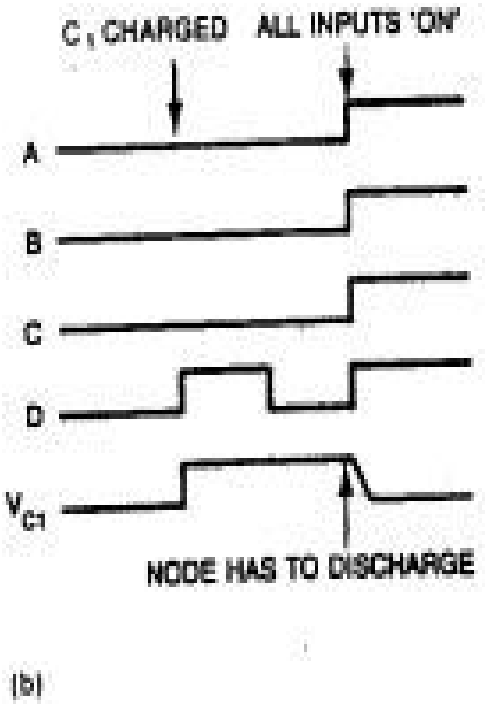
Impact on Gate Delay

•Fall time increases due to slowed discharge path.

•Series-connected nMOS more affected tha pMOS.

•Must account for worst-case body effect i timing.





Design Implications

•Minimize internal node capacitance.

•Reduce number of series transistors in path.

•Prefer NOR if pMOS delay impact is lower.

Optimization Strategies

•**1. Time Sequencing:**

- Early signals discharge internal nodes.
- Late signals switch low-body-effect transistors.

•**2. Capacitance Minimization:**

- Use metal/poly for internal connections.
- Avoid diffusion wiring between internal nodes.
- Keep diffusion area minimal.

•**Layout Considerations**

•Use buried contacts where allowed.

•Complete internal connections in metal or polysilicon.

•Minimize parasitic capacitance by layout rules.

Summary

•Body effect slows down switching due to raised Vt.

•Most visible in series nMOS transistors.

•Smart layout and signal timing reduce its impact.

Input-Output (I/O) Structures

- General pad Layouts
- V_{dd} and V_{ss} pads
- Output pads
- Input pads
- Tri-state pads
- Bi-directional pads

Input-Output (I/O) Structures

Importance of I/O Structures

- I/O design is among the most challenging parts of CMOS circuit design.
- Requires a deep understanding of:
  - Pad layout constraints
  - ESD protection
  - Signal integrity
  - Power delivery
- Poor I/O design can cause chip failure or poor system performance.

I/O Pad Frame – Overall Organization

- Pads are arranged along the chip periphery.
- Standard pad size: ~150 µm × 150 µm.
- Connection points must match predefined locations for packaging.
- Pads are typically grouped:
  - Power pads (VDD, VSS)
  - Input pads
  - Output pads

Example Ordering:

LEFT:

INPUT A

INPUT B

- TOP:

INPUT C

VDD VDD

RIGHT:

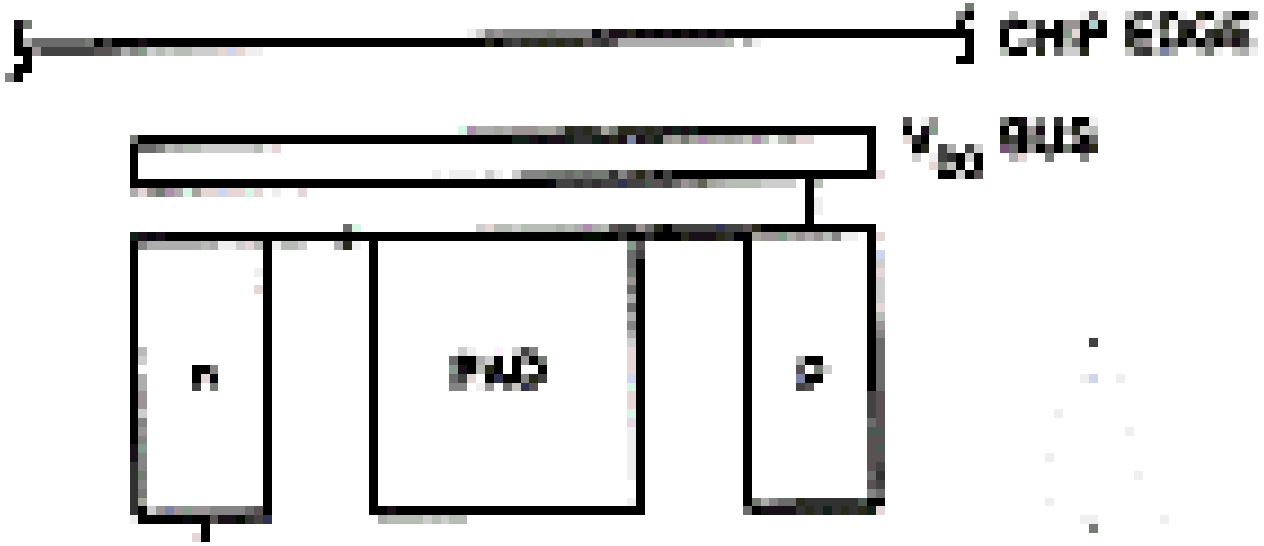
OUTPUT Z

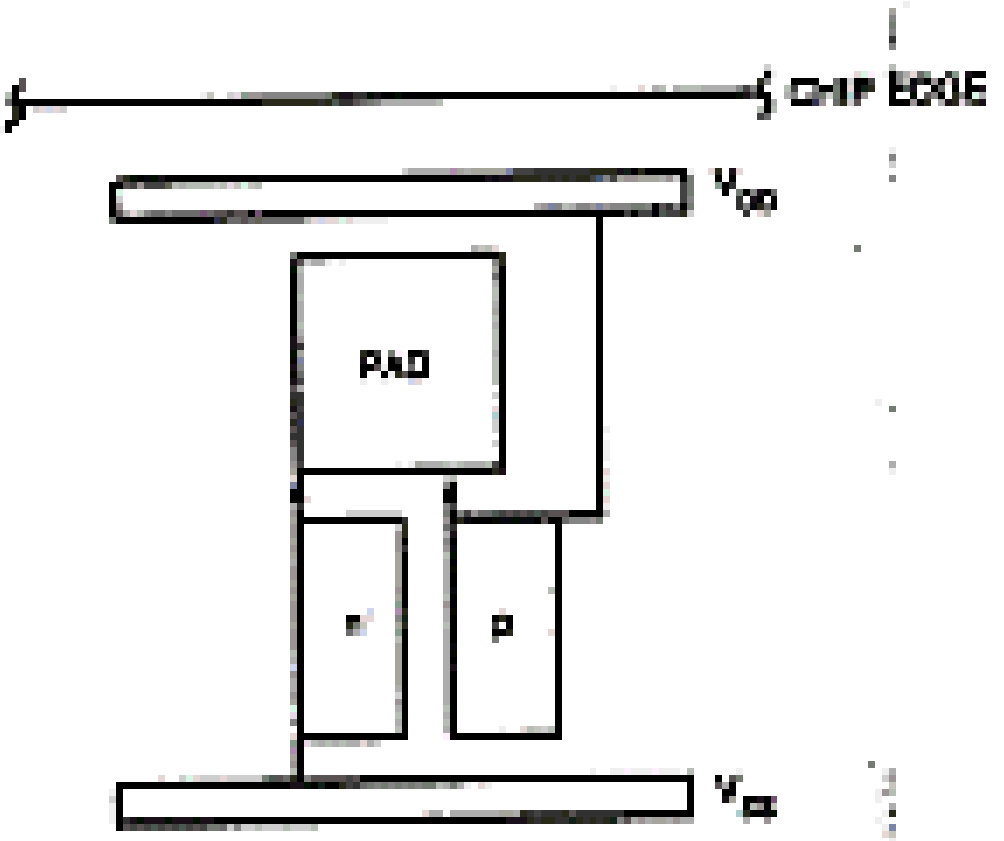
OUTPUT Y

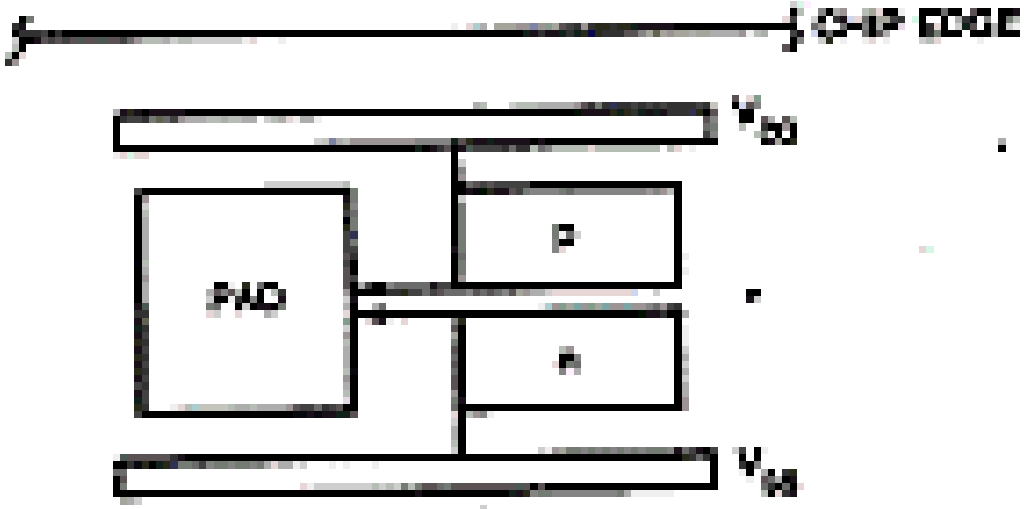
BOTTOM:

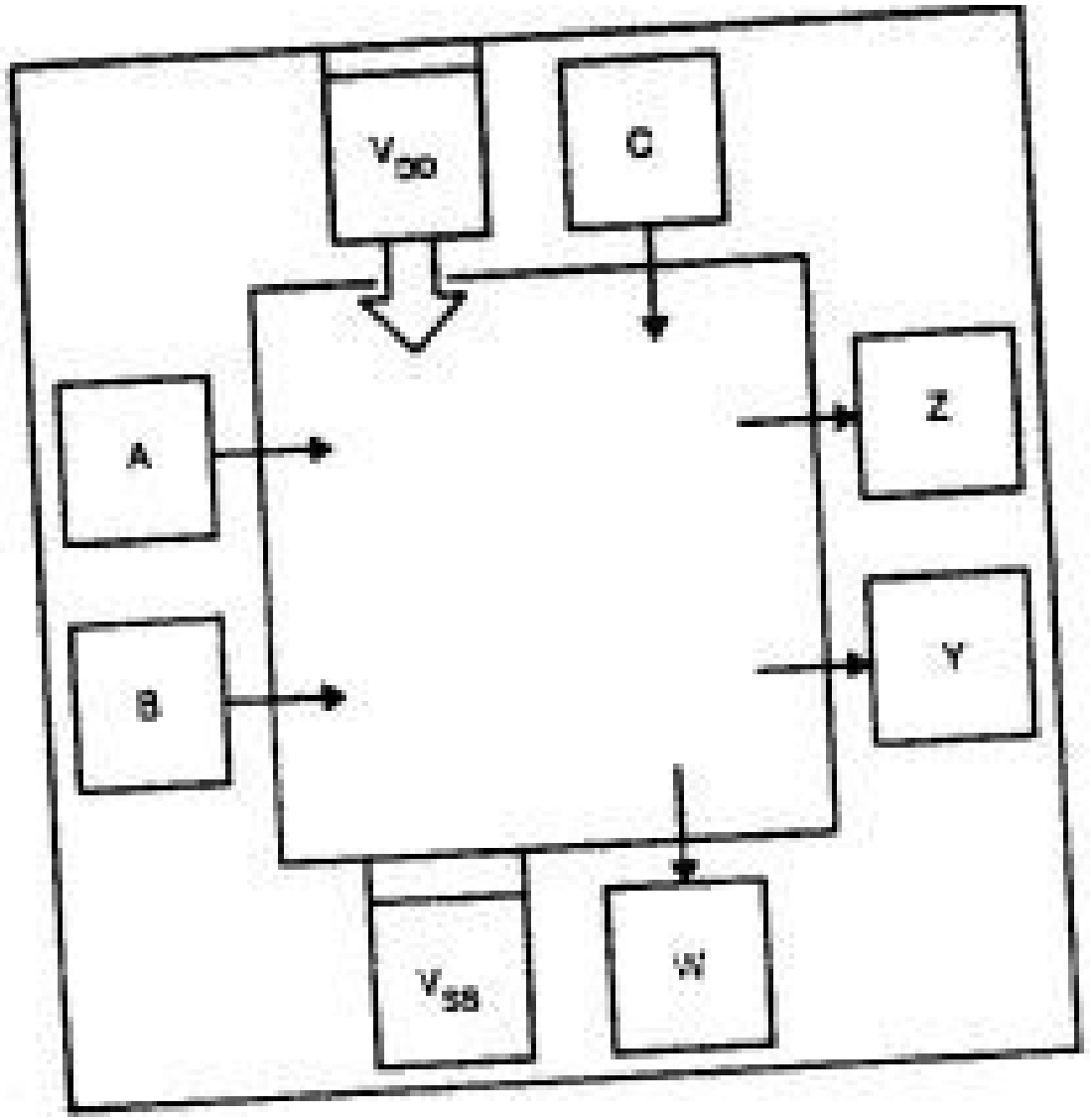
OUTPUT X

VSS VSS

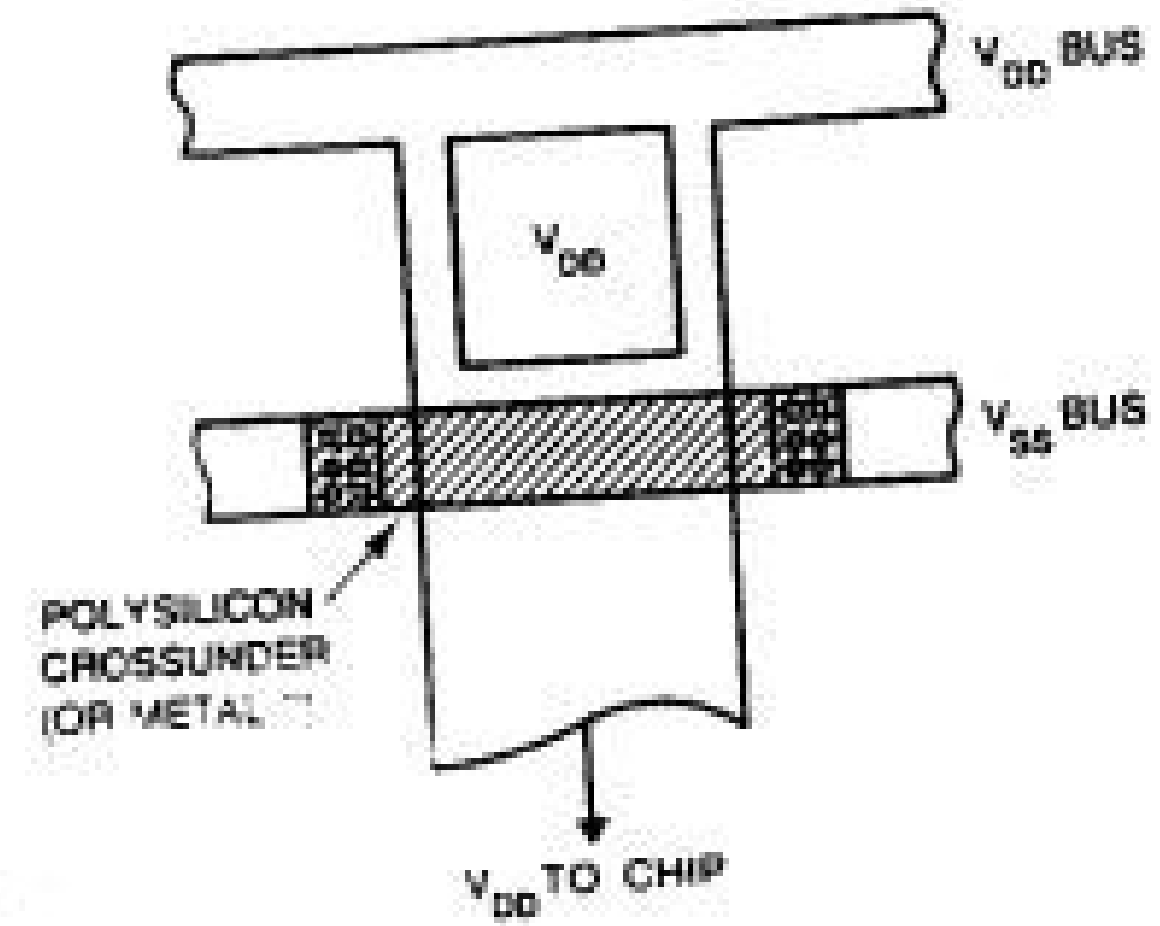

CHIP EDGE
V_{SS} BUS
n
PAD
p


CHIP EDGE
V_{DD}
PAD
n
p
V_{SS}


CHIP EDGE
V_{SS}
PAD
p
n
V_{DD}


V_{DD}
C
A
Z
B
Y
V_{SS}
W

(a)


V_{DD} BUS
V_{DD}
V_{SS} BUS
POLYSILICON
CROSSUNDER
(OR METAL
V_{DD} TO CHIP

(b)

General Pad Layouts

- Pads consist of metal areas connected to power or signal buses.
- May include vias for connectivity.
- VDD/VSS pads connected using metal, poly, or stacked vias.
- No need to minimize power pad size.

Types:

1. Simple metal connection
2. Poly crossover for compact layout
3. Double-layer via connections for strength

Output Pads – Requirements & Design

- Must handle:
  - Large capacitive loads
  - Fast switching requirements
- Use strong buffers:
  - Often a two-stage inverter chain
  - Sizing ratio ~2:7 for strength
- Output stage must meet:
  - DC drive current
  - Rise/fall time targets

Output Pads – Additional Considerations

- Pad capacitance must be matched with required speed.
- Consider use of non-inverting or two-stage drivers.
- Buffers help avoid signal degradation and noise.

Example:

- A high capacitive load may require:
  - Large transistor sizes
  - Lower output resistance

Input Pads – Structure and Timing

- Connected to external signals through pads.
- Must be protected against ESD and high voltage spikes.
- Input resistance: very high (limits input current).

Key Design Equation:

$$V = \frac{I \cdot \Delta t}{C}$$

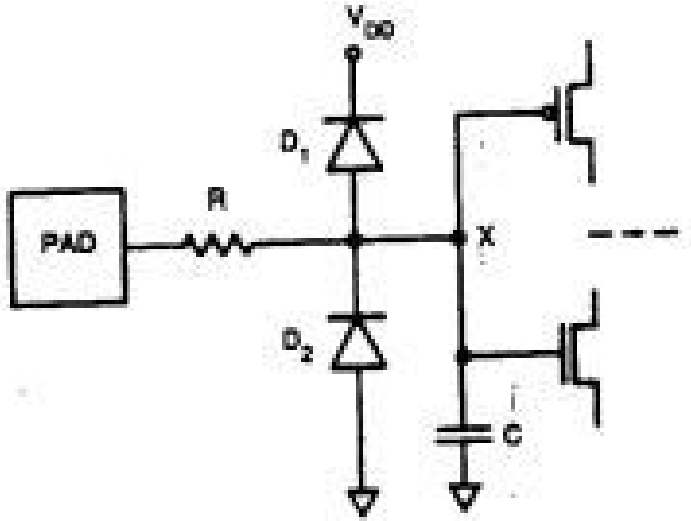
- Where:
  - V = Voltage rise on gate
  - I = Charging current
  - Δt = Time
  - C = Gate capacitance

ESD Protection – Input Pads

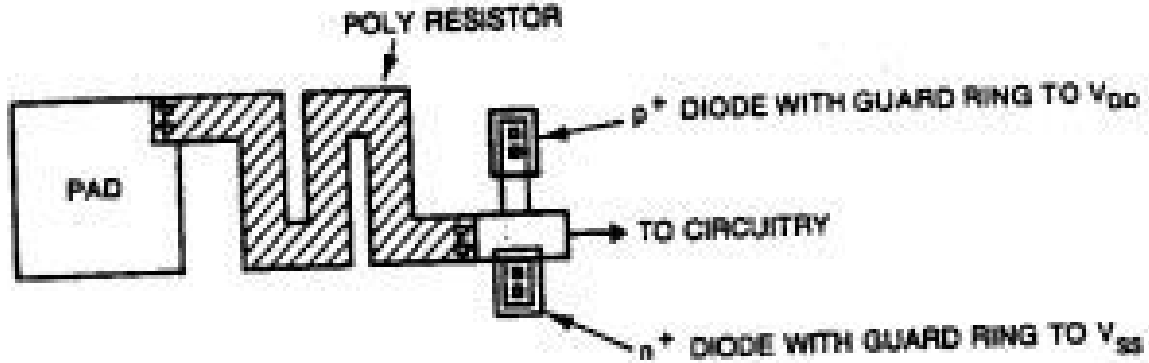
- Use of diode clamps (D1, D2) to VDD and VSS.
- Resistors to limit current.
- Guard rings isolate sensitive areas.

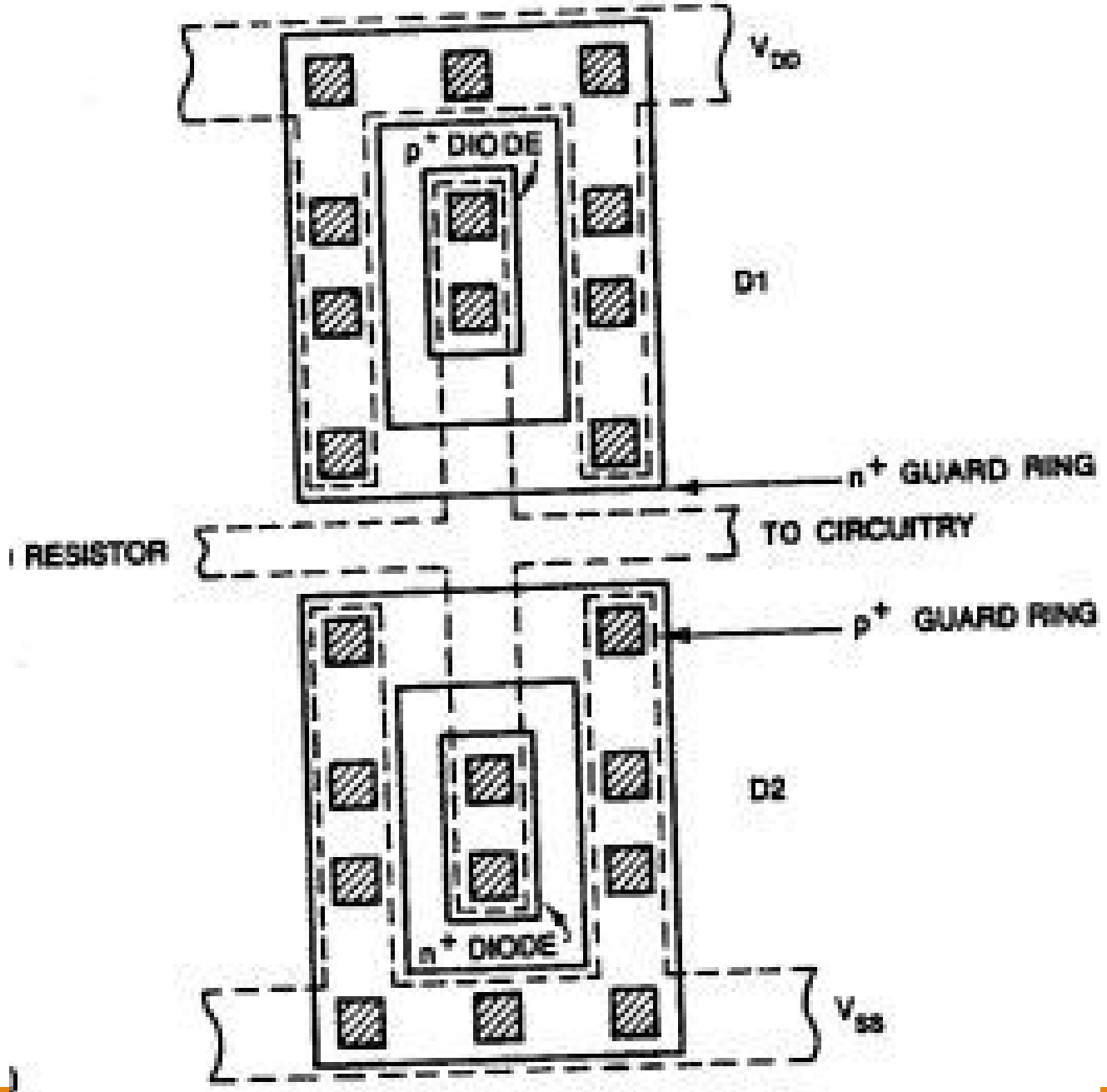
Design Elements:

- Poly resistors
- Diffused guard rings
- Vias to connect to supply



TYPICAL INPUT PROTECTION CIRCUIT




V_{DD}
p^+ DIODE
D1
n^+ GUARD RING
TO CIRCUITRY
RESISTOR
p^+ GUARD RING
D2
n^+ DIODE
V_{SS}

Input Pad Design Practices

- Clamp input pad to prevent latch-up and damage.
- Use wide diffusions and guard rings.
- Avoid punch-through and parasitic conduction paths.

Latch-up Prevention Tips:

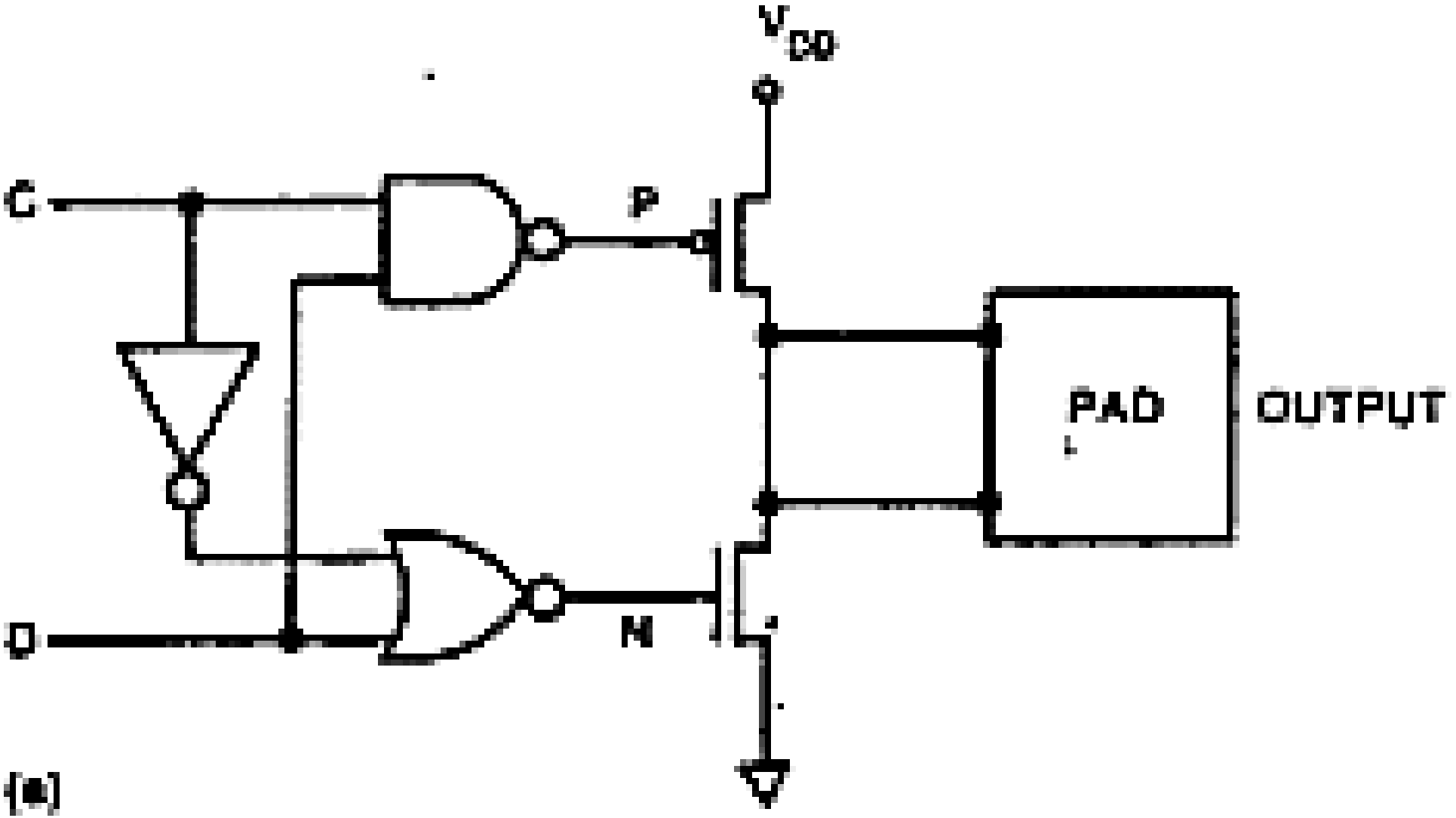
- Separate nMOS and pMOS devices
- Tie guard rings to VDD/VSS

Tri-State Pads

- Allow output to be driven or disabled (High-Z state).
- Used on shared data buses.
- Controlled by enable signal to activate buffer

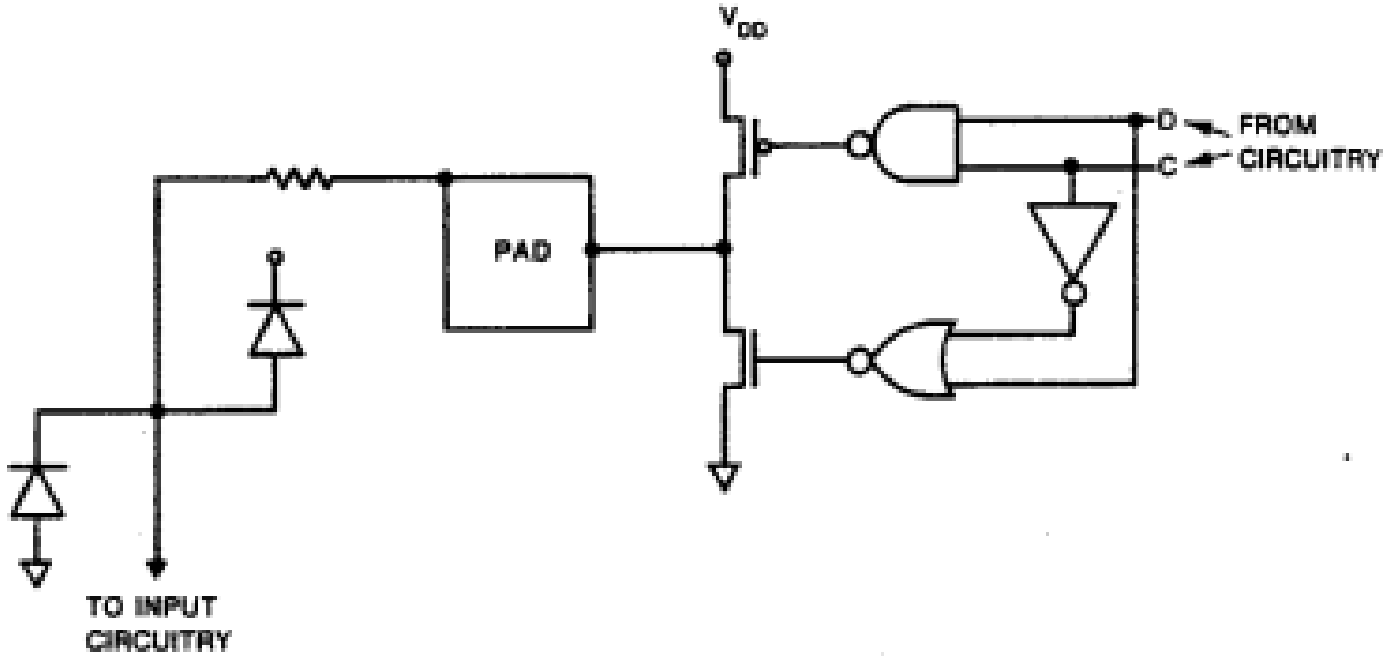
TRUTH TABLE

C	D	M	P	OUTPUT
0	X	0	1	Z (HIGH IMPEDANCE)
1	0	1	1	0
1	1	0	0	1


V_{CC}
C
P
PAD
OUTPUT
D
N
(a)

Bi-Directional Pads

- Combine input and tri-state structures.
- Can switch between input and output mode.
- Use direction control logic.
- Example Applications:
  - Data buses
  - Microcontroller



Summary

- Good I/O design ensures:
  - Reliability
  - Signal integrity
  - Protection from ESD
- Use:
  - Well-sized buffers
  - ESD diodes and resistors
  - Proper pad layout and ordering
- Pay attention to:
  - Power rail placement
  - Latch-up susceptibility