VLSI Design and Testing
BEC602

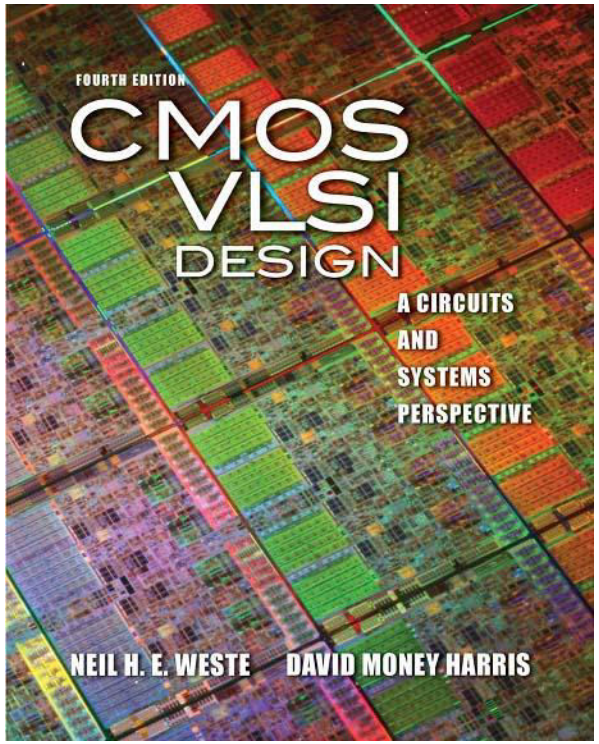
Module 1

Introduction and MOS Transistor Theory

CSP
Assistant Professor,
Department of ECE,

Module-1
Introduction and MOS Transistor Theory

- **Introduction:** A Brief History, MOS Transistors, CMOS Logic **(1.1 to 1.4 of TEXT2)**
- **MOS Transistor Theory:** Introduction, Long-channel I-V Characteristics, Non-ideal I-V Effects, DC Transfer Characteristics **(2.1, 2.2, 2.4 and 2.5 of TEXT2).**



Course Outcomes

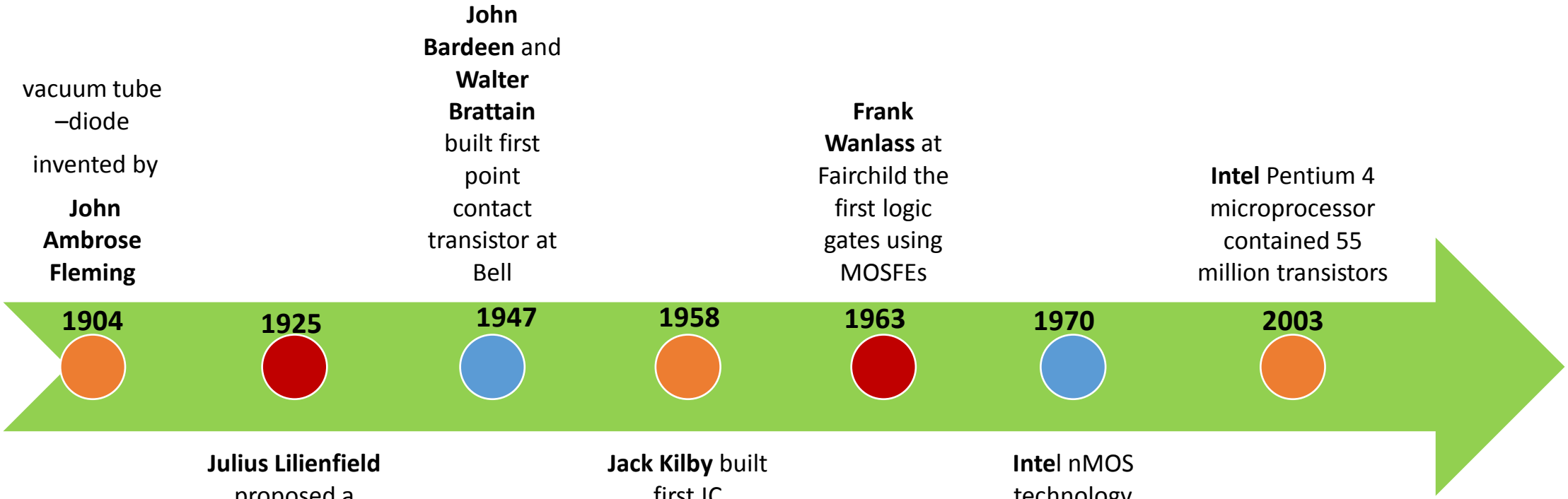
After studying this course, students will be able to:

- Demonstrate understanding of MOS transistor theory, CMOS fabrication flow and technology scaling.
- Draw the basic gates using the stick and layout diagrams with the knowledge of physical design aspects.
- Demonstrate ability to design Combinational, sequential and dynamic logic circuits as per the requirements
- Interpret Memory elements along with timing considerations
- Interpret testing and testability issues in VLSI Design

A Brief History

The history of VLSI…

History of VLSI



History of VLSI

- nMOS process was less expensive than CMOS,
- nMOS logic gates still consumed power while idle.
- Power consumption major issue in the 1980s
- Hundreds of thousands (10^5) of transistors were integrated onto a single die.
- CMOS processes were widely adopted and have essentially replaced nMOS and bipolar processes for nearly all digital logic.

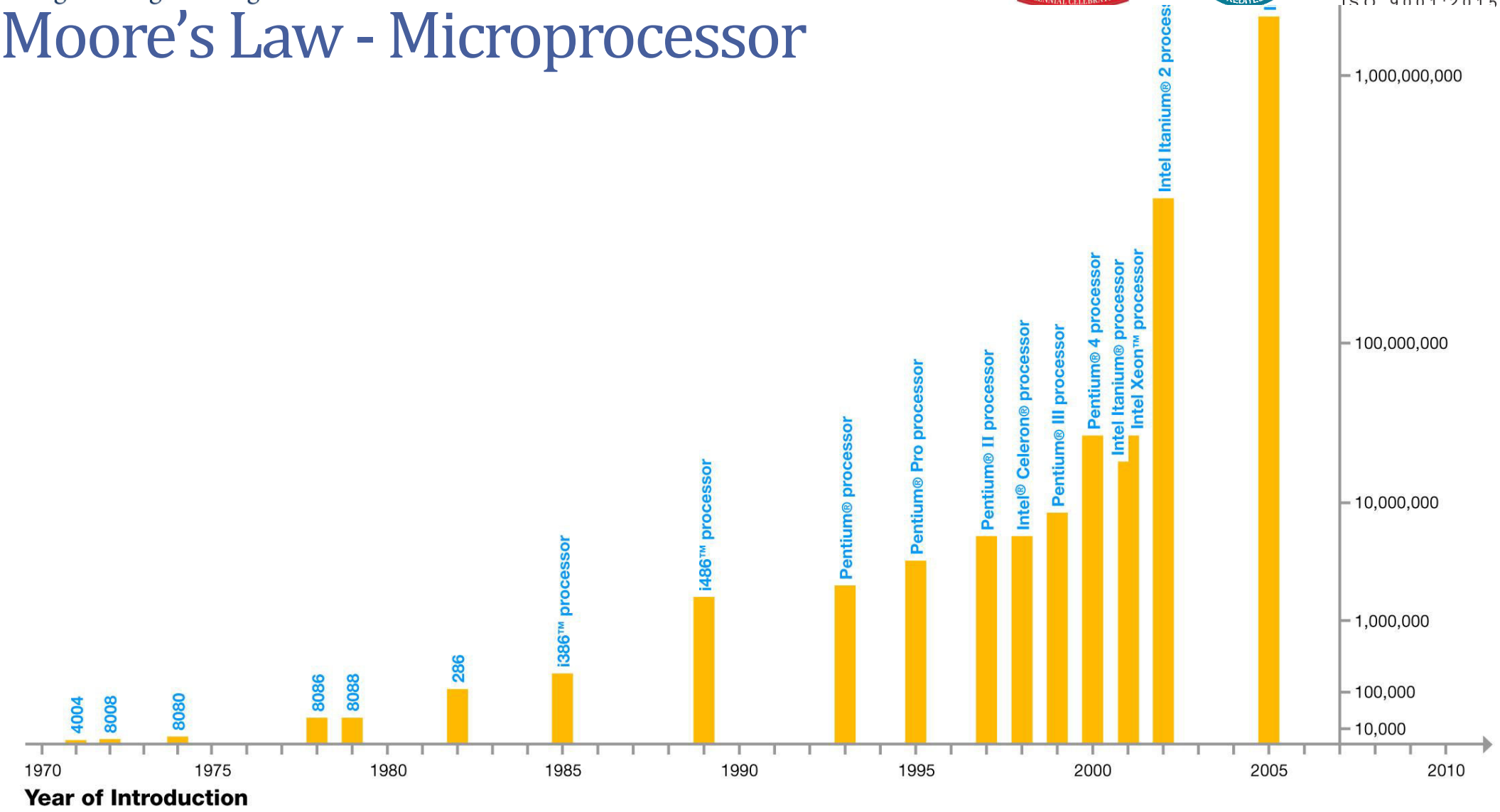
History of VLSI

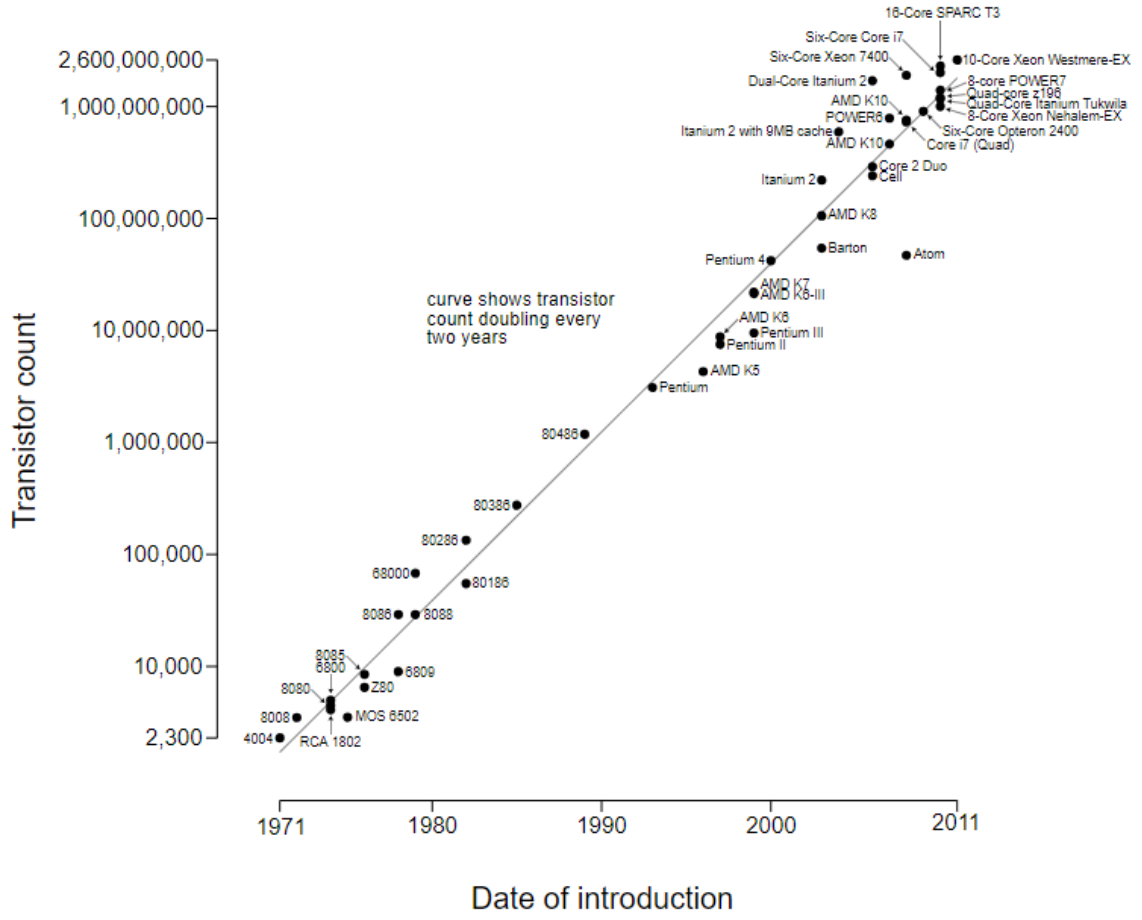
- Gordon Moore observed in 1965 that

  "...*plotting the number of transistors that can be most economically manufactured on a chip gives a straight line on a semilogarithmic scale...*"

- At the time he found transistor count doubling every 18 months. This observation has been called **Moore's Law**

Moore's Law - Microprocessor




Transistor count
2,600,000,000
1,000,000,000
100,000,000
10,000,000
1,000,000
100,000
10,000
2,300
1971
1980
1990
2000
2011
Date of introduction
curve shows transistor count doubling every two years
16-Core SPARC T3
Six-Core Core i7
Six-Core Xeon 7400
10-Core Xeon Westmere-EX
Dual-Core Itanium 2
8-core POWER7
Quad-core z196
AMD K10
Quad-Core Itanium Tukwila
POWER6
8-Core Xeon Nehalem-EX
Itanium 2 with 9MB cache
Six-Core Opteron 2400
AMD K10
Core i7 (Quad)
Core 2 Duo
Itanium 2
Cell
AMD K8
Barton
Atom
Pentium 4
AMD K7
AMD K8-III
AMD K8
Pentium III
Pentium II
AMD K5
Pentium
80486
80386
80286
68000
80186
8086
8088
8085
6800
8809
Z80
8080
8008
MOS 6502
4004
RCA 1802

Intel® Microprocessor Transistor Count Chart

Microprocessor	Year of Introduction	Transistors
4004	1971	2,300
8008	1972	2,500
8080	1974	4,500
8086	1978	29,000
Intel286	1982	134,000
Intel386™ processor	1985	275,000
Intel486™ processor	1989	1,200,000
Intel® Pentium® processor	1993	3,100,000
Intel® Pentium® II processor	1997	7,500,000
Intel® Pentium® III processor	1999	9,500,000
Intel® Pentium® 4 processor	2000	42,000,000
Intel® Itanium® processor	2001	25,000,000
Intel® Itanium® 2 processor	2003	220,000,000
Intel® Itanium® 2 processor (9MB cache)	2004	592,000,000

MOS Transistors

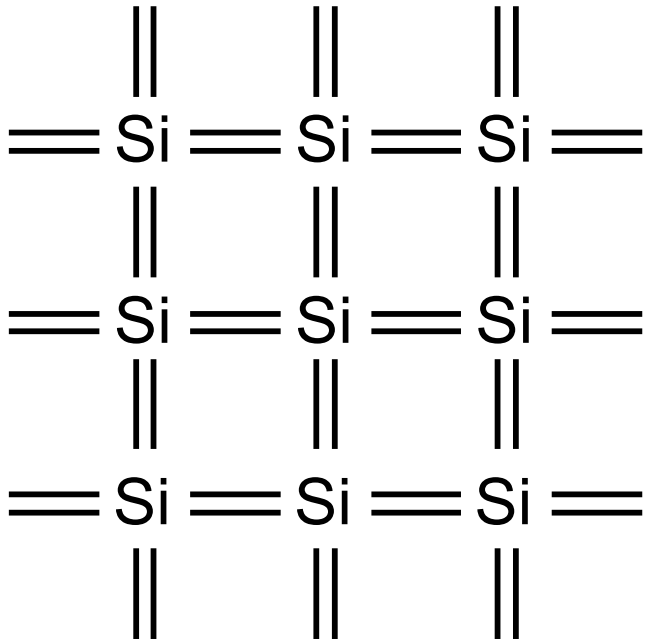
Introduction to MOS Transistors

Introduction

- Integrated circuits: many transistors on one chip.
- *Very Large Scale Integration* (VLSI): bucketloads!
- *Complementary Metal Oxide Semiconductor*
  - Fast, cheap, low power transistors
- Today: How to build your own simple CMOS chip
  - CMOS transistors
  - Building logic gates from transistors
  - Transistor layout and fabrication
- Rest of the course: How to build a good CMOS chip

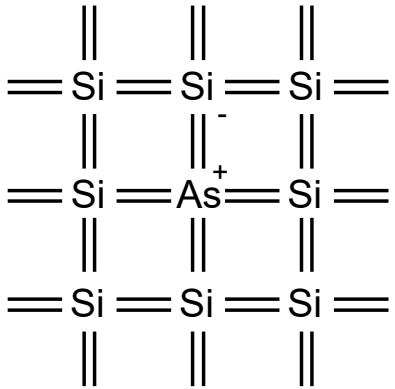
Silicon Lattice

- Transistors are built on a silicon substrate
- Silicon is a Group IV material
- Forms crystal lattice with bonds to four neighbors



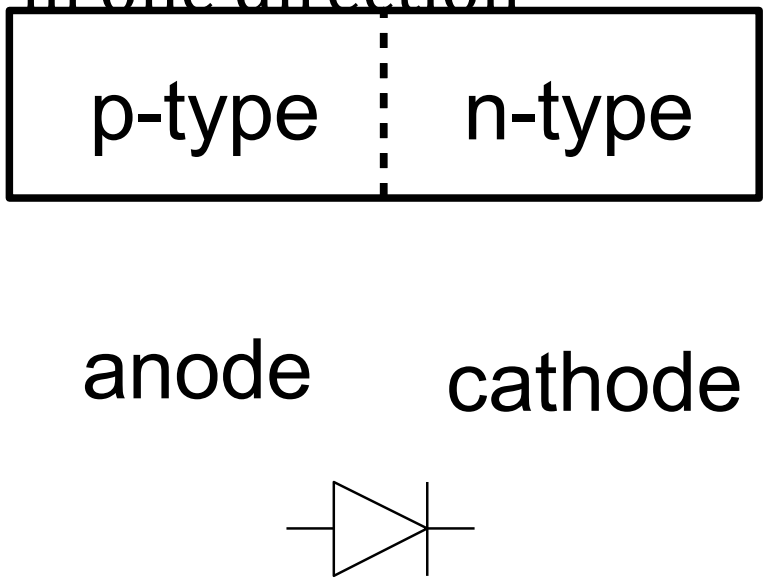
Dopants

- Silicon is a semiconductor
- Pure silicon has no free carriers and conducts poorly
- Adding dopants increases the conductivity
- Group V: extra electron (n-type)
- Group III: missing electron, called hole (p-type)



p-n Junctions

- A junction between p-type and n-type semiconductor forms a diode.
- Current flows only in one direction



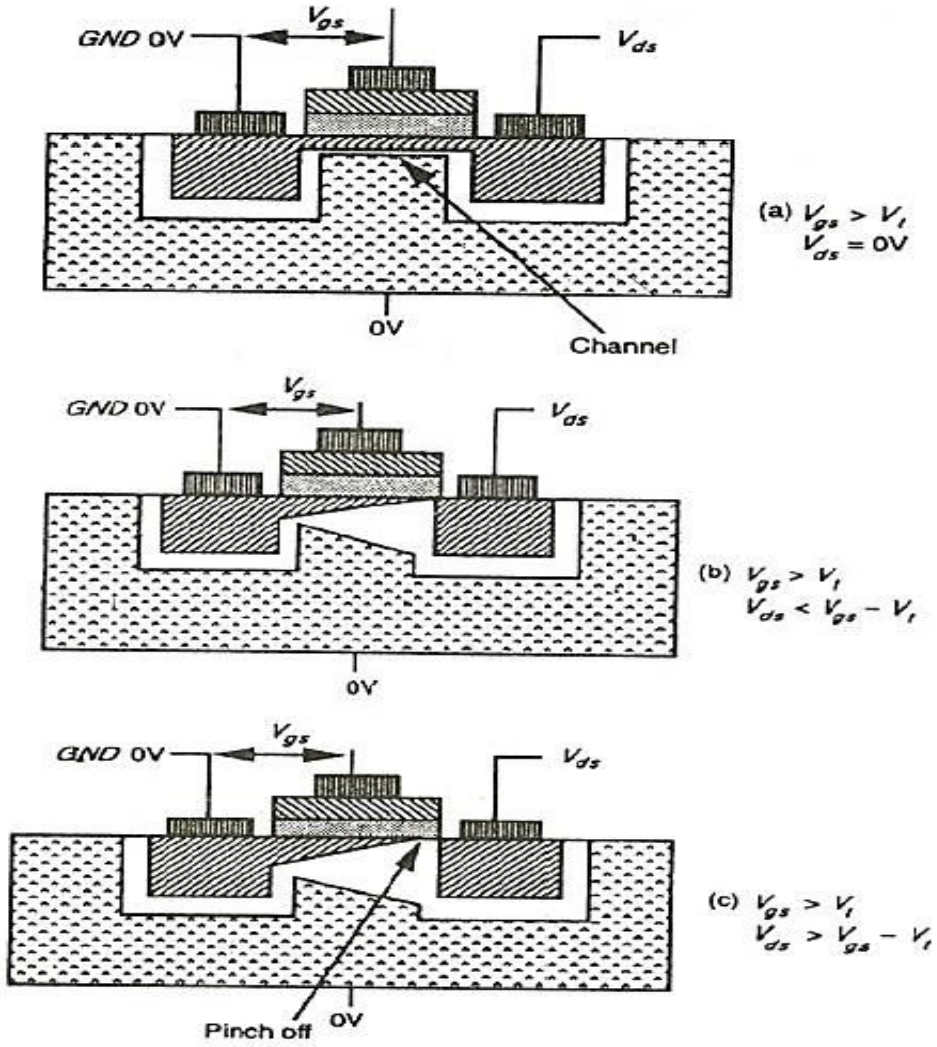
Enhancement mode transistor (channel is going to form after giving a proper positive gate voltage)		Depletion mode transistor (channel will be present by the implant. It can be removed by giving a proper negative gate voltage)	
nMOS	pMOS	nMOS	pMOS
normally off	normally on	normally ON, even with Vgs=0	normally Off, even with Vgs=0
giving a +ve gate voltage a channel of electrons is formed between source drain	A Channel of Holes can be performed by giving a –ve gate voltage	The channel will be implanted while fabricating, hence it is normally ON. To cause the channel to cease to exist, a – ve voltage must be applied between gate and source	Mobility of electrons is 2.5 to 3 times faster than holes. Hence P-MOS devices will have more resistance compared to NMOS

Enhancement mode Transistor action

threshold voltage for an enhancement mode transistor is given by Vt = 0.2 * Vdd

Depletion mode Transistor action: -

We can explain the working of depletion mode transistor in the same manner, as that of the enhancement mode transistor only difference is, channel is established due to the implant even when Vgs = 0 and the channel can be cut off by applying a -ve voltage between the gate and source. Threshold voltage of depletion mode transistor is around 0.8*Vdd.



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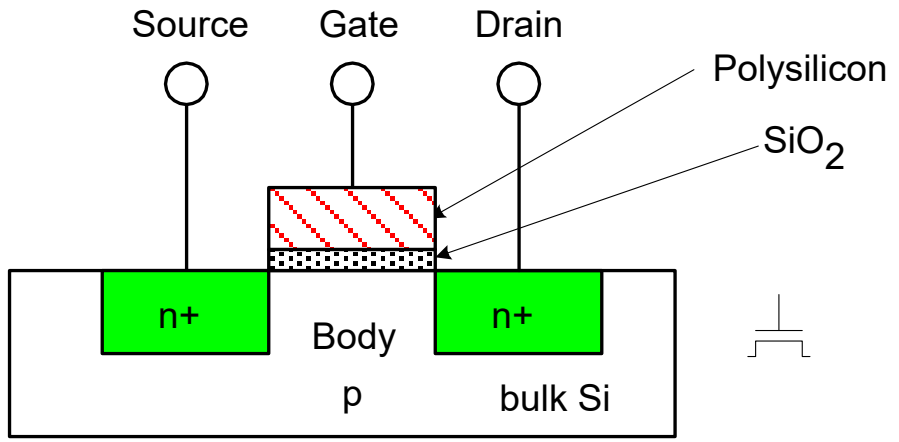
nMOS Transistor

- Four terminals: gate, source, drain, body
- Gate – oxide – body stack looks like a capacitor
  - Gate and body are conductors
  - SiO_2 (oxide) is a very good insulator
  - Called metal – oxide – semiconductor (MOS) capacitor
  - Even though gate is no longer made of metal*



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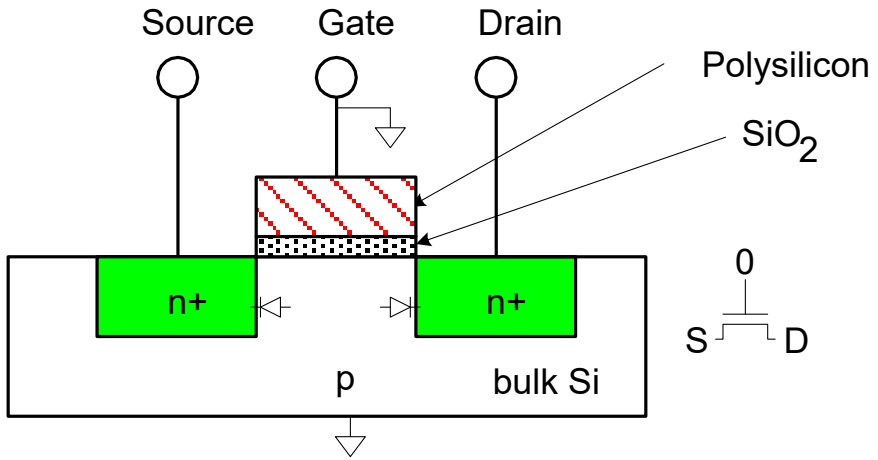
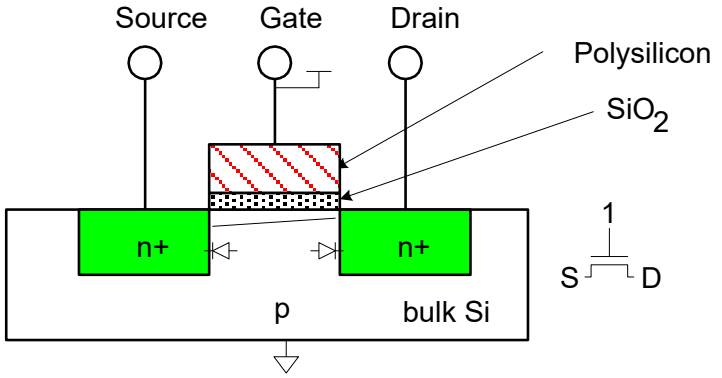
nMOS Operation

- Body is usually tied to ground (0 V)
- When the gate is at a low voltage:
  - P-type body is at low voltage
  - Source-body and drain-body diodes are OFF
  - No current flows, transistor is OFF



nMOS Operation Cont.

- When the gate is at a high voltage:
  - Positive charge on gate of MOS capacitor
  - Negative charge attracted to body
  - Inverts a channel under gate to n-type
  - Now current can flow through n-type silicon from source through channel to drain, transistor is ON



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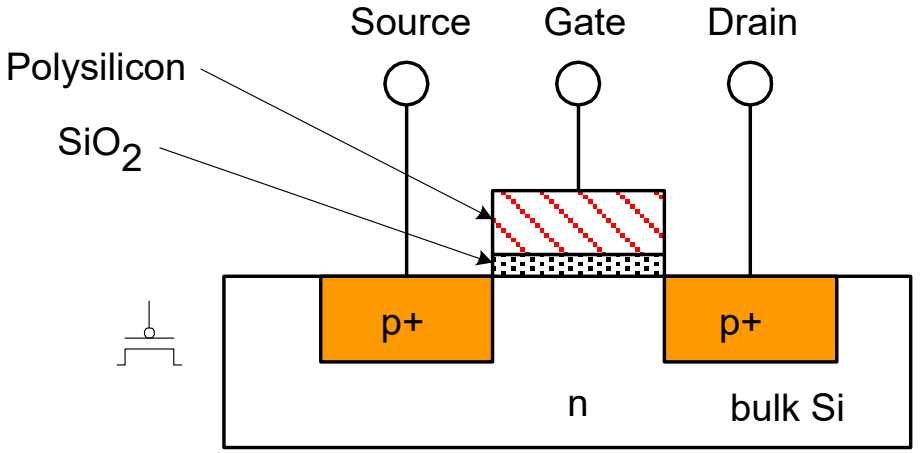
pMOS Transistor

- Similar, but doping and voltages reversed
  - Body tied to high voltage (V_{DD})
  - Gate low: transistor ON
  - Gate high: transistor OFF
  - Bubble indicates inverted behavior



Power Supply Voltage

- GND = 0 V
- In 1980's, V_{DD} = 5V
- V_{DD} has decreased in modern processes
  - High V_{DD} would damage modern tiny transistors
  - Lower V_{DD} saves power
- V_{DD} = 3.3, 2.5, 1.8, 1.5, 1.2, 1.0, …

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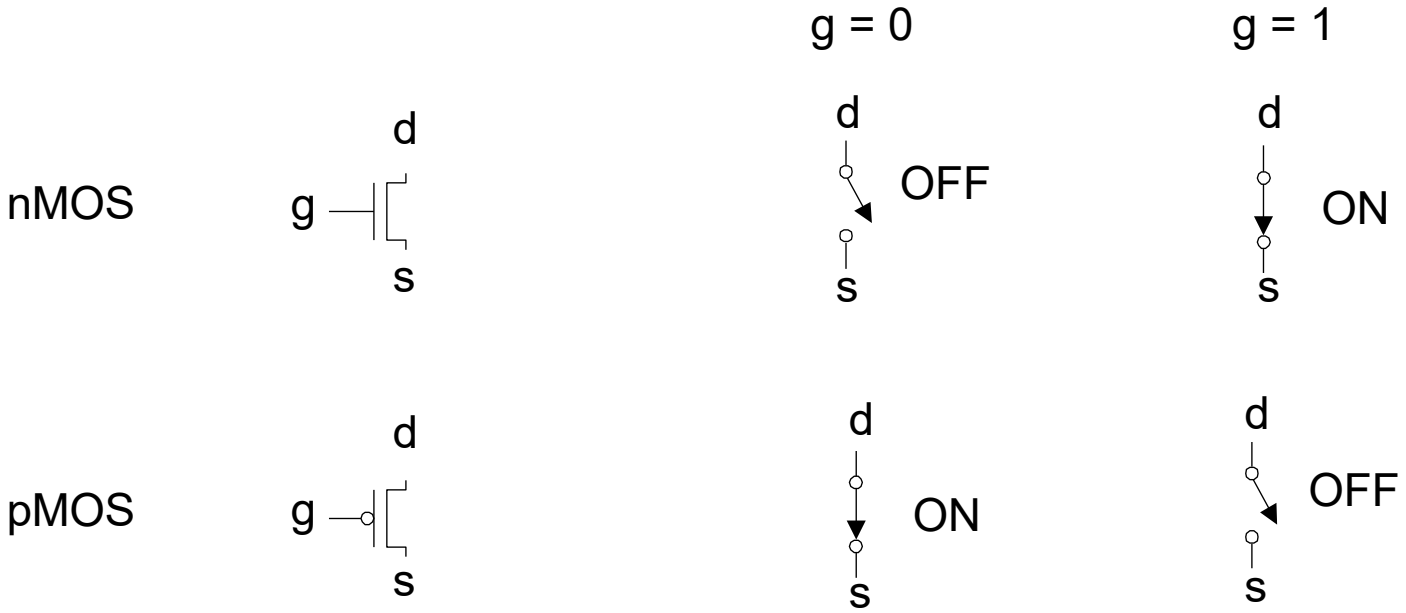
Transistors as Switches

- We can view MOS transistors as electrically controlled switches
- Voltage at gate controls path from source to drain

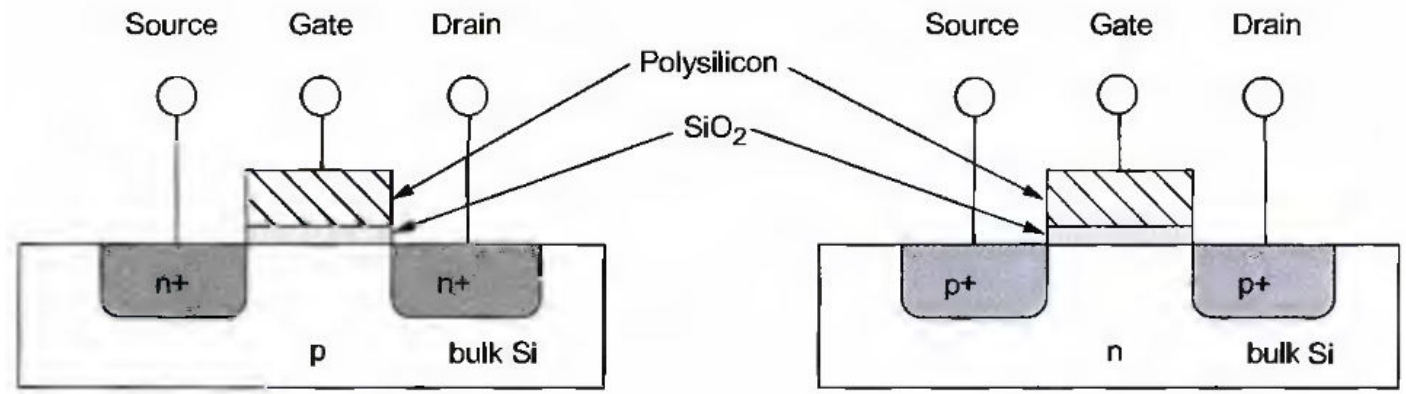


MOS Devices

MOSWorking.mp4

MOS Transistor Working

- deposition and etching of aluminum or other metals to provide interconnection
- Layers grown on a single crystal of silicon
- Thin flat circular wafers around 15-30 cm in diameter.



nMOS

pMOS

CMOS Logic

Basics of CMOS Logic

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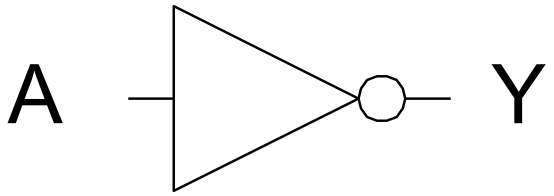
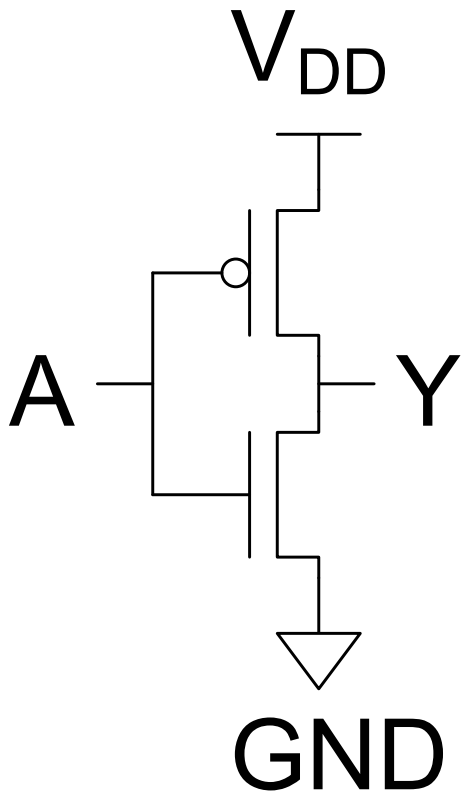
CMOS Inverter

A	Y





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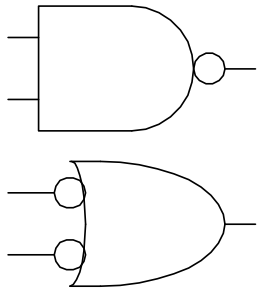
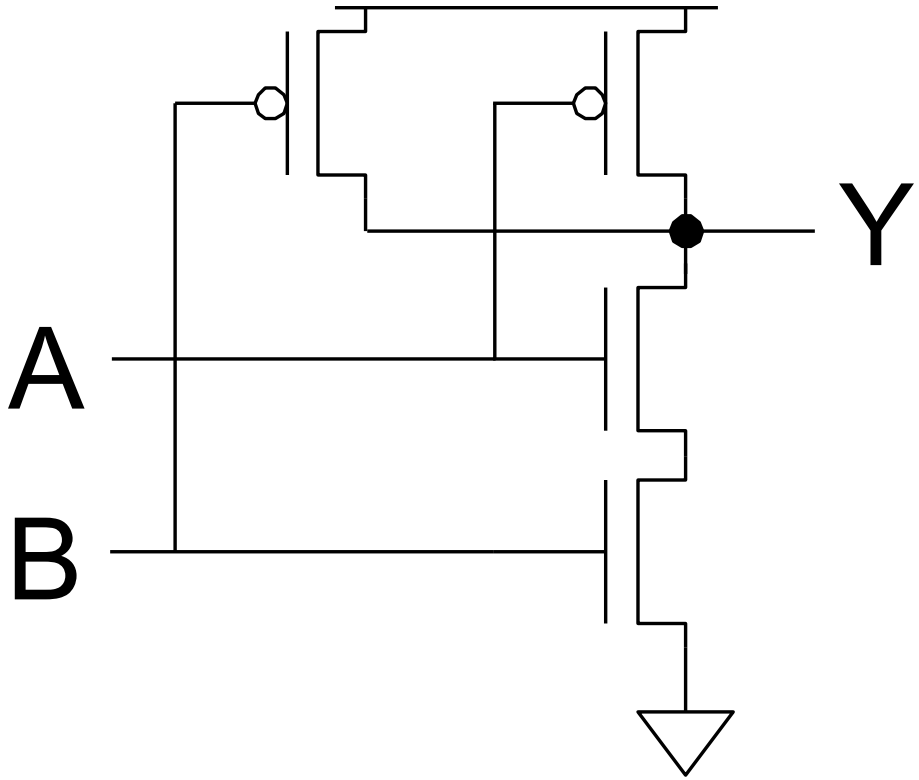
CMOS NAND Gate

A	B	Y
0	0	
0	1	
1	0	
1	1	





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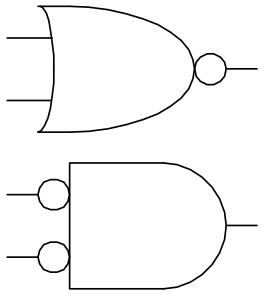
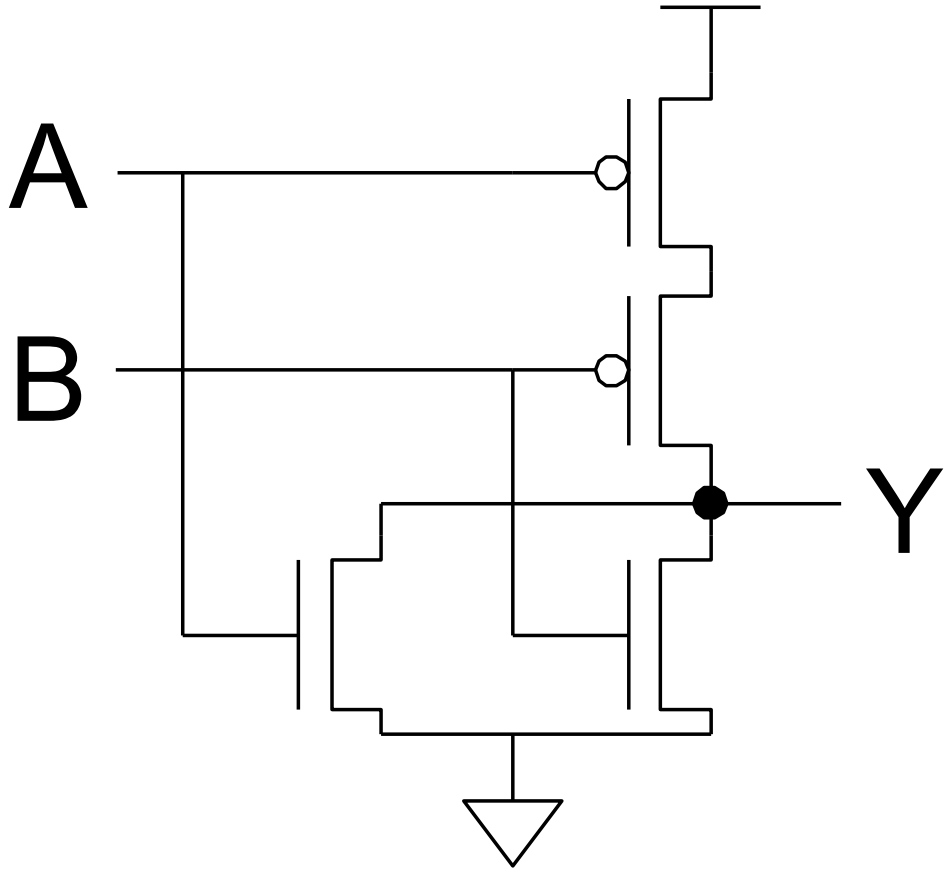
CMOS NOR Gate

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

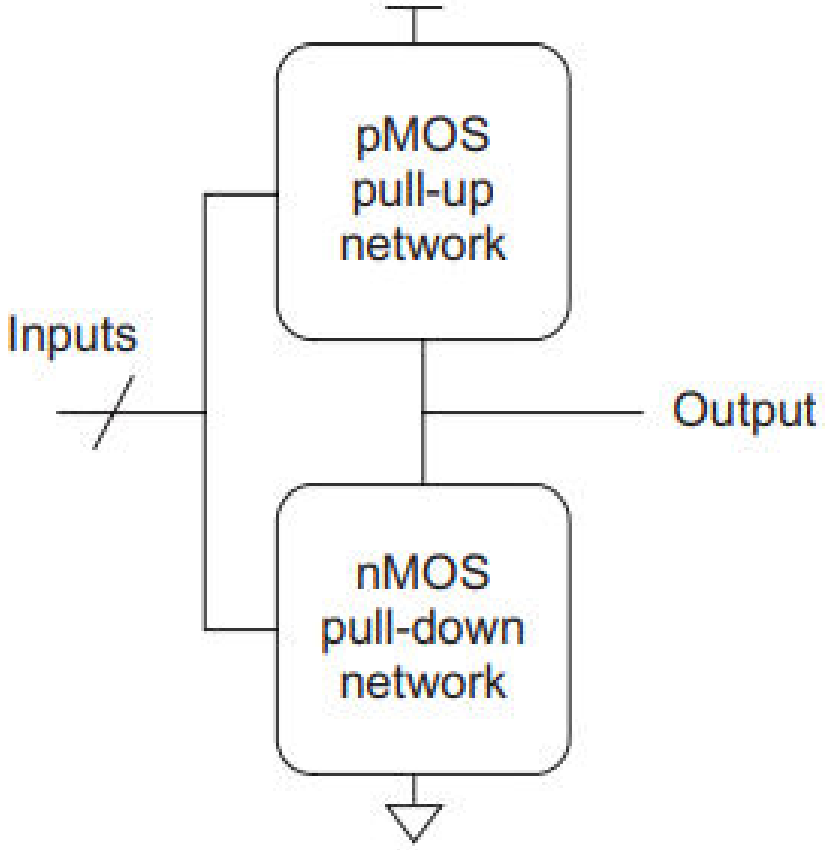


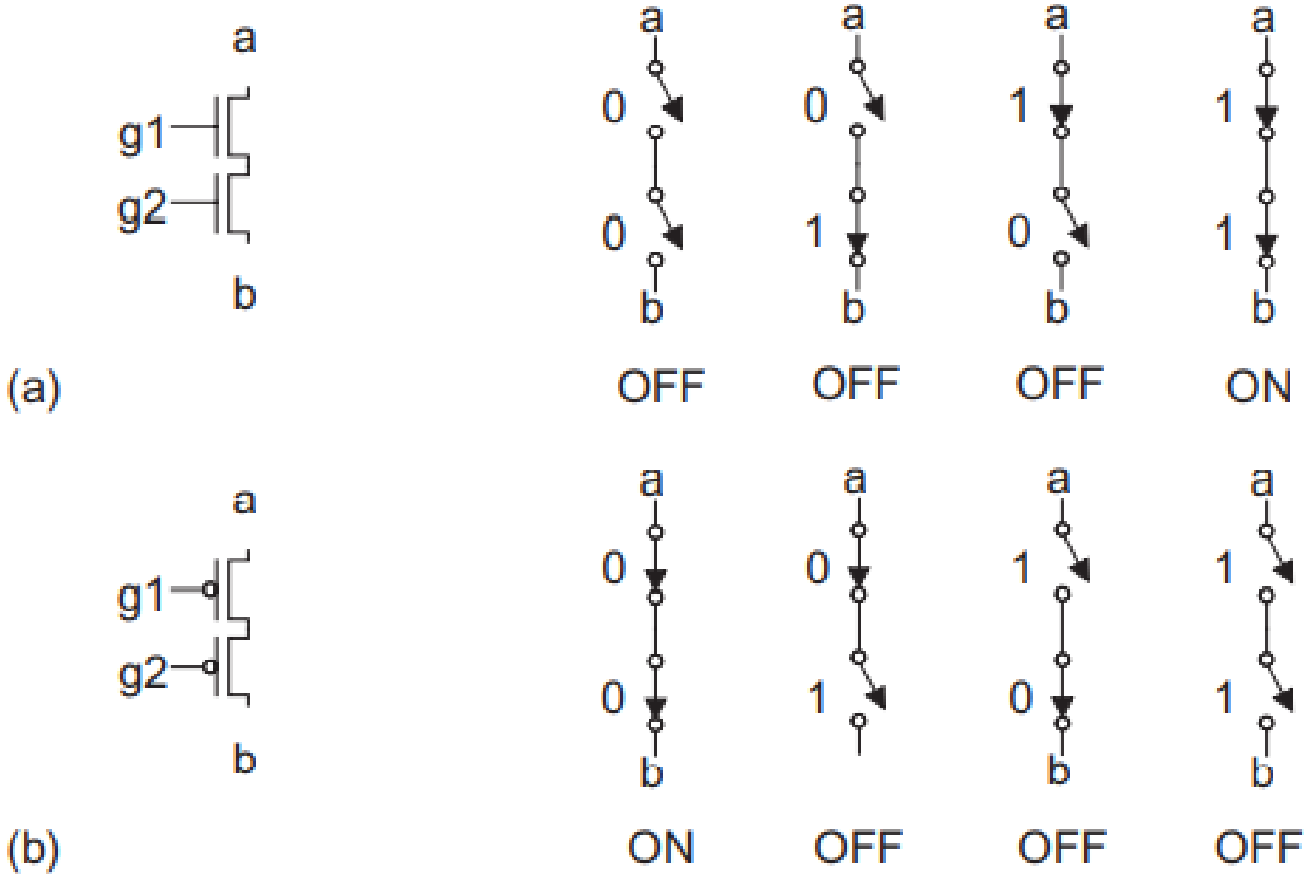


3-input NAND Gate

- Y pulls low if ALL inputs are 1
- Y pulls high if ANY input is 0

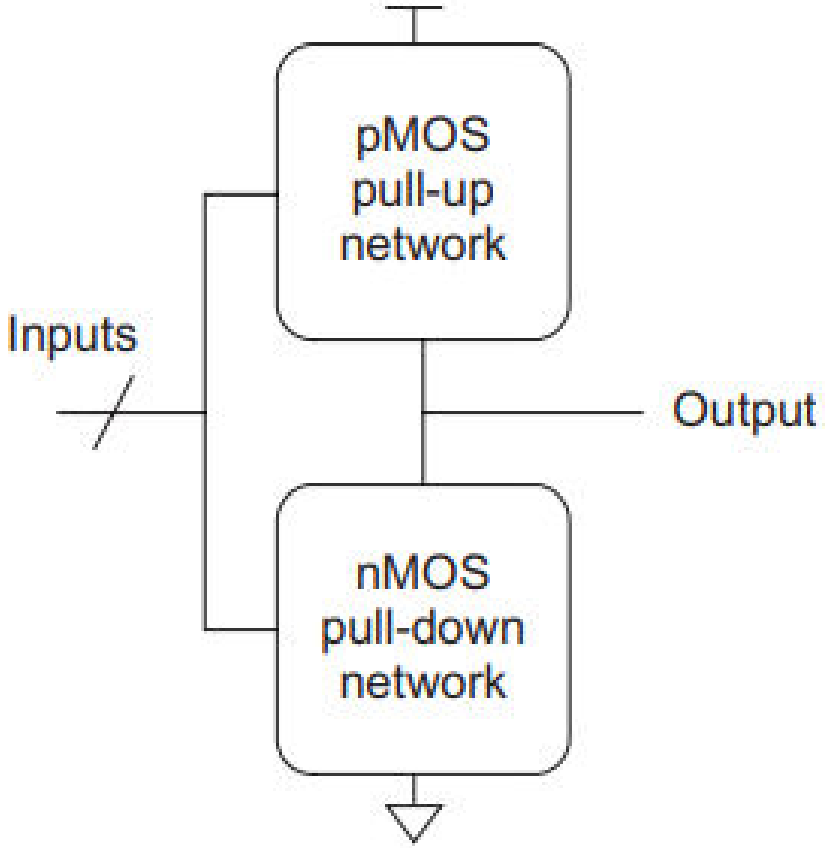
CMOS Logic Gates

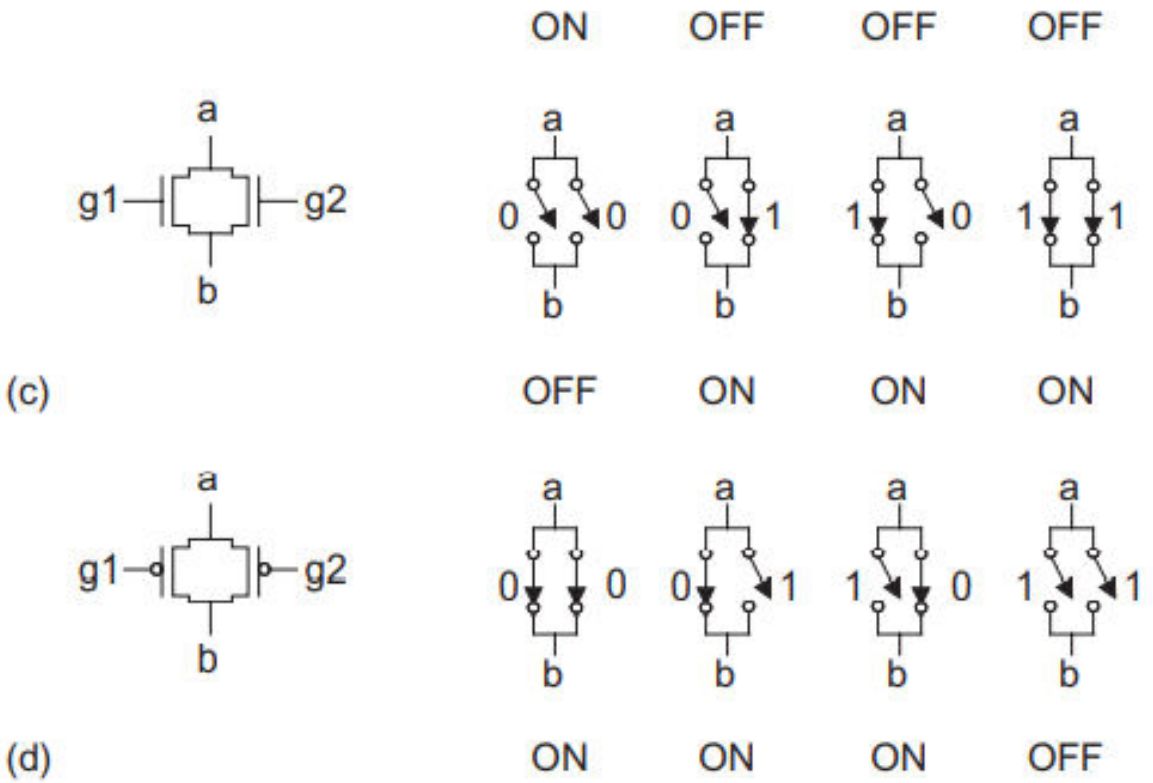




Connection behavior of Series and Parallel Transistors

CMOS Logic Gates

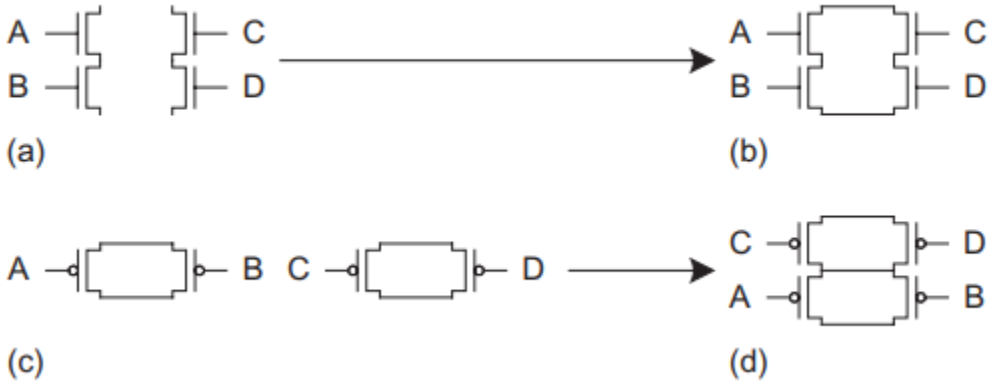


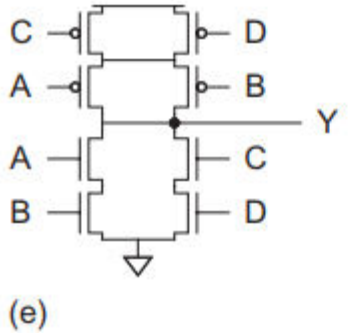


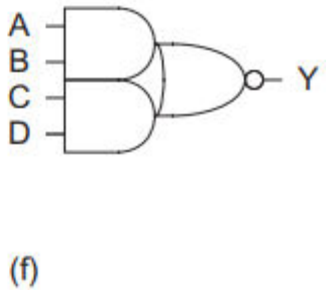
Connection behavior of Series and Parallel Transistors

Compound Gates

- Steps to build CMOS Circuit for Complex Expressions
  - A. Build nMOS Network from AOI or SOP Expression
    - a) And is implemented by series connections
    - b) OR s implemented by parallel connections
  - B. Build pMOS Network by applying DeMorgan's Principle to nMOS







CMOS compound gate for function $Y = \overline{(A.B) + (C.D)}$

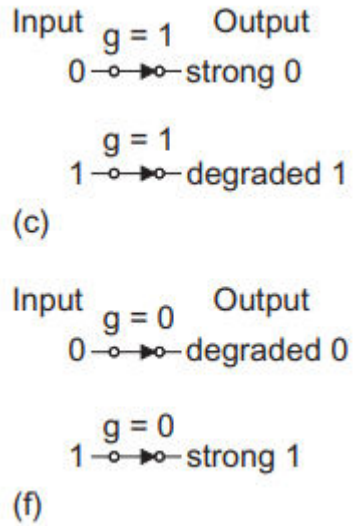
Exercise

- Sketch the static gate for the expression: $Y = \overline{(A + B + C).D}$

Solution

Pass Transistor

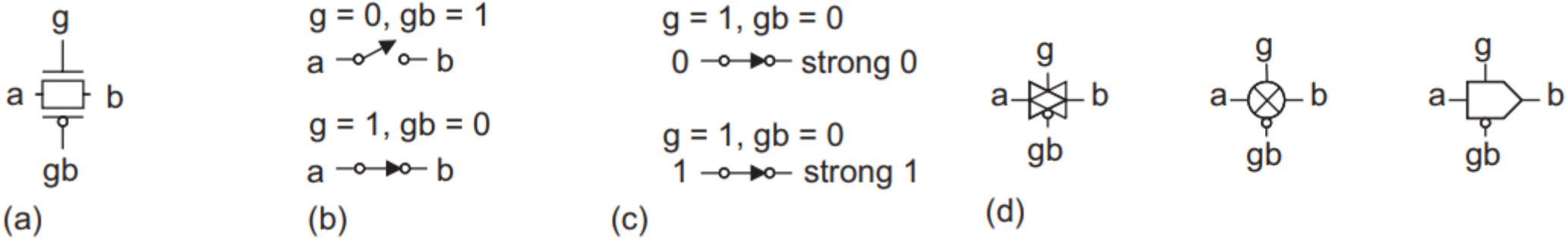
- Strength of a signal is measured by how closely it approximates an ideal voltage source.
- Stronger a signal, the more current it can source or sink.
- The power supplies, or rails, (VDD and GND) are the source of the strongest 1s and 0s.
- An nMOS transistor
  - perfect switch when passing a 0
  - imperfect at passing a 1
- A pMOS transistor
  - perfect switch when passing a 1
  - imperfect at passing a 0



"When an nMOS or pMOS is used alone as an imperfect switch, we call it a pass transistor."

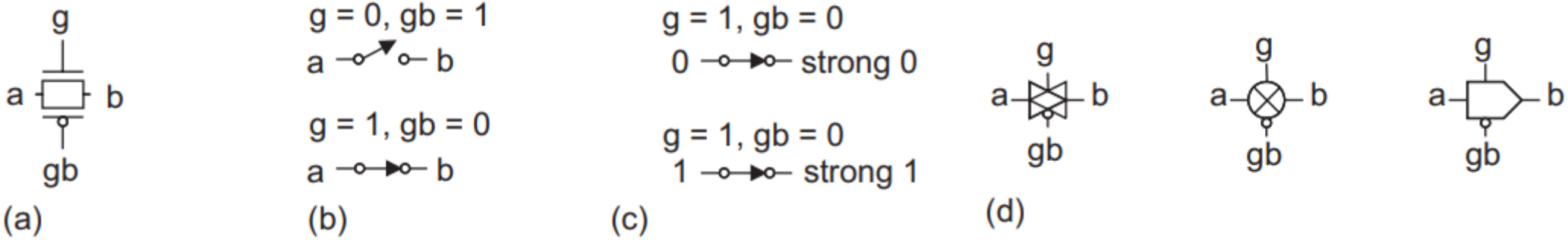
Transmission Gates

- By combining an nMOS and a pMOS transistor in parallel a switch when turned on passes both 0s and 1s in an acceptable fashion.
- This a transmission gate or pass gate.



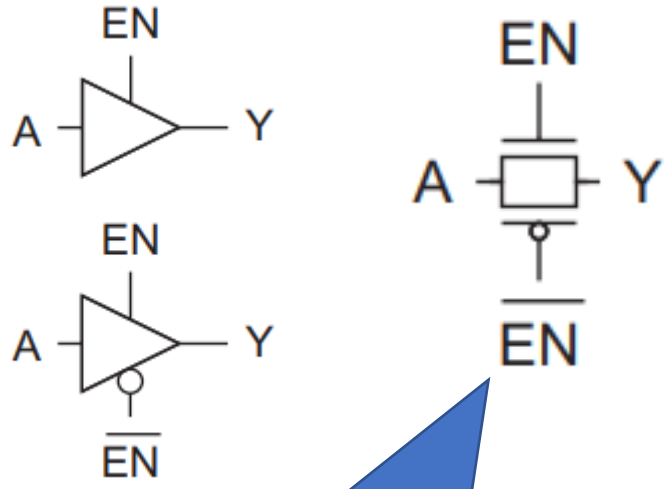
Transmission Gates

- Control and its complement are required to drive TG. (*Double Rail* Logic)
- So output is always strongly driven and the levels are never degraded. This is called a fully restored logic gate



Tristate Circuits – Tristate Buffer

EN / $\overline{EN}$	A	Y
0 / 1	0	Z
0 / 1	1	Z
1 / 0	0	0
1 / 0	1	1



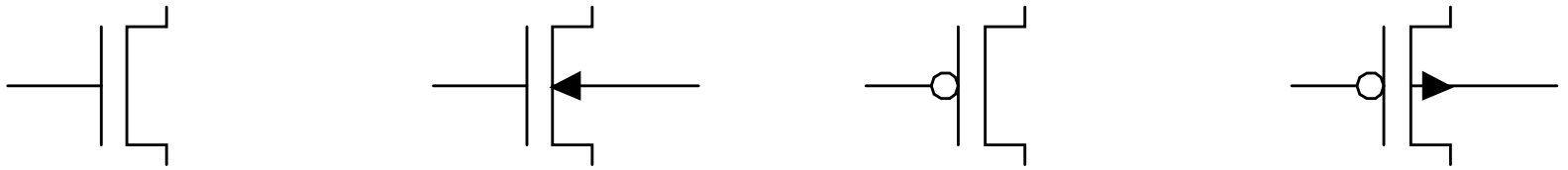
Practical Tristate with ‘non-restoring’ behavior..!!!

MOS Transistor Theory

MOS Transistors' Working and Characteristics

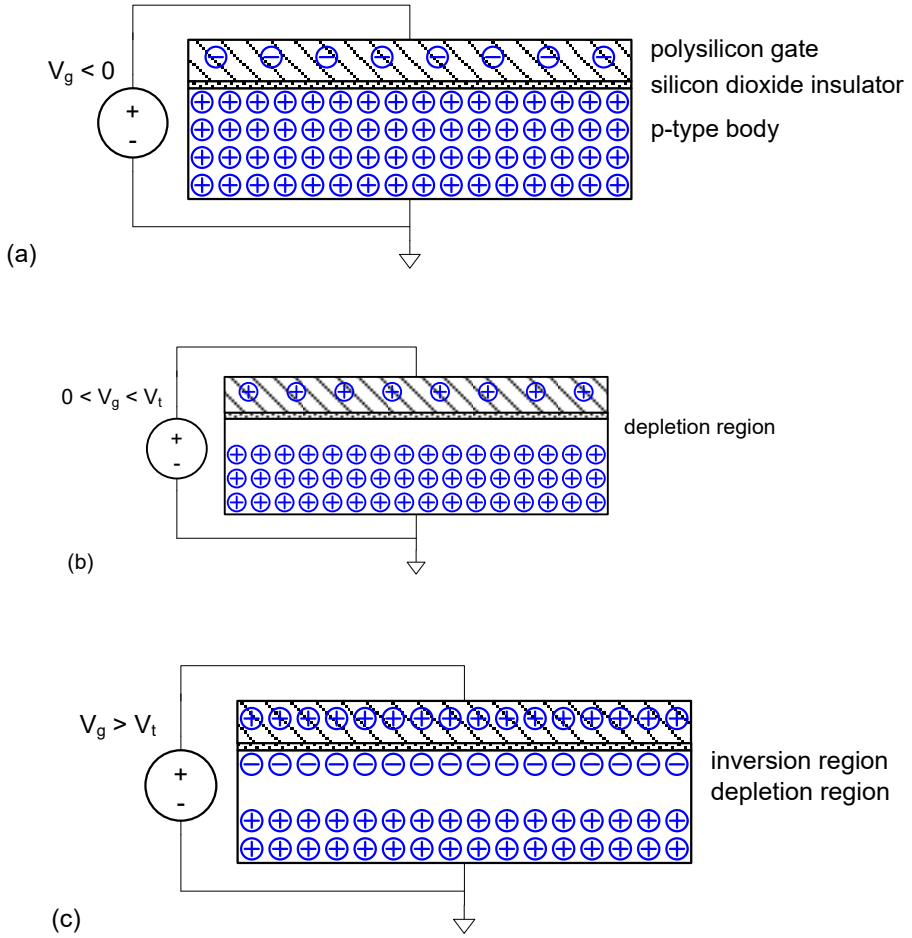
Introduction

- So far, we have treated transistors as ideal switches
- An ON transistor passes a finite amount of current
  - Depends on terminal voltages
  - Derive current-voltage (I-V) relationships
- Transistor gate, source, drain all have capacitance
  - $I = C (\Delta V/\Delta t) \rightarrow \Delta t = (C/I) \Delta V$
  - Capacitance and current determine speed



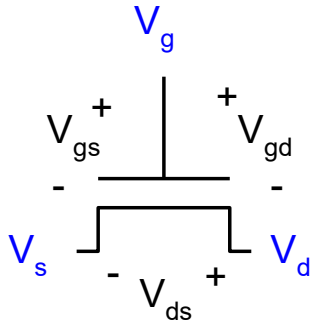
MOS Capacitor

- Gate and body form MOS capacitor
- Operating modes
  - Accumulation
  - Depletion
  - Inversion



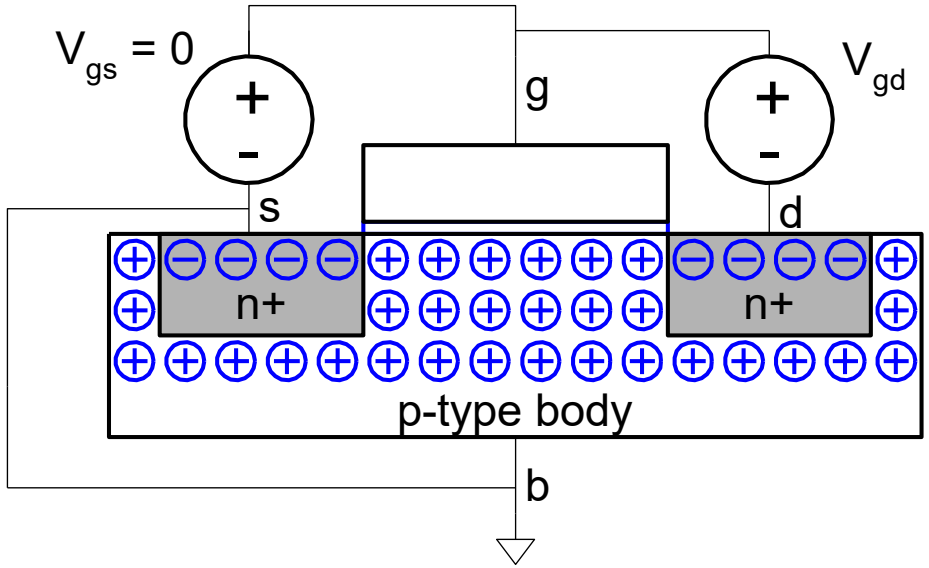
Terminal Voltages

- Mode of operation depends on V_g, V_d, V_s
  - $V_{gs} = V_g - V_s$
  - $V_{gd} = V_g - V_d$
  - $V_{ds} = V_d - V_s = V_{gs} - V_{gd}$
- Source and drain are symmetric diffusion terminals
  - By convention, source is terminal at lower voltage
  - Hence $V_{ds} \geq 0$
- nMOS body is grounded. First assume source is 0 too.
- Three regions of operation
  - *Cutoff*
  - *Linear*
  - *Saturation*



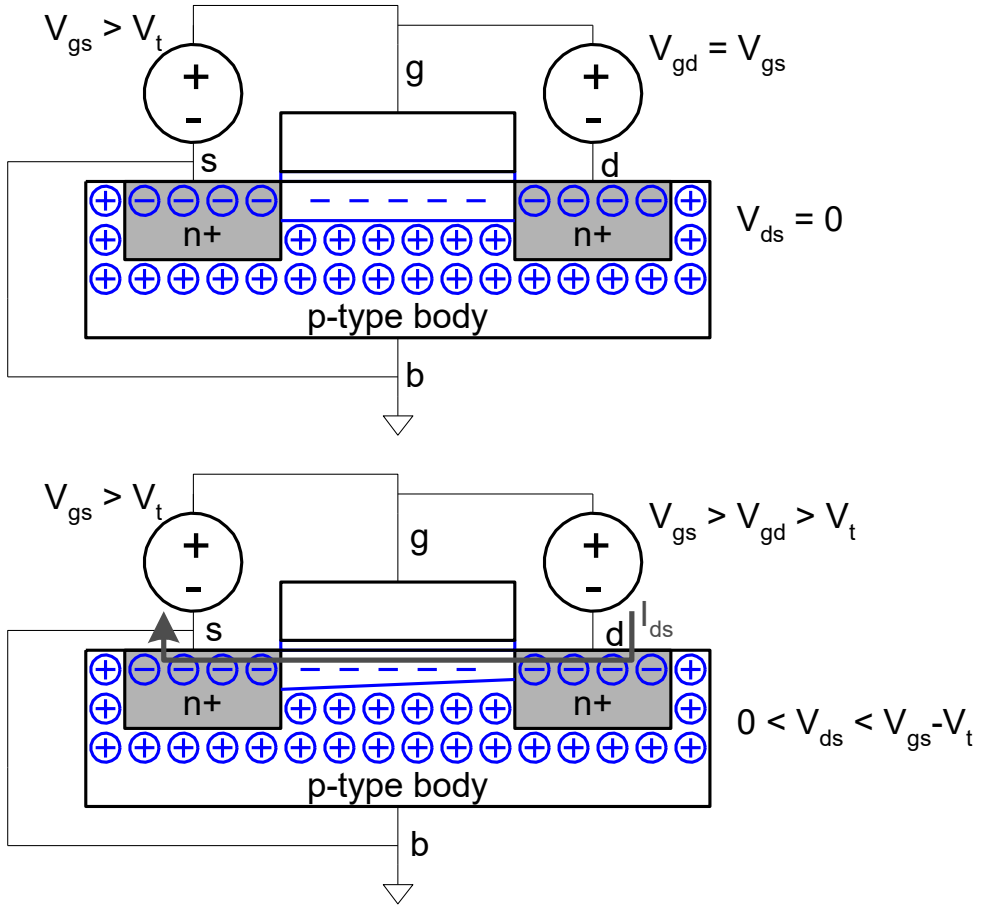
nMOS Cutoff

- No channel
- $I_{ds} \approx 0$



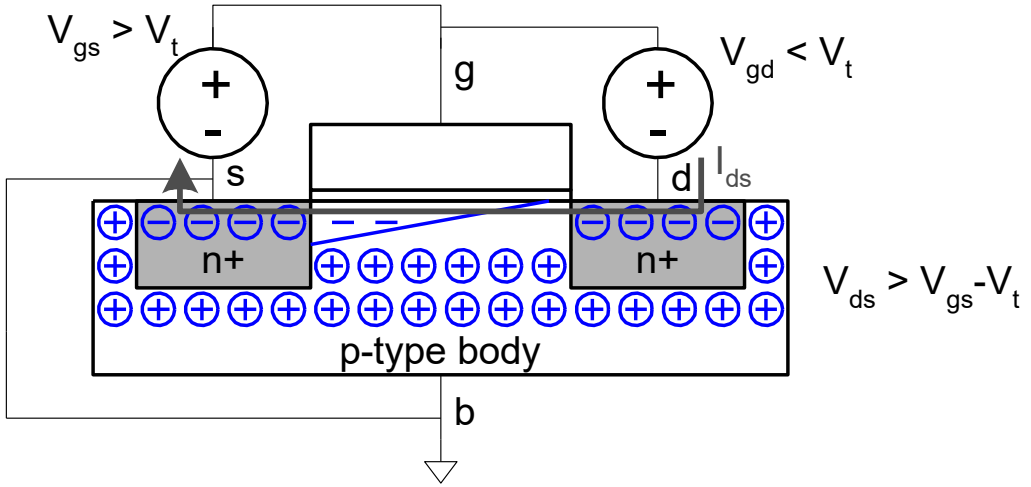
nMOS Linear

- Channel forms
- Current flows from d to s
  - e^- from s to d
- I_{ds} increases with V_{ds}
- Similar to linear resistor



nMOS Saturation

- Channel pinches off
- I_{ds} independent of V_{ds}
- We say current *saturates*
- Similar to current source



Ideal I-V Characteristics

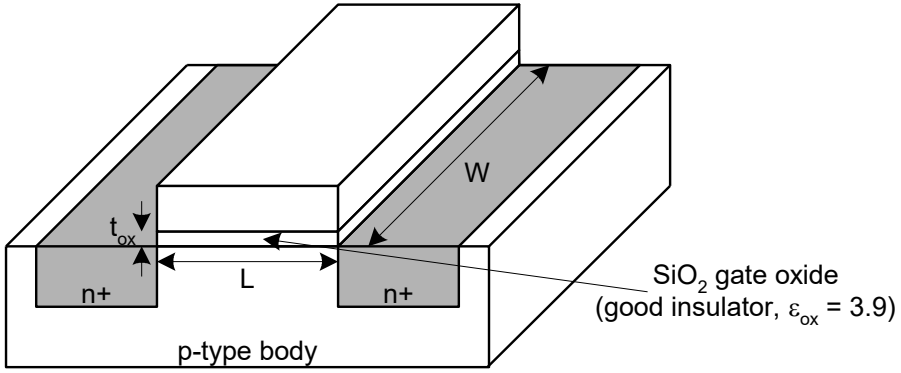
MOS Transistors' Working and Characteristics

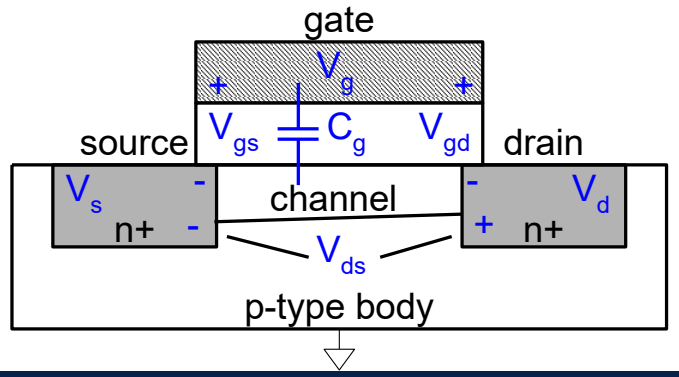
I-V Characteristics

- In Linear region, I_{ds} depends on
  - How much charge is in the channel?
  - How fast is the charge moving?

Channel Charge

- MOS structure looks like parallel plate capacitor while operating in inversions
  - Gate – oxide – channel
- $Q_{channel} = CV$
- $C = C_g = \varepsilon_{ox}WL/t_{ox} = C_{ox}WL$ where $C_{ox} = e_{ox} / t_{ox}$
- $V = V_{gc} - V_t = (V_{gs} - V_{ds}/2) - V_t$





Carrier velocity

- Charge is carried by e-
- Electrons are propelled by the lateral electric field between source and drain
  - $E = V_{ds}/L$
- Carrier velocity *v* proportional to lateral E-field
  - $v = \mu E$ μ called mobility
- Time for carrier to cross channel:
  - $t = L / v$

nMOS Linear I-V

- Now we know
  - How much charge $Q_{channel}$ is in the channel
  - How much time *t* each carrier takes to cross

$$I_{ds} = \frac{Q_{\text{channel}}}{t}$$

$$= \mu C_{\text{ox}} \frac{W}{L}\left(V_{gs} - V_t - V_{ds}/2\right)V_{ds}$$

$$= \beta\left(V_{gs} - V_t - V_{ds}/2\right)V_{ds} \qquad \beta = \mu C_{\text{ox}} \frac{W}{L}$$

nMOS Saturation I-V

- If $V_{gd} < V_t$, channel pinches off near drain
  - When $V_{ds} > V_{dsat} = V_{gs} - V_t$
- Now drain voltage no longer increases current

$$I_{ds} = \beta\left(V_{gs} - V_t - {V_{dsat}}/{2}\right)V_{dsat}$$

$$= \frac{\beta}{2}\left(V_{gs} - V_t\right)^2$$

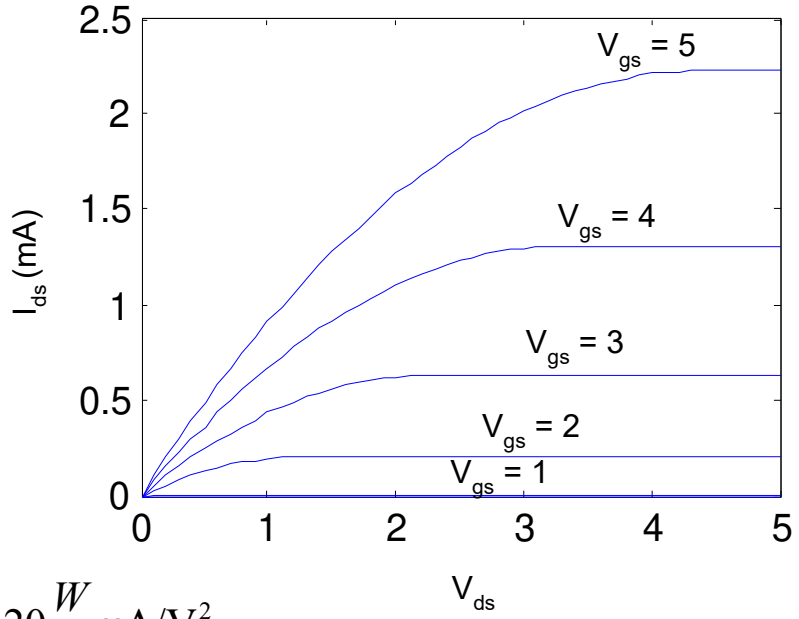
nMOS I-V Summary

- *Shockley* 1st order transistor models

$$I_{ds} = \begin{cases} 0 & V_{gs} < V_t \quad \text{cutoff} \\ \beta\left(V_{gs} - V_t - V_{ds}/2\right)V_{ds} & V_{ds} < V_{dsat} \quad \text{linear} \\ \frac{\beta}{2}\left(V_{gs} - V_t\right)^2 & V_{ds} > V_{dsat} \quad \text{saturation} \end{cases}$$

Example

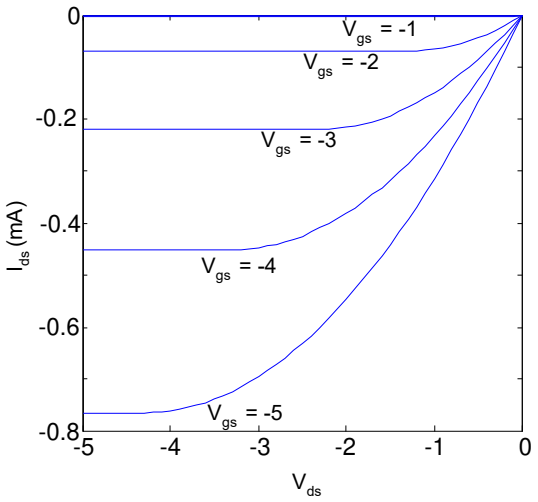
- We will be using a 0.6 μm process for your project
  - From AMI Semiconductor
  - t_{ox} = 100 Å
  - μ = 350 $cm^2/V*s$
  - V_t = 0.7 V
- Plot I_{ds} vs. V_{ds}
  - V_{gs} = 0, 1, 2, 3, 4, 5
  - Use W/L = 4/2 λ



$$\beta = \mu C_{ox}\frac{W}{L} = (350)\left(\frac{3.9\times 8.85\cdot 10^{-14}}{100\cdot 10^{-8}}\right)\left(\frac{W}{L}\right) = 120\frac{W}{L}\,\mu A/V^2$$

pMOS I-V

- All dopings and voltages are inverted for pMOS
  - Source is the more positive terminal
- Mobility μ_p is determined by holes
  - Typically 2-3x lower than that of electrons μ_n
  - 120 $cm^2/V \bullet s$ in AMI 0.6 μm process
- Thus pMOS must be wider to provide same current
  - In this class, assume $\mu_n / \mu_p = 2$



Non-ideal I-V Effects

MOS Transistors' Working and Characteristics

Mobility Degradation

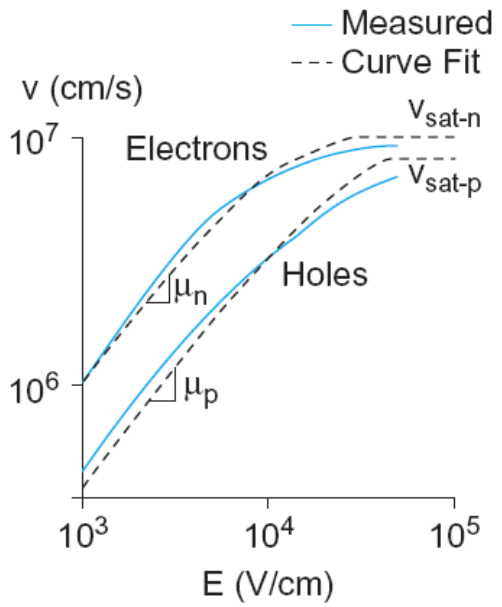
- High E_{vert} effectively reduces mobility
  - Collisions with oxide interface

$$\mu_{\text{eff}-n} = \frac{540\,\frac{\text{cm}^2}{\text{V}\cdot\text{s}}}{1+\left(\frac{V_{gs}+V_t}{0.54\,\frac{\text{V}}{\text{nm}}\,t_{\text{ox}}}\right)^{1.85}} \qquad \mu_{\text{eff}-p} = \frac{185\,\frac{\text{cm}^2}{\text{V}\cdot\text{s}}}{1+\frac{\left|V_{gs}+1.5V_t\right|}{0.338\,\frac{\text{V}}{\text{nm}}\,t_{\text{ox}}}}$$

Velocity Saturation

- At high E_{lat}, carrier velocity rolls off
  - Carriers scatter off atoms in silicon lattice
  - Velocity reaches v_{sat}
    - Electrons: 10^7 cm/s
    - Holes: 8 x 10^6 cm/s
  - Better model

$$v = \begin{cases} \dfrac{\mu_{eff} E}{1 + \dfrac{E}{E_c}} & E < E_c \\ v_{sat} & E \geq E_c \end{cases} \qquad E_c = \frac{2 v_{sat}}{\mu_{eff}}$$



Vel Sat I-V Effects

- Ideal transistor ON current increases with V_{DD}^2

$$I_{ds} = \mu C_{ox} \frac{W}{L} \frac{(V_{gs} - V_t)^2}{2} = \frac{\beta}{2}(V_{gs} - V_t)^2$$

- Velocity-saturated ON current increases with V_{DD}

$$I_{ds} = C_{ox} W (V_{gs} - V_t) v_{max}$$

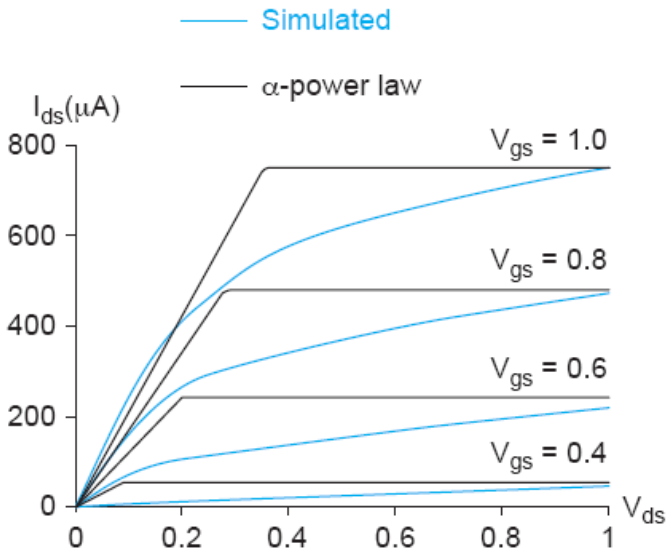
- Real transistors are partially velocity saturated
  - Approximate with α-power law model
  - $I_{ds} \propto V_{DD}^{\alpha}$
  - $1 < \alpha < 2$ determined empirically (≈ 1.3 for 65 nm)

α-Power Model

$$I_{ds} = \begin{cases} 0 & V_{gs} < V_t \quad \text{cutoff} \\ I_{dsat}\dfrac{V_{ds}}{V_{dsat}} & V_{ds} < V_{dsat} \quad \text{linear} \\ I_{dsat} & V_{ds} > V_{dsat} \quad \text{saturation} \end{cases}$$

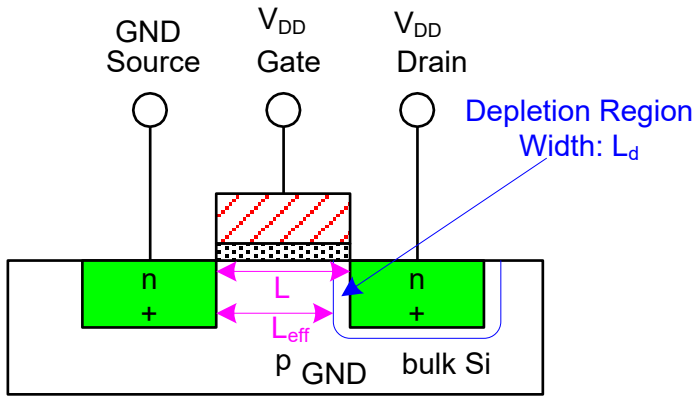
$$I_{dsat} = P_c \frac{\beta}{2}\left(V_{gs} - V_t\right)^{\alpha}$$

$$V_{dsat} = P_v \left(V_{gs} - V_t\right)^{\alpha/2}$$



Channel Length Modulation

- Reverse-biased p-n junctions form a *depletion region*
  - Region between n and p with no carriers
  - Width of depletion L_d region grows with reverse bias
  - $L_{eff} = L - L_d$
- Shorter L_{eff} gives more current
  - I_{ds} increases with V_{ds}
  - Even in saturation



Chan Length Mod I-V

$$I_{ds} = \frac{\beta}{2}\left(V_{gs} - V_t\right)^2\left(1 + \lambda V_{ds}\right)$$

- λ = *channel length modulation coefficient*
  - not feature size
  - Empirically fit to I-V characteristics

Threshold Voltage Effects

- V_t is V_{gs} for which the channel starts to invert
- Ideal models assumed V_t is constant
- Really depends (weakly) on almost everything else:
  - Body voltage: *Body Effect*
  - Drain voltage: *Drain-Induced Barrier Lowering*
  - Channel length: *Short Channel Effect*

Body Effect

$$V_t = V_{t0} + \gamma\left(\sqrt{\phi_s + V_{sb}} - \sqrt{\phi_s}\right)$$

- Body is a fourth transistor terminal
- V_{sb} affects the charge required to invert the channel
  - Increasing V_s or decreasing V_b increases V_t

- ϕ_s = *surface potential* at threshold

$$\phi_s = 2v_T \ln\frac{N_A}{n_i}$$

  - Depends on doping level N_A
  - And intrinsic carrier concentration n_i
- γ = *body effect coefficient*

$$\gamma = \frac{t_{ox}}{\varepsilon_{ox}}\sqrt{2q\varepsilon_{si}N_A} = \frac{\sqrt{2q\varepsilon_{si}N_A}}{C_{ox}}$$

Body Effect Cont.

- For small source-to-body voltage, treat as linear

$$V_t = V_{t0} + k_\gamma V_{sb}$$

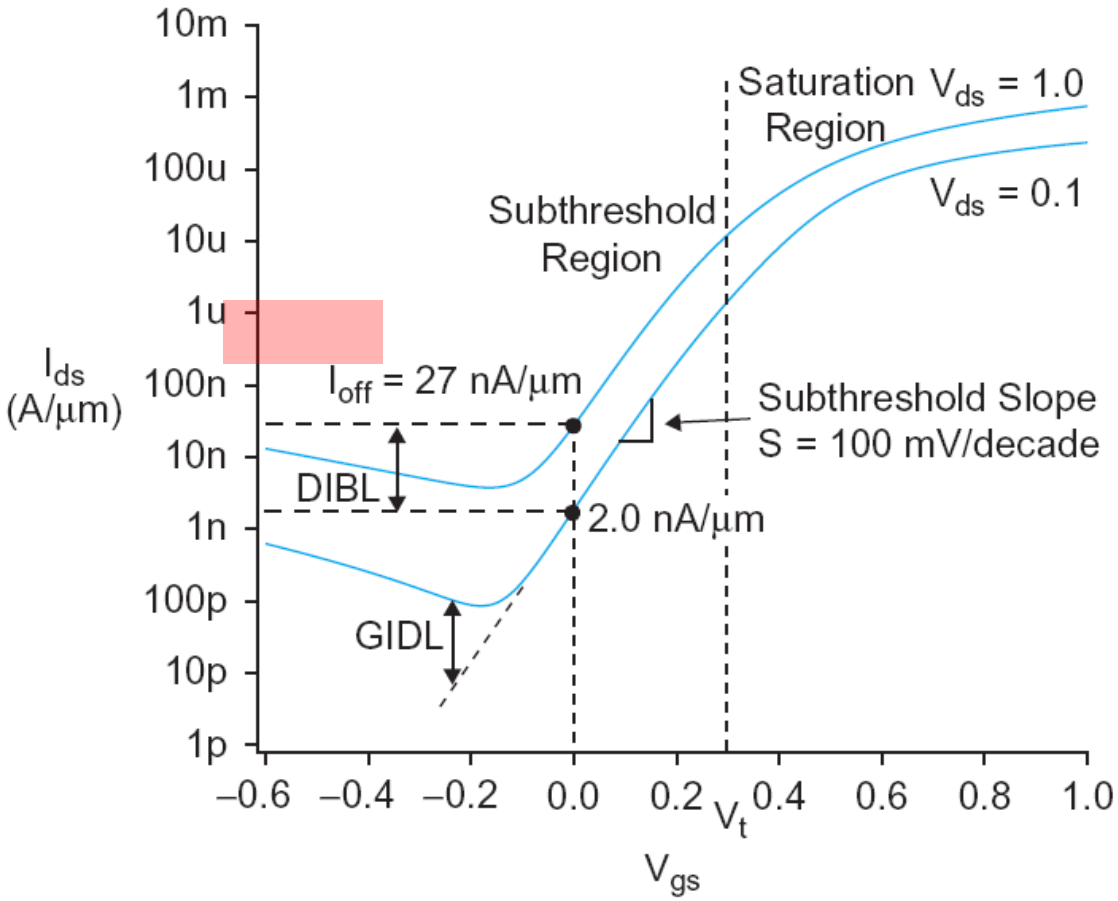
$$k_\gamma = \frac{\gamma}{2\sqrt{\phi_s}} = \frac{\sqrt{\frac{q\varepsilon_{si}N_A}{v_T \ln\frac{N_A}{n_i}}}}{2C_{ox}}$$

DIBL

- Electric field from drain affects channel
- More pronounced in small transistors where the drain is closer to the channel
- Drain-Induced Barrier Lowering
  - Drain voltage also affect V_t

$$V_t' = V_t - \eta V_{ds}$$

- High drain voltage causes current to increase.

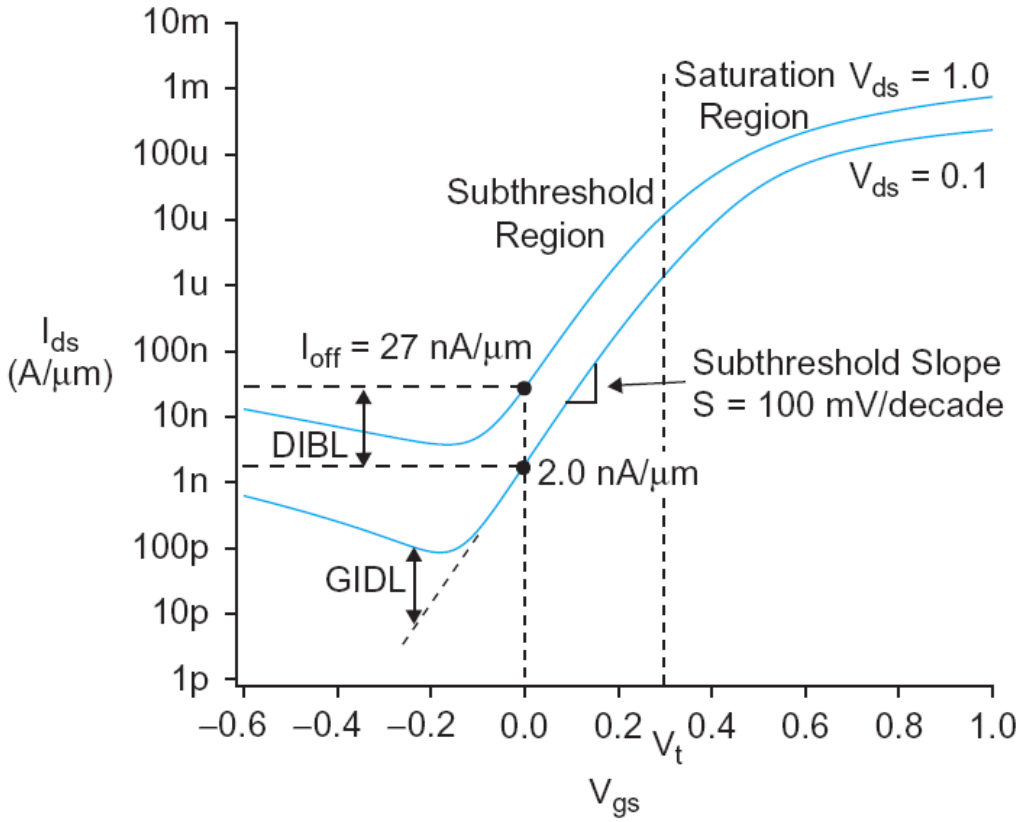


Short Channel Effect

- In small transistors, source/drain depletion regions extend into the channel
  - Impacts the amount of charge required to invert the channel
  - And thus makes V_t a function of channel length
- Short channel effect: V_t increases with L
  - Some processes exhibit a reverse short channel effect in which V_t decreases with L

Leakage

- What about current in cutoff?
- Simulated results
- What differs?
  - Current doe
    go to 0 in cutoff



Leakage Sources

- Subthreshold conduction
  - Transistors can't abruptly turn ON or OFF
  - Dominant source in contemporary transistors
- Gate leakage
  - Tunneling through ultrathin gate dielectric
- Junction leakage
  - Reverse-biased PN junction diode current

Subthreshold Leakage

- Subthreshold leakage exponential with V_{gs}

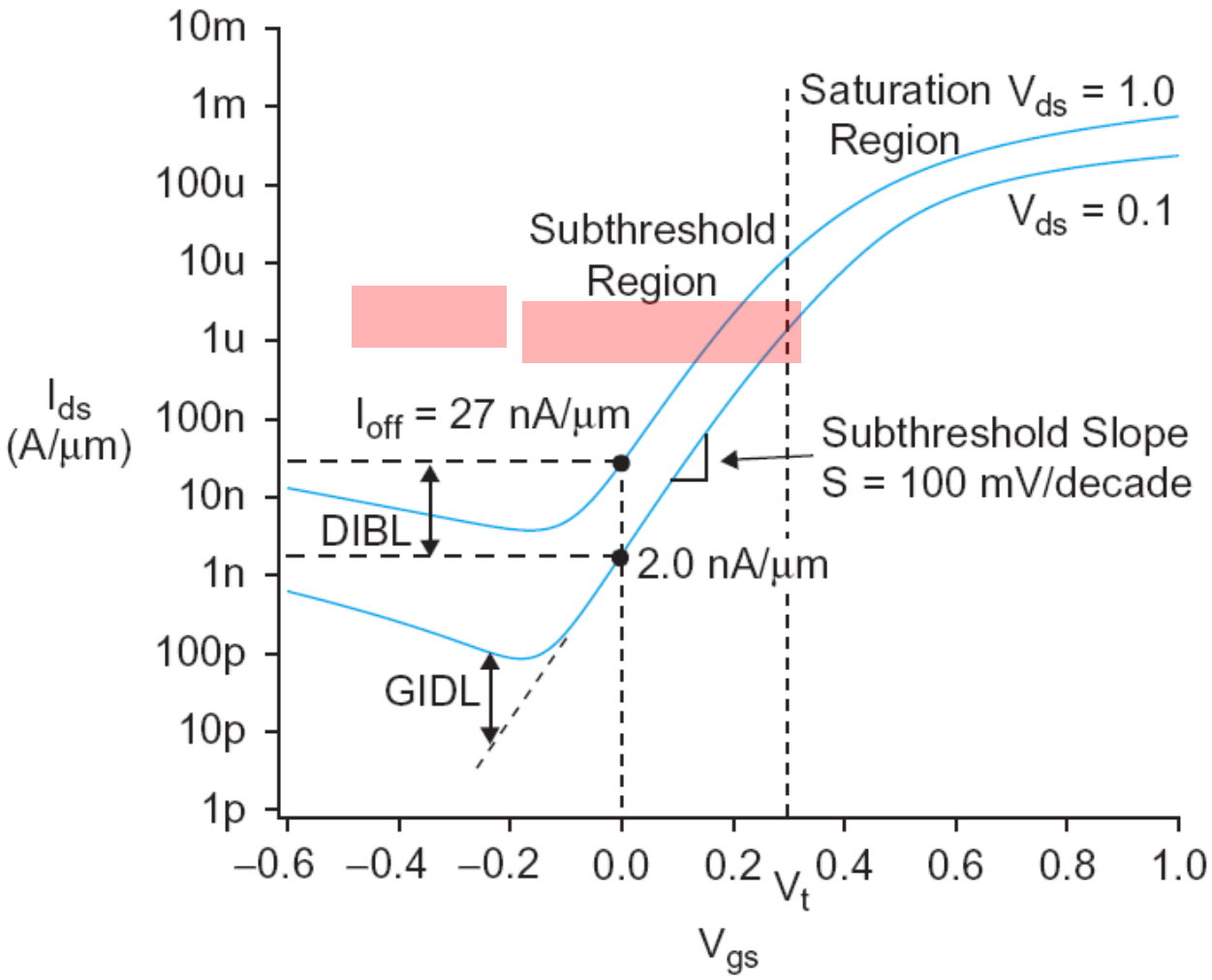
$$I_{ds} = I_{ds0} e^{\frac{V_{gs} - V_{t0} + \eta V_{ds} - k_\gamma V_{sb}}{n v_T}} \left(1 - e^{\frac{-V_{ds}}{v_T}}\right)$$

- n is process dependent
  - typically 1.3-1.7
- Rewrite relative to I_{off} on log scale

$$I_{ds} = I_{off} 10^{\frac{V_{gs} + \eta(V_{ds} - V_{dd}) - k\gamma V_{sb}}{S}} \left(1 - e^{\frac{-V_{ds}}{v_t}}\right)$$

$$S = \left[\frac{d(\log_{10} I_{ds})}{dV_{gs}}\right]^{-1} = n v_T \ln 10$$

- S ≈ 100 mV/decade @ room temperature

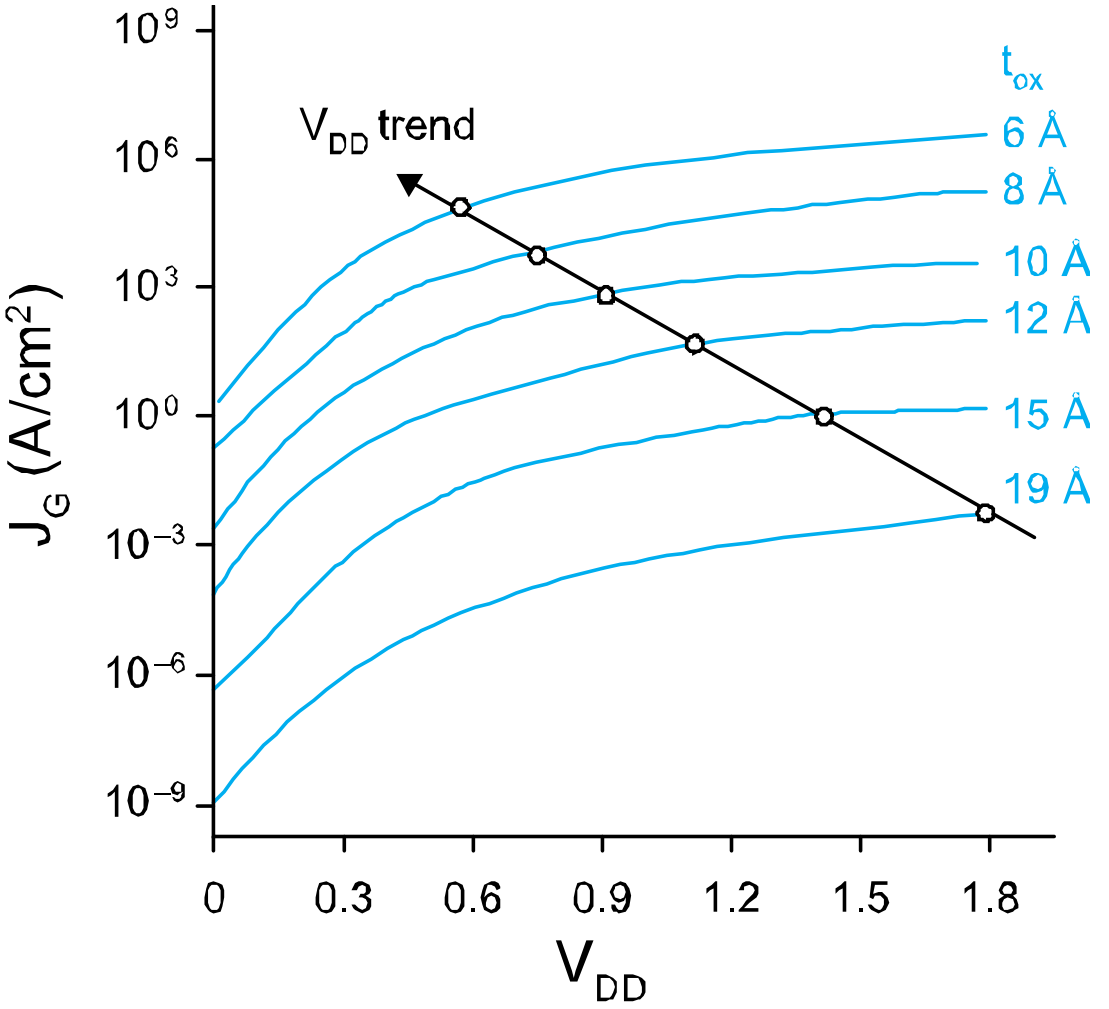


Gate Leakage

- Carriers tunnel thorough very thin gate oxides
- Exponentially sensitive to t_{ox} and V_{DD}

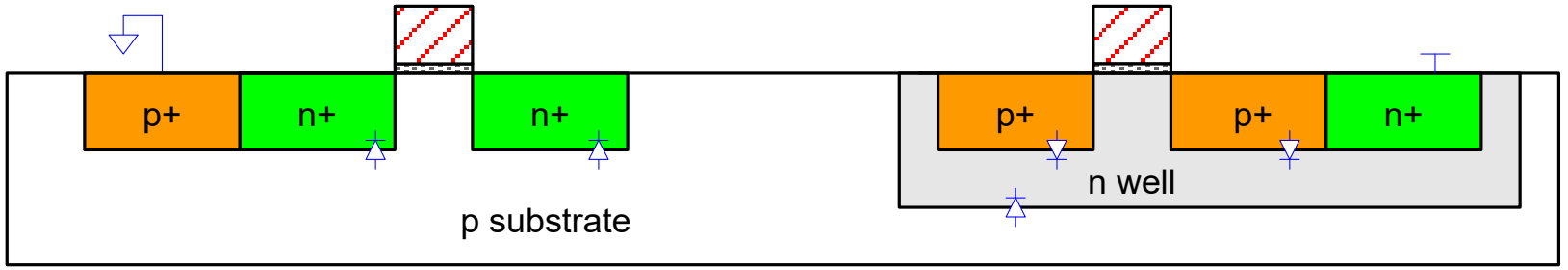
$$I_{gate} = WA\left(\frac{V_{DD}}{t_{ox}}\right)^2 e^{-B\frac{t_{ox}}{V_{DD}}}$$

  - A and B are tech constants
  - Greater for electrons
    - So nMOS gates leak more
- Negligible for older processes (t_{ox} > 20 Å)
- Critically important at 65 nm and below (t_{ox} ≈ 10.5 Å)



Junction Leakage

- Reverse-biased p-n junctions have some leakage
  - Ordinary diode leakage
  - Band-to-band tunneling (BTBT)
  - Gate-induced drain leakage (GIDL)



Diode Leakage

- Reverse-biased p-n junctions have some leakage

$$I_D = I_S\left(e^{\frac{V_D}{v_T}} - 1\right)$$

- At any significant negative diode voltage, $I_D = -I_s$
- I_s depends on doping levels
  - And area and perimeter of diffusion regions
  - Typically < 1 fA/μm^2 (negligible)

Band-to-Band Tunneling

- Tunneling across heavily doped p-n junctions
  - Especially sidewall between drain & channel when *halo doping* is used to increase V_t
- Increases junction leakage to significant levels

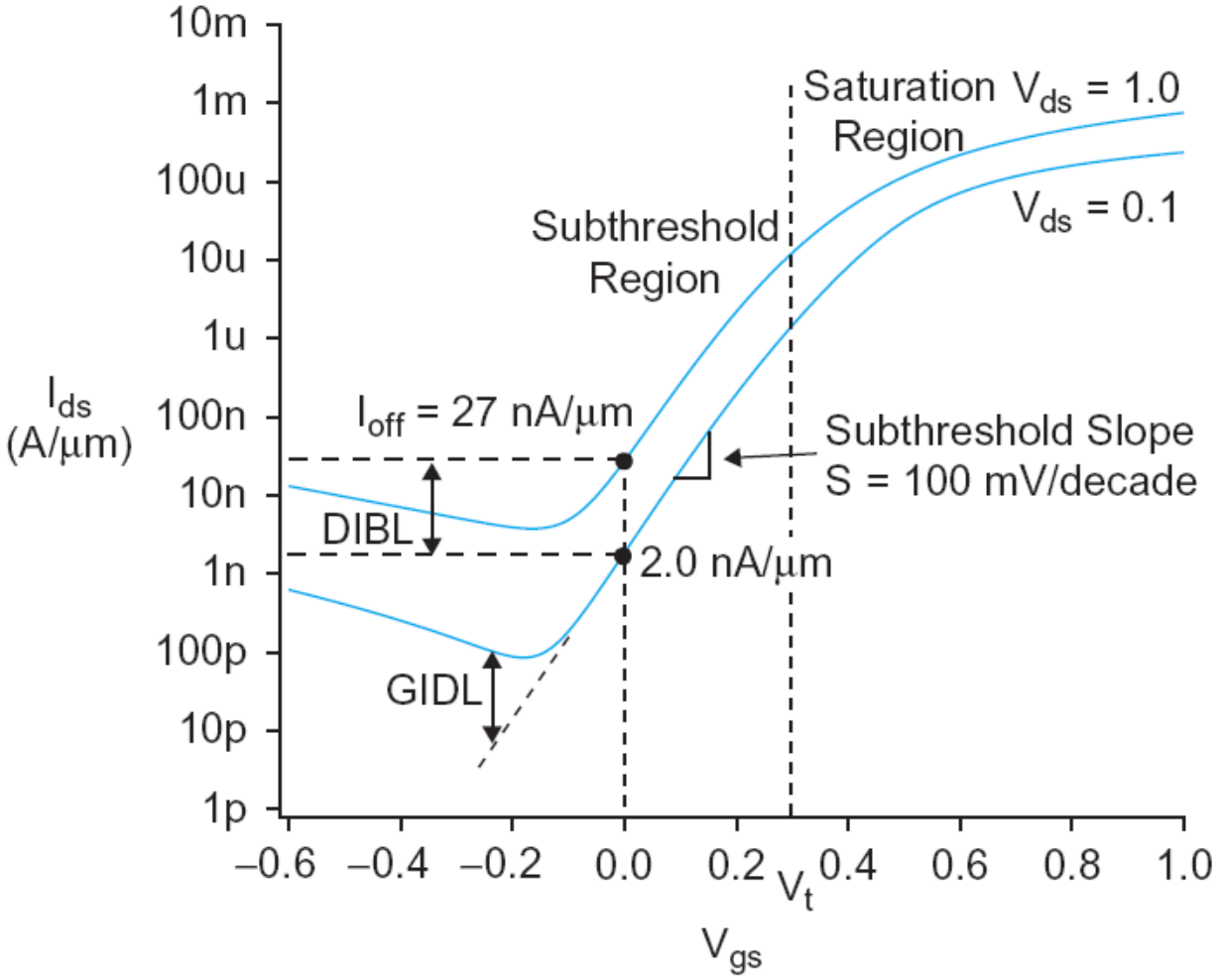
$$I_{BTBT} = WX_j A \frac{E_j}{E_g^{0.5}} V_{dd} \, e^{-B\frac{E_g^{1.5}}{E_j}}$$

$$E_j = \sqrt{\frac{2qN_{halo}N_{sd}}{\varepsilon\left(N_{halo}+N_{sd}\right)}}\left(V_{DD} + v_T \ln\frac{N_{halo}N_{sd}}{n_i^2}\right)$$

  - X_j: sidewall junction depth
  - E_g: bandgap voltage
  - A, B: tech constants

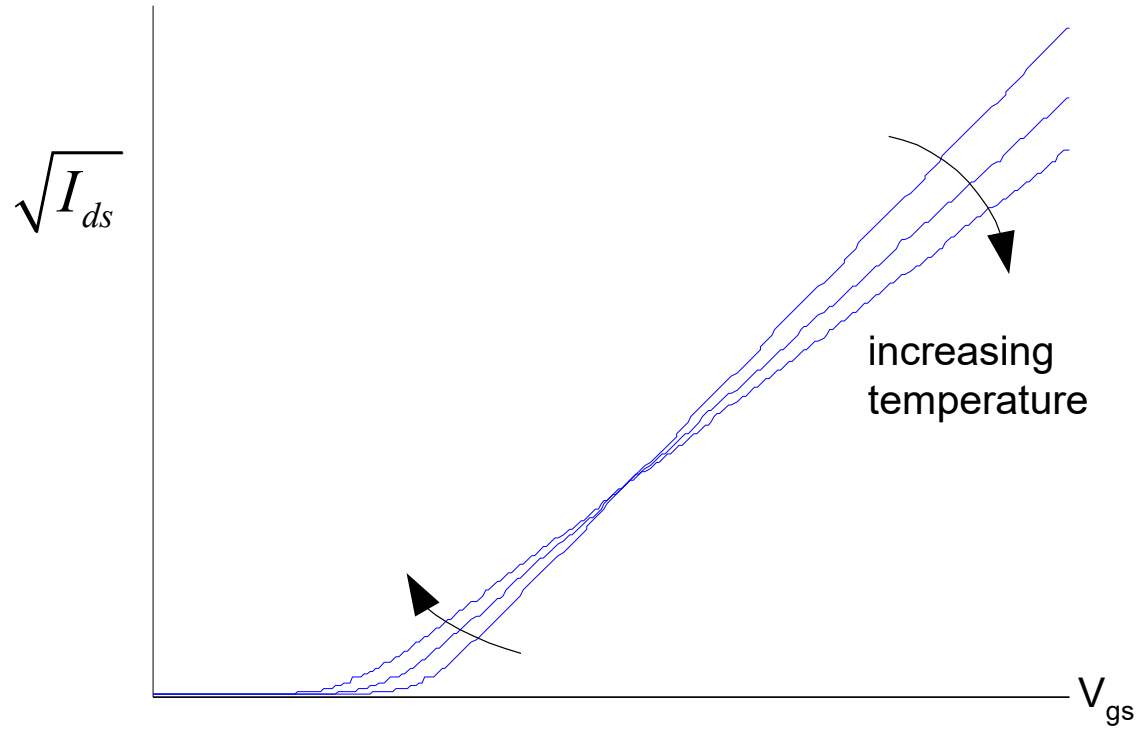
Gate-Induced Drain Leakage

- Occurs at overlap between gate and drain
  - Most pronounced when drain is at VDD, gate is at a negative voltage
  - Thwarts efforts to reduce subthreshold leakage using a negative gate voltage



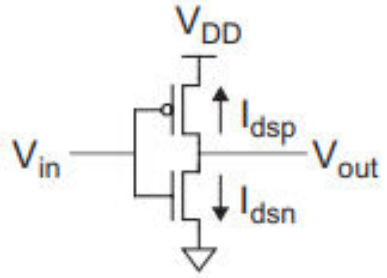
Temperature Sensitivity

- Increasing temperature
  - Reduces mobility
  - Reduces V_t
- I_{ON} decreases with temperature
- I_{OFF} increases with temperature



DC Transfer Characteristics

Static CMOS Inverter DC Characteristics



	Cutoff	Linear	Saturated
nMOS	$V_{gsn} < V_{tn}$	$V_{gsn} > V_{tn}$	$V_{gsn} > V_{tn}$
	$V_{in} < V_{tn}$	$V_{in} > V_{tn}$	$V_{in} > V_{tn}$
		$V_{dsn} < V_{gsn} - V_{tn}$	$V_{dsn} > V_{gsn} - V_{tn}$
		$V_{out} < V_{in} - V_{tn}$	$V_{out} > V_{in} - V_{tn}$
pMOS	$V_{gsp} > V_{tp}$	$V_{gsp} < V_{tp}$	$V_{gsp} < V_{tp}$
	$V_{in} > V_{tp} + V_{DD}$	$V_{in} < V_{tp} + V_{DD}$	$V_{in} < V_{tp} + V_{DD}$
		$V_{dsp} > V_{gsp} - V_{tp}$	$V_{dsp} < V_{gsp} - V_{tp}$
		$V_{out} > V_{in} - V_{tp}$	$V_{out} < V_{in} - V_{tp}$

- V_{tn} - threshold voltage nMOS
- V_{tp} - threshold voltage pMOS

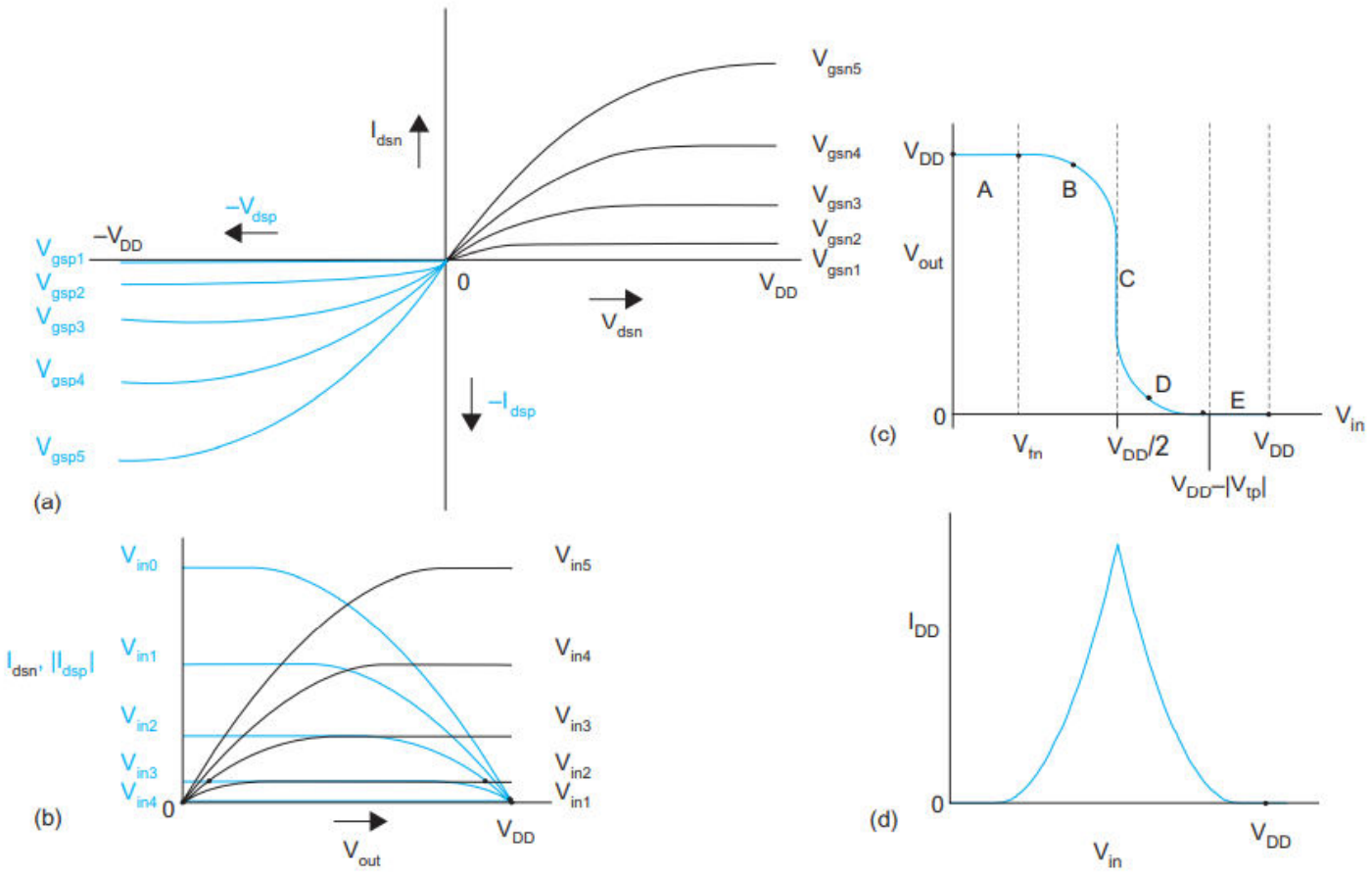
(V_{tp} is negative)

- Equations -in terms of V_{gs}/V_{ds} and Vin /Vout.
- Source of the nMOS transistor is grounded,

$V_{gsn} = V_{in}$ and $V_{dsn} = V_{out}$

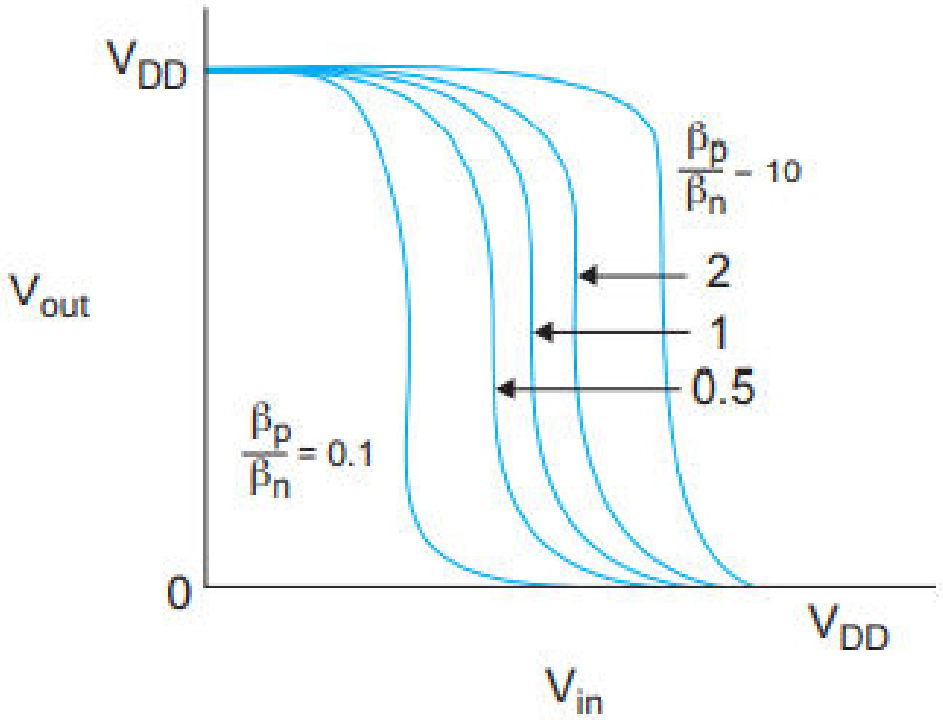
- As the source of the pMOS transistor is tied to VDD, Vgsp = Vin – VDD and Vdsp = Vout – VDD

Static CMOS Inverter DC Characteristics



Region	Condition	p-device	n-device	Output
A	$0 \le V_{in} < V_{tn}$	linear	cutoff	$V_{out} = V_{DD}$
B	$V_{tn} \le V_{in} < V_{DD}/2$	linear	saturated	$V_{out} > V_{DD}/2$
C	$V_{in} = V_{DD}/2$	saturated	saturated	V_{out} drops sharply
D	$V_{DD}/2 < V_{in} \le V_{DD} - \|V_{tp}\|$	saturated	linear	$V_{out} < V_{DD}/2$
E	$V_{in} > V_{DD} - \|V_{tp}\|$	cutoff	linear	$V_{out} = 0$

Beta Ratio Effects



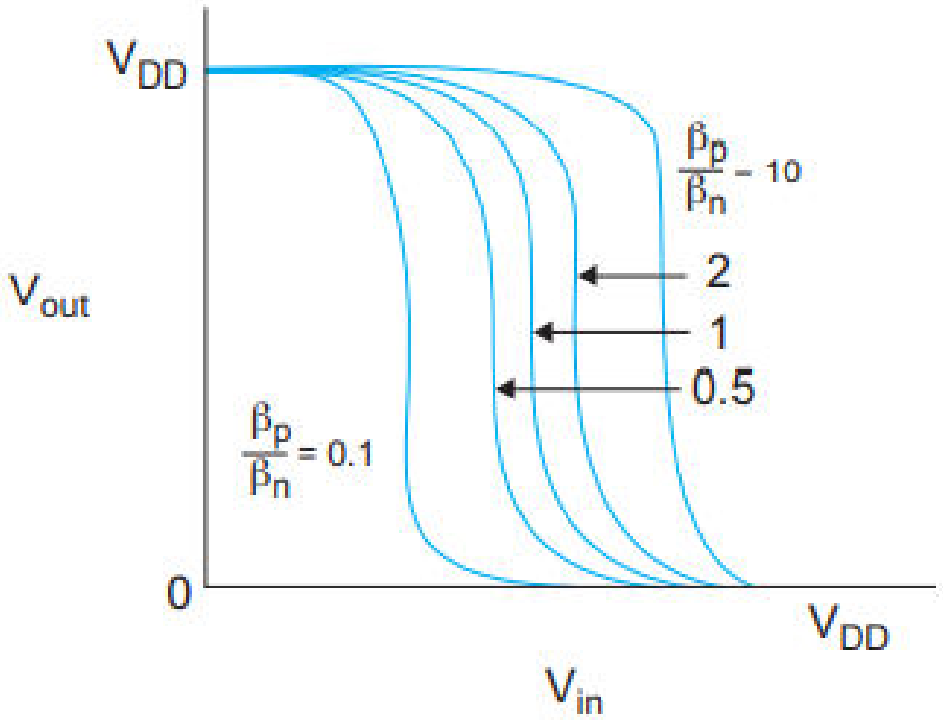
- Inverters with different beta ratios

$$r = \beta_p / \beta_n$$

are called skewed inverters.

- If r > 1, the inverter is HI-skewed.
- If r < 1, the inverter is LO-skewed.
- If r = 1, the inverter has normal skew or is unskewed.

Beta Ratio Effects



- HI-skew inverter - stronger pMOS transistor.
- Input is VDD /2
- Output greater VDD /2.
- Input threshold must be higher than an unskewed inverter.
- LO-skew inverter has a weaker pMOS transistor - Lower switching threshold.

Beta Ratio Effects

- The inverter threshold can also be computed analytically.

From the long-channel models of for saturated transistors:

$$I_{dn} = \frac{\beta_n}{2}\left(V_{\text{inv}} - V_{tn}\right)^2$$

$$I_{dp} = \frac{\beta_p}{2}\left(V_{\text{inv}} - V_{DD} - V_{tp}\right)^2$$

By setting the currents to be equal and opposite, we can solve for V_{inv} as a function of r:

$$V_{\text{inv}} = \frac{V_{DD} + V_{tp} + V_{tn}\sqrt{\frac{1}{r}}}{1+\sqrt{\frac{1}{r}}}$$

Beta Ratio Effects

- In the limit that the transistors are fully velocity saturated

$$I_{dn} = W_n C_{ox} v_{sat-n} (V_{inv} - V_{tn})$$
$$I_{dp} = W_p C_{ox} v_{sat-p} (V_{inv} - V_{DD} - V_{tp})$$

- Redefining $r = W_p v_{sat-p} / W_n v_{sat-n}$, the inverter threshold

$$V_{inv} = \frac{V_{DD} + V_{tp} + V_{tn}\frac{1}{r}}{1 + \frac{1}{r}}$$

- In either case, if $V_{tn} = -V_{tp}$ and r = 1, $V_{inv} = V_{DD}/2$ as expected.
- Velocity saturated inverters are more sensitive to skewing because their DC transfer characteristics are not as sharp.

Noise Margin

- Noise margin allows to determine the allowable noise voltage on the input of a gate so that the output will not be corrupted.
- Noise margin (or noise immunity) uses two parameters:
  - the LOW noise margin, NM_L
  - the HIGH noise margin, NM_H.
- NM_L is defined as difference in maximum LOW input voltage recognized by the receiving gate and the maximum LOW output voltage produced by the driving gate.

$$NM_L = V_{IL} - V_{OL}$$

Noise Margin

- The value of NMH is the difference between the minimum HIGH output voltage of the driving gate and the minimum HIGH input voltage recognized by the receiving gate. Thus,

$$NM_H = V_{OH} - V_{IH}$$

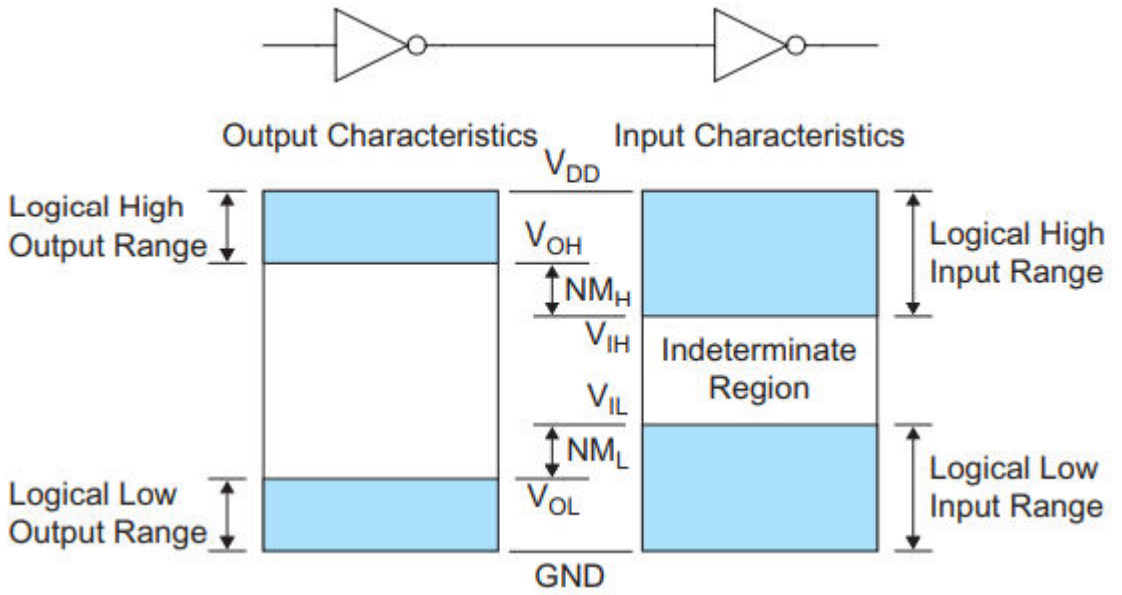
Where,

V_{IH} = minimum HIGH input voltage

V_{IL} = maximum LOW input voltage

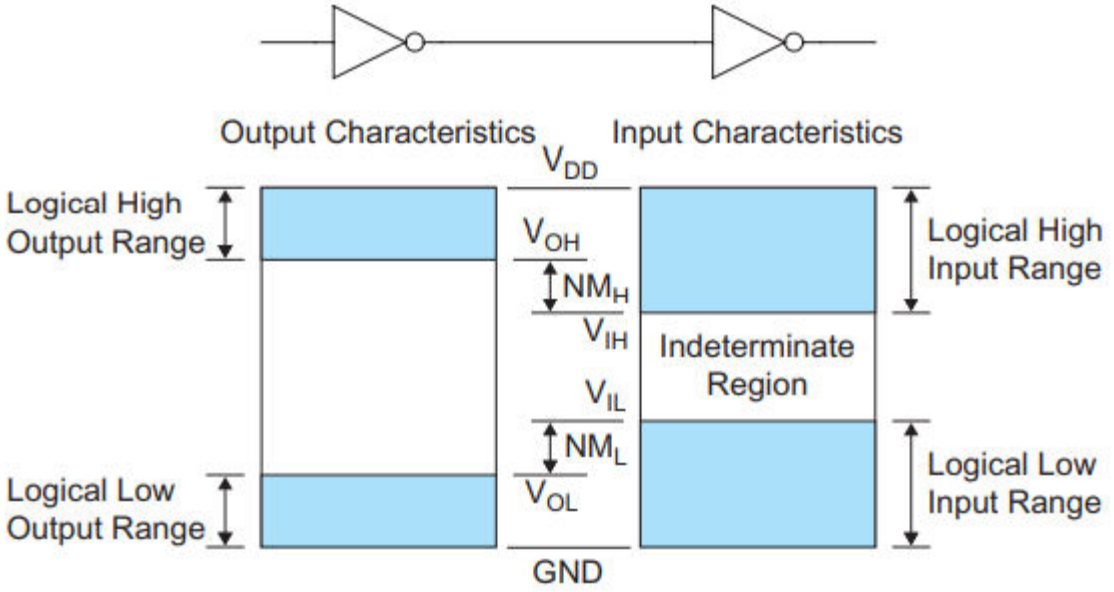
V_{OH}= minimum HIGH output voltage

V_{OL} = maximum LOW output voltage



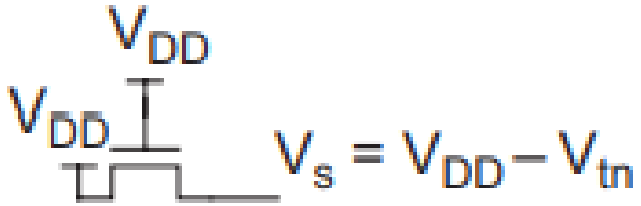
Noise Margin

- Inputs between VIL and VIH are said to be in the indeterminate region or forbidden zone and do not represent legal digital logic levels.
- Therefore, it is generally desirable to have VIH as close as possible to VIL and for this value to be midway in the "logic swing," VOL to VOH.



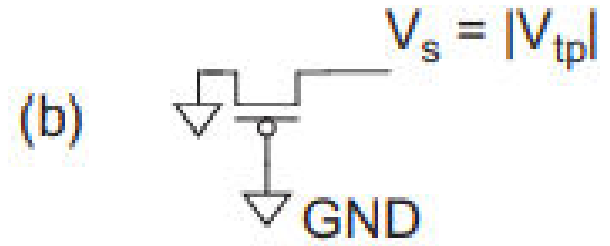
Pass Transistor DC Characteristics

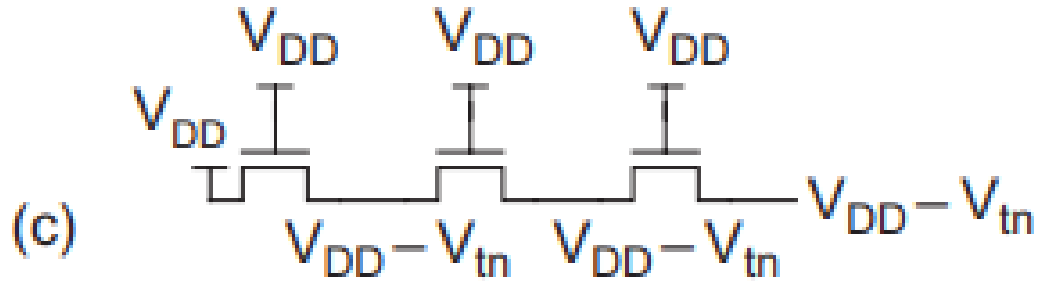
- Figure shows an nMOS transistor with the gate and drain tied to VDD.
- If the source is initially at $V_s = 0$.
- $V_{gs} > V_{tn}$, so the transistor is ON and current flows.
- If the voltage on the source rises to $V_s = V_{DD} - V_{tn}$, V_{gs} falls to V_{tn} and the transistor cuts itself OFF.
- Therefore, nMOS transistors attempting to pass a 1 never pull the source above VDD – Vtn.
- This loss is sometimes called a threshold drop.

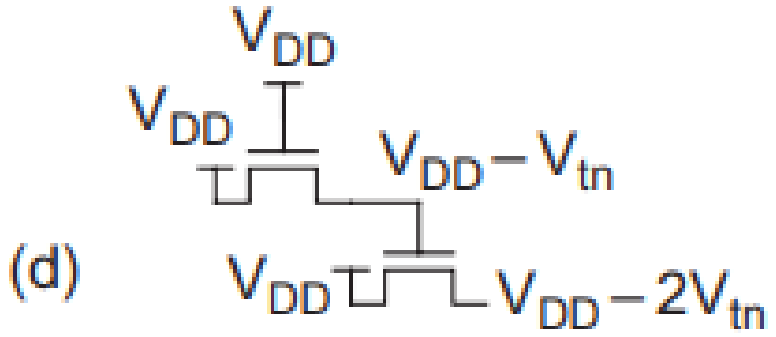


Pass Transistor DC Characteristics

- pMOS transistors pass 1s well but 0s poorly.
- If the pMOS source drops below $|V_{tp}|$, the transistor cuts off.
- Hence, pMOS transistors only pull down to within a threshold above GND, as shown in Figure







- 49,38,037,407,400,412,001,02127,012,066,052,90,61,36,40,404,67,85,59,409,401,28,34,14,31,13,18ec42,89,80,50,82,76,005,002,87,65,88,72
- Absent – 1,21,27,59,50, present – 413,411,35,56,23,69,79