Department of Computer Science Engineering – (Data Science)

COURSE MODULE OF THE SUBJECT TAUGHT FOR THE SESSION 2024-25 (ODD SEM)

Course Syllabi with CO's

Faculty Name: Dr. Vinod Kumar P			Academic Year: 2024 - 2025				
Department: Computer Science & Engineering- Data Science							
Course Code	**Course Title**	**Core / Elective**	**Prerequisite**	**Contact Hours**			**Total Hrs/ Sessions**
				L	**T**	**P**	
BCS302	Digital Design and Computer Organization	Core	Introduction to Electronics Communication	3	0	2	40T+20P
Course Objectives	1. To demonstrate the functionalities of binary logic system 2. To explain the working of combinational and sequential logic system 3. To realize the basic structure of computer system 4. To illustrate the working of I/O operations and processing unit						

Topics Covered as per Syllabus

Module-1

Introduction to Digital Design: Binary Logic, Basic Theorems And Properties Of Boolean Algebra, Boolean Functions, Digital Logic Gates, Introduction, The Map Method, Four-Variable Map, Don't-Care Conditions, NAND and NOR Implementation, Other Hardware Description Language – Verilog Model of a simple circuit.

Module-2

Combinational Logic: Introduction, Combinational Circuits, Design Procedure, Binary Adder-Subtractor, Decoders, Encoders, Multiplexers. HDL Models of Combinational Circuits – Adder, Multiplexer, Encoder. Sequential Logic: Introduction, Sequential Circuits, Storage Elements: Latches, Flip-Flops.

Module-3

Basic Structure of Computers: Functional Units, Basic Operational Concepts, Bus structure, Performance Processor Clock, Basic Performance Equation, Clock Rate, Performance Measurement.Machine Instructions and Programs: Memory Location and Addresses, Memory Operations, Instruction and Instruction sequencing, Addressing Modes.

Module-4

Input/output Organization: Accessing I/O Devices, Interrupts – Interrupt Hardware, Enabling and Disabling Interrupts, Handling Multiple Devices, Direct Memory Access: Bus Arbitration, Speed, size and Cost of memory systems. Cache Memories – Mapping Functions.

Module-5

Basic Processing Unit: Some Fundamental Concepts: Register Transfers, Performing ALU operations, fetching a word from Memory, Storing a word in memory. Execution of a Complete Instruction. Pipelining: Basic concepts, Role of Cache memory, Pipeline Performance.

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Laboratory Component:

1. Given a 4-variable logic expression, simplify it using appropriate technique and simulate the same using basic gates.
2. Design a 4 bit full adder and subtractor and simulate the same using basic gates.
3. Design Verilog HDL to implement simple circuits using structural, Data flow and Behavioural model.
4. Design Verilog HDL to implement Binary Adder-Subtractor – Half and Full Adder, Half and Full Subtractor.
5. Design Verilog HDL to implement Decimal adder.
6. Design Verilog program to implement Different types of multiplexer like 2:1, 4:1 and 8:1.
7. Design Verilog program to implement types of De-Multiplexer.
8. Design Verilog program for implementing various types of Flip-Flops such as SR, JK and D

List of Textbook and Reference book

1. M. Morris Mano & Michael D. Ciletti, Digital Design With an Introduction to Verilog Design, 5e, Pearson Education.
2. Carl Hamacher, Zvonko Vranesic, SafwatZaky, Computer Organization, 5 th Edition, Tata McGraw Hill.

Web links and Video Lectures (e-Resources)

https://cse11-iiith.vlabs.ac.in/

Course Outcomes	At the end of the course, the student will be able to: 1. CO1: **Apply** the K–Map techniques to simplify various Boolean expressions. 2. CO2: **Design** different types of combinational and sequential circuits along with Verilog programs. 3. CO3: **Describe** the fundamentals of machine instructions, addressing modes and Processor performance. 4. CO4: **Explain** the approaches involved in achieving communication between processor and I/O devices. 5. CO5: **Analyze** internal Organization of Memory and Impact of cache/Pipelining on Processor Performance.

Internal Assessment Marks: 50 (CIE marks for the theory component are 25 marks and that for the practical component is 25 marks. 25 marks for the theory component are split into 15 marks for internal Assessment Tests and 10 marks for other Assessment. 25 marks for the practical component are split into 15 marks for the conduction of the experiment and preparation of laboratory record, and 10 marks for the test to be conducted after the completion of all the laboratory sessions.).

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The Correlation of Course Outcomes (CO's) and Program Outcomes (PO's)

Course Code:	BCS302	TITLE: Digital Design and Computer Organization						Faculty Name:		Dr. Vinod Kumar P	
List of Course Outcomes	Program Outcomes										
	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12
CO-1	3	-	-	-	3	-	-		3	3	-	2
CO-2	3	2	2	-	3	-	-	-	3	3	-	2
CO-3	3	-	-	-	-	-	-	-	-	-	-	2
CO-4	3	-	-	-	-	-	-	-	-	-	-	2
CO-5	3	2	-	-	-	-	-	-	-	-	-	2

Note: 3 = Strong Contribution, 2 = Average Contribution, 1 = Weak Contribution, - = No Contribution

The Correlation of Course Outcomes (CO's) and Program Specific Outcomes (PSO's)

Course Code	BCS402	Title: Digital Design and Computer Organization	Faculty name: Dr. Vinod Kumar P
List of Course Outcomes	Program Specific Outcomes		
	PSO1	PSO2	PSO3
CO1	2	-	-
CO2	2	-	-
CO3	2	-	-
CO4	2	-	-
CO5	2	-	-

Note: 3 = Strong Contribution, 2 = Average Contribution, 1 = Weak Contribution, - = No Contribution