Department of Computer Science & Engineering (Data Science)

Lesson Plan &Work-done Diary for AY: 2024-25, ODD Semester

Course with Code: Digital Design and Computer Organization - BCS302				Faculty: Dr Vinod Kumar P			Semester & Section: 3	
Class No.	**Date planned (DD/MM)**	**Topics to be covered**	**TLP Planned**	**Class No.**	**Date of Conduction (DD/MM)**	**Topics Covered**	**TLP Executed**	**Remarks if any deviation**
MODULE-1								
1.		Introduction to Digital Design and Computer Organization	Chalk & Talk PPT					
2.		Binary Logic	Chalk & Talk PPT					
3.		Basic Theorems And Properties Of Boolean Algebra	Chalk & Talk PPT					
4.		Boolean Functions	Chalk & Talk PPT					
5.		Digital Logic Gates	Chalk & Talk PPT					
6.		Introduction to K-Map. The Map Method	Chalk & Talk PPT					
7.		Four-Variable Map, Don’t-Care Conditions, Other	Chalk & Talk PPT					
8.		NAND and NOR Implementation	Chalk & Talk PPT					
9.		Hardware Description Language – Verilog Model of a simple circuit.	Chalk & Talk PPT					

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MODULE-2								
10		Combinational Logic: Introduction	Chalk & Talk PPT					
11		Combinational Circuits, Design Procedure, Binary Adder- Subtractor.	Chalk & Talk PPT					
12		Decoders, Encoders	Chalk & Talk PPT					
13		Multiplexers.	Chalk & Talk PPT					
14		HDL Models of Combinational Circuits	Chalk & Talk PPT					
15		Adder, Multiplexer, Encoder	Chalk & Talk PPT					
16		Sequential Logic: Introduction	Chalk & Talk PPT					
17		Sequential Circuits, Storage Elements: Latches,	Chalk & Talk PPT					
18		Flip-Flops.	Chalk & Talk PPT					

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MODULE-3								
19		Basic Structure of Computers: Functional Units	Chalk & Talk PPT,					
20		Basic Operational Concepts	Chalk & Talk PPT,					
21		Bus structure	Chalk & Talk PPT,					
22		Performance Processor Clock, Basic Performance Equation, Clock Rate	Chalk & Talk PPT,					
23		Performance Measurement	Chalk & Talk PPT,					
24		Machine Instructions and Programs:	Chalk & Talk PPT,					
25		Memory Location and Addresses, Memory Operations,	Chalk & Talk PPT,					
26		Instruction and Instruction sequencing,	Chalk & Talk PPT,					
27		Addressing Modes.	Chalk & Talk PPT,					

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MODULE-4								
28		Input/output Organization: Accessing I/O Devices	Chalk & Talk PPT					
29		Interrupts – Interrupt Hardware	Chalk & Talk PPT					
30		Enabling and Disabling Interrupts	Chalk & Talk PPT					
31		Handling Multiple Devices	Chalk & Talk PPT					
32		Direct Memory Access: Bus Arbitration, Speed	Chalk & Talk PPT					
33		Size and Cost of memory systems	Chalk & Talk PPT					
34		Cache Memories	Chalk & Talk PPT					
35		Mapping Functions.	Chalk & Talk PPT					

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MODULE-5								
36		Basic Processing Unit: Some Fundamental Concepts	Chalk & Talk PPT	1				
37		Register Transfers	Chalk & Talk PPT	2				
38		Performing ALU operations	Chalk & Talk PPT	3				
39		fetching a word from Memory, Storing a word in memory	Chalk & Talk PPT	4				
40		Execution of a Complete Instruction	Chalk & Talk PPT	5				
41		Pipelining: Basic concepts	Chalk & Talk PPT	6				
42		Role of Cache memory,	Chalk & Talk PPT	7				
43		Pipeline Performance.	Chalk & Talk PPT	8				

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LAB COMPONENT								
1.		Introduction to the tool, procedure to create circuit diagram, simulate and verify the output waveform.	Electronic workbench					
2.		Simulation of simple circuits using electronics workbench	Electronic workbench					
3.		Given a 4-variable logic expression, simplify it using appropriate technique and simulate the same using basic gates.	Electronic workbench					
4.		Design a 4 bit full adder simulate the same using basic gates.	Electronic workbench					
5.		Design a 4 bit full subtractor and simulate the same using basic gates.	Electronic workbench					
6.		Introduction to the tool, procedure to create Project, simulate and verify the output waveform.	Xilinx 14					
7.		Design Verilog HDL to implement simple circuits using structural, Data flow and Behavioural model.	Xilinx 14					
8.		Design Verilog HDL to implement Binary Adder-Subtractor – Half and Full Adder, Half and Full Subtractor.	Xilinx 14					
9.		Design Verilog program to implement Different types of multiplexer like 2:1, 4:1 and 8:1	Xilinx 14					
10.		Design Verilog program to implement types of De-Multiplexer.	Xilinx 14					
11.		Design Verilog program for implementing various types of Flip-Flops such as SR, JK and D.	Xilinx 14					

	Activity	Planned	Actual	Remarks
1	Theory Classes/ Lab Session	43/ 11		
2	Assignments/ Quizzes/ Self-study	5		
3	Tutorials/ Extra classes	2		
4	Internal Assessments/ Lab Test	3/1		
5	ICT based Teaching (% of usage in Curriculum)	70%		
Planning			**Execution**	
Faculty Signature:			**Faculty Signature:**	
HoD Signature:			**HoD Signature:**	