COURSE MODULES OF THE SUBJECT TAUGHT FOR THE EVEN SEMESTER 2025-2026

Course Syllabi with CO's

Simulation and Control of Power Electronics Circuits		Semester	VI
Faculty Name: Dr Sathish K R		**AY: 2025-26**	
Course Code	BEEL657B	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	0-0-1	SEE Marks	50
Credits	01	Exam Hours	100
Examination type (SEE)	practical/Viva-Voce		

Course objectives:

- To be able to simulate any DC-DC converter and observe the performance under various test conditions
- To be able to simulate single phase and three phase DC –AC converters and observe the performance under various test conditions
- To be able to simulate uncontrolled, half controlled and fully controlled AC-DC converters and observe the performance under various test conditions

Sl.NO	Experiments
1	(a)Simulate a single-phase half-wave diode bridge rectifier. Input 100V, 50 Hz. AC supply. At the out put, resistance of 50 ohms. (b)Simulate a single-phase full-wave diode bridge rectifier. Input 100V, 50 Hz. AC supply. At the out put, resistance of 50 ohms.
2	(a) Simulate a single phase half controlled full wave rectifier. Input 100V, 50 Hz. AC supply. At the output, resistance of 50 ohms. (b) Simulate a single-phase fully controlled full-wave rectifier. Input 100V, 50 Hz. AC supply. At the out put, resistance of 50 ohms.
3	Simulate a buck converter with 20 V DC input, and regulate the output at 10 V by implementing a PI controller for closed loop operation. The out put power to vary from 10 W to 20 W. Ensure that voltage ripple is limited to 1%.
4	Simulate a boost converter with 20 V DC input, and regulate the output at 35 V by implementing a PI controller for closed-loop operation. The output power varies from 30W to 60 W. Ensure that the voltage ripple is limited to 1%
5	Simulate a single phase AC voltage controller using a triac with 100V ,50 Hz. AC supply for an RL load of 10 oms and 2 mH.
6	Simulate a three-phase inverter with 180-degree conduction mode with a DC input of 100V and a star-connected balanced resistive of 40 ohms each. Use an IGBT for the inverter.
7	Simulate a single-phase SPWM inverter with 50V DC input with modulation indices of 0.5, 0.6 and 0.8. Connect a resistance of 25 ohms at the output of the inverter. Use power MOSFETs for the inverter.
8	Simulate a three-phase inverter with 120 degree mode of conduction. Take input DC voltage of 100V and three phase star connected balanced resistive load of 50 ohms each.
	Demonstration Experiments (For CIE)
9	In expt. 8. connect suitable LC filter at the output to obtain a sinusoidal output with THD of less than 8 %.

10	Simulate a three phase SPWM inverter with 50V DC input with modulation indices of 0.5, 0.6 and 0.8. connect a star connected resistances of 25 ohms each at the output of the inverter. Use power Mosfets for inverter.
11	Simulate a three phase, 5 level, neutral point clamped (NPC) inverter. Input DC voltage is 100V. The inverter output is connected to a balanced 3 phase resistive load of 40 Ohms each.
12	Simulate a forward converter with input DC voltage of 30 V. Take transformer ratio of 1.5:1. Observe the output voltages for duty cycles of 0.4, 0.6 and 0.8. Ensure that the output voltage ripple is less than 0.5 V. The load resistance is 10 Ohms.

Course outcomes (Course Skill Set):

At the end of the course the student will be able to:

CO1: Simulate any given power electronic circuit and evaluate its performance under different test conditions and also observe the performance for different values of passive filtering elements used in the converter.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation (CIE):

CIE marks for the practical course are **50 Marks**.

The split-up of CIE marks for record/ journal and test are in the ratio **60:40**.

- Each experiment is to be evaluated for conduction with an observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments are designed by the faculty who is handling the laboratory session and are made known to students at the beginning of the practical session.
- Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.
- Total marks scored by the students are scaled down to **30 marks** (60% of maximum marks).
- Weightage to be given for neatness and submission of record/write-up on time.
- Department shall conduct a test of 100 marks after the completion of all the experiments listed in the syllabus.
- In a test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.
- The suitable rubrics can be designed to evaluate each student's performance and learning ability.
- The marks scored shall be scaled down to **20 marks** (40% of the maximum marks).

The Sum of scaled-down marks scored in the report write-up/journal and marks of a test is the total CIE marks scored by the student.

Semester End Evaluation (SEE):

- SEE marks for the practical course are 50 Marks.
- **SEE shall be conducted by the two examiners. One from the same institute as an internal examiner and another from a different institute as an external examiner, appointed by the university.**
- The examination schedule and names of examiners are informed to the university before the conduction of the examination. These practical examinations are to be conducted between the schedule mentioned in the

The Correlation of Course Outcomes (CO's) and Program Outcomes (PO's)

Course Code:	BEEL657B	TITLE: **Simulation and Control of Power Electronics Circuits**					Faculty Name:			Dr. Sathish K R		
Course Outcomes	Program Outcomes											
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO-1	3	3	2	2	3	-	1	-	-	-	-	2

Note: 3 = Strong Contribution 2 = Average Contribution 1 = Weak Contribution = No Contribution

The Correlation of Course Outcomes (CO's) and Program Specific Outcomes (PSO's)

Subject Code:	BEE503	TITLE: Power Electronics
List of Course Outcomes	PSO1	PSO2
CO-1	2	-

Note: 3 = Strong Contribution 2 = Average Contribution 1 = Weak Contribution '-'= No Contribution

Justification for CO1–PO Mapping

- **PO1 (Engineering knowledge) – 3**
  Application of power electronics theory, circuit laws, and converter principles during simulation and analysis.
- **PO2 (Problem analysis) – 3**
  Evaluation of converter performance under varying load, input, and filter parameters.
- **PO3 (Design/development of solutions) – 2**
  Selection and tuning of passive filter elements to meet ripple and performance constraints.
- **PO4 (Investigation of complex problems) – 2**
  Interpretation of simulation waveforms, THD, ripple, and efficiency under different test cases.
- **PO5 (Modern tool usage) – 3**
  Extensive use of **MATLAB/Simulink** for modeling, simulation, and performance evaluation.
- **PO7 (Environment and sustainability) – 1**
  Indirect consideration through efficiency improvement and ripple reduction.
- **PO12 (Life-long learning) – 2**
  Exposure to simulation tools and evolving power electronic topologies encourages continuous learning.