COURSE MODULE

Academic Year:**2025-26**							
Department: **Electronics and Communication Engineering**							
Course Code	Course Title	Core/Elective	Prerequisite	Contact Hours			Total Hrs/ Sessions
				L	T	P	
BEC602	**VLSI Design and Testing**	**core**	**Basic VLSI, Digital Electronics, Verilog**	**4**	**0**	**0**	**50**

Course objectives: This course (BEC602) will enable students to:

CLO1: This course deals with analysis and design of digital CMOS integrated circuits.

CLO2: The course emphasizes on basic theory of digital circuits, design principles and techniques for digital design blocks implemented in CMOS technology.

CLO3: This course will also cover switching characteristics of digital circuits along with delay and power estimation.

CLO4: Understanding the CMOS sequential circuits and memory design concepts.

CLO5: Explore the knowledge of VLSI Design flow and Testing

Topics Covered as per Syllabus

MODULE-I

Introduction to CMOS Circuits: Introduction, MOS Transistors, MOS Transistor switches, CMOS Logic, Alternate Circuit representation, CMOS-nMOS comparison.

[Text 1: 1.1,1.2,1.3,1.4,1.5.1.6.] **(RBT: L1, L2, L3)**

MODULE-2

MOS Transistor Theory: n-MOS enhancement transistor, p-MOS transistor, Threshold Voltage, Threshold voltage adjustment, Body effect, MOS device design equations, V-I characteristics, CMOS inverter DC characteristics, Influence of βn / βp ratio on transfer characteristics, Noise margin, Alternate CMOS inverters. Transmission gate DC characteristics. Latch-up in CMOS.

[Text 1: 2.1,2.2,2.3,2.4,2.5.2.6.] **(RBT: L1, L2, L3)**

MODULE - 3

CMOS Process Technology: Silicon Semiconductor Technology, CMOS Technologies, Layout Design Rules. [Text 1: 3.1,3.2,3.3.]

Circuit Characterization and Performance Estimation: Introduction, Resistance Estimation, Capacitance Estimation, Switching Characteristics, CMOS gate transistor sizing, Determination of conductor size, Power consumption, Charge sharing, Scaling of MOS transistor sizing, Yield.

[Text 1: 4.1,4.2,4.3,4.4,4.5.4.6.4.7,4.8,4.9,4.10] **(RBT: L1, L2, L3)**

MODULE-4

CMOS Circuit and Logic Design: Introduction, CMOS Logic structures, CMOS Complementary logic, Pseudo n-MOS logic, Dynamic CMOS logic, Clocked CMOS Logic, Cascade Voltage Switch logic, Pass transistor Logic, Electrical and Physical design of Logic gates, The inverter, NAND and NOR gates, Body effect, Physical Layout of Logic gates, Input output Pads.

[Text 1: 5.1,5.2,5.2.1, , 5.2.2, 5.2.3, 5.2.4, 5.2.6, 5.2.8, 5.3,5.3.1,5.3.2, 5.3.4 ,5.3.8,5.5] **(RBT: L1, L2, L3)**

MODULE-5

Sequential MOS Logic Circuits: Introduction, Behavior of Bistable Elements (Excluding Mathematical analysis) SR Latch Circuit, Clocked Latch and Flip-Flop Circuits, Clocked SR Latch, Clocked JK Latch.

[Text2: 8.1, 8.2, 8.3, 8.4]

Structured Design and Testing: Introduction, Design Styles, Testing

[Text1: 6.1, 6.2. 6.5] **(RBT: L1, L2, L3)**

List of Textbooks

1. Principals of CMOS VLSI Design A System approach Neil H E Weste and Kamran Eshraghain . Addition Wisley Publishing company.
2. "CMOS Digital Integrated Circuits: Analysis and Design", Sung Mo Kang & Yosuf Leblebici, Third Edition, Tata McGraw-Hill.

List of URLs, Text Books, Notes, Multimedia Content, etc

1. https://m.youtube.com/playlist?list=PLfMCiCIRnpUkZjEsg1bc4DNZFa4P0DzBx
2. https://youtu.be/otOSL1ZLnOo
3. https://youtu.be/eS_1Numj7Oo

4. "CMOS VLSI Design- A Circuits and Systems Perspective", Neil H E Weste, and David Money Harris 4th Edition, Pearson Education.
5. "Basic VLSI Design", Douglas A Pucknell, Kamran Eshraghian, 3rd Edition, Prentice Hall of India publication, 2005.

Course Outcomes (Course Skill Set): Students will be able to

1. Apply the fundamentals of semiconductor physics in MOS transistors and analyze the geometrical effects of MOS transistors.
2. Design and realize combinational, sequential digital circuits and memory cells in CMOS Logic.
3. Analyze the synchronous timing metrics for sequential designs and structured design basics.
4. Understand designing digital blocks with design constraints such as propagation delay and dynamic power dissipation.
5. Understand the concepts of Sequential circuits design and VLSI testing

Assessment Details (both CIE and SEE):

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 35% (18 Marks out of 50) in the semester-end examination (SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

Three Unit Tests each of 20 Marks (duration 01 hour)

1. First test at the end of 5th week of the semester
2. Second test at the end of the 10th week of the semester
3. Third test at the end of the 15th week of the semester

Two assignments each of 10 Marks

4. First assignment at the end of 4th week of the semester
5. Second assignment at the end of 9th week of the semester

Group discussion/Seminar/quiz any one of three suitably planned to attain the COs and POs for 20 Marks (duration 01 hours)

6. At the end of the 13th week of the semester

The sum of three tests, two assignments, and quiz/seminar/group discussion will be out of 100 marks and will be scaled down to 50 marks (to have less stressed CIE, the portion of the syllabus should not be common /repeated for any of the methods of the CIE. Each method of CIE should have a different syllabus portion of the course).

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the subject (duration 03 hours)

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), should have a mix of topics under that module.

The students have to answer 5 full questions, selecting one full question from each module.. Marks scored out of 100 shall be reduced proportionally to 50 marks

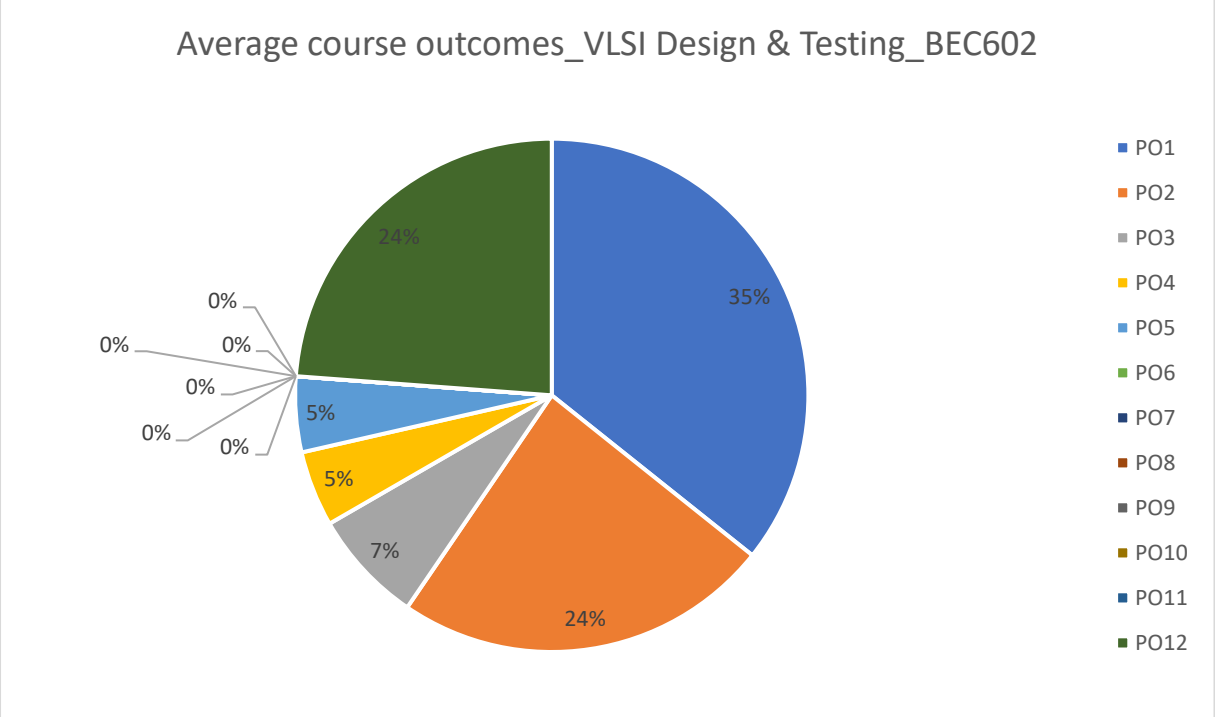
The Correlation of Course Outcomes (CO's) and Program Outcomes (PO's)

Subject Code:	BEC602		**TITLE:** VLSI Design and Testing									Total
List of Course Outcomes	Program Outcomes											
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	
CO-1(L3)	3	2	1	-	-	-	-	-	-	-	1	7
CO-2(L3)	3	2	3	-	2	-	-	-	-	-	1	11
CO-3(L2)	3	3	2	-	2	-	-	-	-	-	1	11
CO-4(L2)	3	3	3	-	2	-	-	-	-	-	1	12
CO-5(L1)	2	2	2	1	2	-	-	-	-	-	1	10
Total	14	12	11	1	8	-	-	-	-	-	5	51

The Correlation of Course Outcomes (CO's) and Program Specific Outcomes (PSO's)

Subject Code: BEC602		**TITLE:** VLSI Design and Testing	
List of Course Outcomes	**Program Specific Outcomes**		
	PSO1	**PSO2**	**Total**
CO-1(L3)	3	2	**5**
CO-2(L3)	3	2	**5**
CO-3(L2)	3	2	**5**
CO-4(L2)	2	2	**4**
CO-5(L1)	3	2	**5**
Total	**14**	**10**	**24**
Ave. CO	**2.00**	**2.00**	**4.00**

Note: 3 = Strong Contribution 2 = Average Contribution
1 = Weak Contribution - = No Contribution



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