Lesson Plan &Work-done Diary for AY:2025-26 EVEN Semester

Course with Code: VLSI Design and Testing_BEC602							**Semester:** 6
Class No.	**Date planned (DD/MM)**	**Topics to be covered**	**TLP Planned**	**Date of Conduction (DD/MM)**	**Topics Covered**	**TLP Executed**	**Remarks if any deviation**
1		Module 0_Bridge course on VLSI	PPT				
2		Module 0_Bridge course on VLSI					
3		Module 0_Bridge course on VLSI					
Module-1							
4		Introduction to CMOS Circuits: Introduction, MOS Transistors, MOS Transistor switches,	PPT				
5		CMOS Logic					
6		Alternate Circuit representation,					
7		CMOS-nMOS comparison					
8		Revision and VTU QP Discussion, Quiz/SRS					

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Module-2							
Class No.	**Date planned (DD/MM)**	**Topics to be covered**	**TLP Planned**	**Date of Conduction (DD/MM)**	**Topics Covered**	**TLP Executed**	**Remarks if any deviation**
9		MOS Transistor Theory: n-MOS enhancement transistor, p-MOS transistor	PPT				
10		Threshold Voltage, Threshold voltage adjustment,					
11		Body effect					
12		MOS device design equations,					
13		V-I characteristics					
14		CMOS inverter DC characteristics, Influence of βn / βp ratio on transfer characteristics					
15		Noise margin,					
16		Alternate CMOS inverters.					
17		Transmission gate DC characteristics Latch-up in CMOS					
18		Revision and VTU QP Discussion, Quiz/SRS					

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Module-3							
Class No.	**Date planned (DD/MM)**	**Topics to be covered**	**TLP Planned**	**Date of Conduction (DD/MM)**	**Topics Covered**	**TLP Executed**	**Remarks if any deviation**
19		CMOS Process Technology: Silicon Semiconductor Technology	PPT				
20		CMOS Technologies					
21		CMOS Technologies					
22		CMOS Technologies					
23		Layout Design Rules					
24		Layout Design Rules					
25		Layout Design Rules					
26		Introduction, Resistance Estimation					
27		Capacitance Estimation, Switching Characteristics, CMOS gate transistor sizing					
28		Determination of conductor size, Power consumption					
29		Charge sharing, Scaling of MOS transistor sizing, Yield					
30		Revision and VTU QP Discussion, Quiz/SRS					

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Module-4							
Class No.	**Date planned (DD/MM)**	**Topics to be covered**	**TLP Planned**	**Date of Conduction (DD/MM)**	**Topics Covered**	**TLP Executed**	**Remarks if any deviation**
31		CMOS Circuit and Logic Design: Introduction, CMOS Logic structures	PPT				
32		CMOS Complementary logic, Pseudo n-MOS logic,					
33		Dynamic CMOS logic					
34		Clocked CMOS Logic, CMOS Domino logic					
35		Cascade Voltage Switch logic, Pass transistor Logic,					
36		Electrical and Physical design of Logic gates					
37		The inverter, NAND and NOR gates,					
38		Body effect, Source – drain Capacitance					
39		Physical Layout of Logic gates, Input output Pads.					
40		Revision and VTU QP Discussion, Quiz/SRS					

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Module-5							
Class No.	**Date planned (DD/MM)**	**Topics to be covered**	**TLP Planned**	**Date of Conduction (DD/MM)**	**Topics Covered**	**TLP Executed**	**Remarks if any deviation**
41		Sequential MOS Logic Circuits: Introduction,	PPT				
42		Behaviour of Bistable Elements (Excluding Mathematical analysis)					
43		SR Latch Circuit					
44		Clocked Latch					
45		Flip-Flop Circuits					
46		Clocked SR Latch,					
47		Clocked JK Latch.					
48		Structured Design and Testing:					
49		Introduction, Design Styles, Testing					
50		Revision and VTU QP Discussion, Quiz/SRS					

	Activity	Planned	Actual	Remarks
1	Theory Classes + Practical	50		
2	Assignments/Quizzes/Self-study	2/5/2		
3	Tutorials/ Extra classes	-		
4	Internal Assessments	3		
5	ICT based Teaching (% of usage in Curriculum)	100 %		
Planning			**Execution**	
Faculty Signature:			**Faculty Signature:**	
HoD Signature:			**HoD Signature:**	