ATME COLLEGE OF ENGINEERING

13th KM Stone, Bannur Road, Mysore - 570 028

DEPARTMENT OF ELECTRICAL & ELECTRONICS ENGINEERING

NOTES

SUBJECT: ANALOG ELECTRONIC CIRCUITS

SEMESTER: III

Prepared by

Department of EEE,

ATME College of Engineering

INSTITUTIONAL VISION AND MISSION

VISION:

- Development of academically excellent, culturally vibrant, socially responsible and globally competent human resources.

MISSION:

- To keep pace with advancements in knowledge and make the students competitive and capable at the global level.
- To create an environment for the students to acquire the right physical, intellectual, emotional and moral foundations and shine as torchbearers of tomorrow's society.
- To strive to attain ever-higher benchmarks of educational excellence.

Department Vision and Mission

Vision:

To create Electrical and Electronics Engineers who excel to be technically competant and fulfill the cultural and social aspirations of the society.

Mission:

- To provide knowledge to students that builds a strong foundation in the basic principles of electrical engineering, problem solving abilities, analytical skills, soft skills and communication skills for their overall development.
- To offer outcome based technical education.
- To encourage faculty in training & development and to offer consultancy through research & industry interaction.

Program Educational Objectives (PEOs)

PEO1: To produce competent and ethical Electrical and Electronics Engineers who will exhibit the necessary technical and managerial skills to perform their duties in society.

PEO2: To make Graduates continuously acquire and enhance their technical and socio-economic skills.

PEO3: To aspire Graduates on R & D activities leading to offering solutions and excel in various career paths.

PEO4: To produce quality engineers who have the capability to work in teams and contribute to real time projects.

Program Outcomes (POs)

Engineering Graduates will be able to:

PO1: Engineering Knowledge: Apply the knowledge of mathematics, science, engineering fundamentals and an engineering specialization to the solution of complex engineering problems.

PO2: Problem Analysis: Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.

PO3: Design / Development of solutions: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.

PO4: Conduct investigations of complex problems: Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.

PO5: Modern tool usage: Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.

PO6: The engineer and society: Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.

PO7: Environment and sustainability: Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.

PO8: Ethics: Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.

PO9: Individual and team work: Function effectively as an individual and as a member or leader in diverse teams, and in multidisciplinary settings.

PO10: Communication: Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.

PO11: Project management and finance: Demonstrate knowledge and understanding of the engineering management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.

PO12: Life-long learning: Recognize the need for and have the preparation and ability to engage in independent and lifelong learning in the broadest context of technological change.

Program Specific Outcomes (PSOs)

The students will develop an ability to produce the following engineering traits:

PSO1: Apply the concepts of Electrical and Electronics Engineering to evaluate the performance of powe system and also to control industrial drives by using power electronics.

PSO2: Demonstarte the concepts of process control for Industrial Automation, design models for environmental and social concerns and also exhibit continuous self-learning.

Module – I

Contents:

Diode Circuits: Diode clipping and clamping circuits.
Transistor biasing and stabilization: Operating point, analysis and design of fixed bias circuit, self- bias circuit, Emitter stabilized bias circuit, voltage divider bias circuit, stability factor of different biasing circuits. Problems and Transistor switching circuits**.**

Objectives:

1. To study the concepts of diode clipping and clamping circuits.
2. To design and analyse the transistor biasing circuits and switching circuits.

1.1. Diode Circuits

1.1.1. Diode Clipping Circuits or Limiting Circuits:

Clipping circuits are used to **remove a portion of a time varying input signal without distorting the remaining part of the applied waveform**. One simple example of a clipper is a **half-wave rectifier** which transfers only one half cycle of the input to the output, while clipping off the other half cycle. By changing orientation of the diode in the circuit, positive or negative portion of the input signal can be clipped off.

A. Shunt or Parallel Clipper:

In parallel clipper the diode appears in the **parallel branch or shunt** with the applied input signal. The Fig.1 shows a shunt clipper with bias or reference voltage V_R.

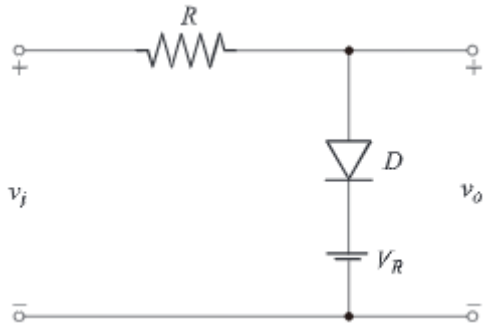


Fig.1.1: Shunt Clipper

The input signal can be any periodic signal such as sine, square, triangle etc. with peak value V_M greater than reference voltage V_R. If $\mathbf{V_M < V_R}$, the clipping does not takes place. Just before the diode conducts, the current through R is zero and hence input signal is V_I is directly available at the anode of the diode as shown in Fig.1.2.

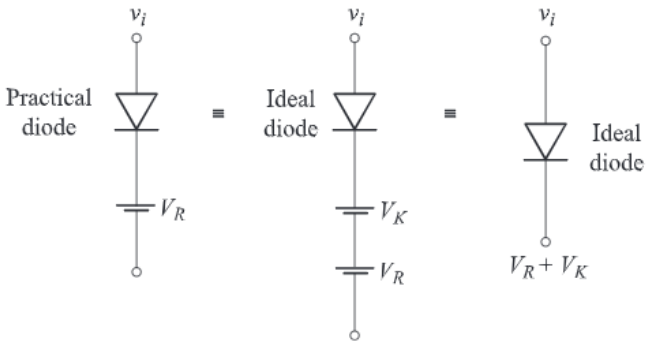


Fig.1.2: Voltage at diode terminals

For the ideal diode to conduct, it is enough that the anode voltage just equals the cathode voltage. For the circuit in Fig.1.1 the diode conducts for $\mathbf{v_I \geq V_R + V_K}$. The equivalent circuit during the diode conduction is shown in Fig.1.3 (a).

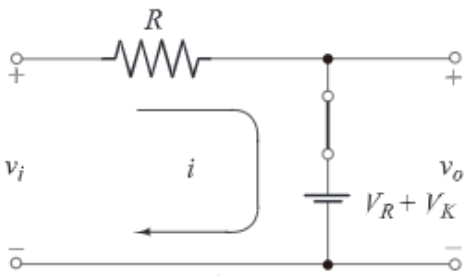


Fig.1.3 (a): Diode Conduction

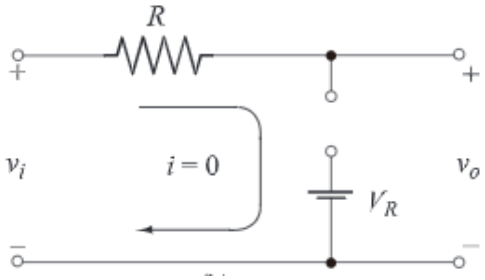


Fig.1.3 (b): Diode Off

From the circuit of Fig.1.3 (a) we find that

$$\mathbf{v_O = V_R + V_K \text{ for } v_I \geq V_R + V_K} \text{ ---------- (1)}$$

For $v_I \leq V_R + V_K$, the diode is off and the equivalent circuit is shown in Fig.1.3 (b). By applying KVL to the circuit we get,

$$\mathbf{v_i - iR - v_o = 0}$$

$$\mathbf{v_o = v_i, \text{ for } v_i \leq V_R + V_K} \text{ ---------- (2)}$$

The output waveforms are shown in Fig.1.4. The circuit clips off a portion of the input signal which lies above V_R+V_K and retains the remaining part as it is.

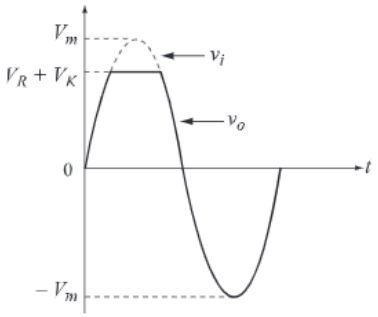


Fig.1.4: Waveforms of shunt clipper with positive clipping.

Transfer Characteristics:

The transfer characteristics are obtained by plotting v_o as a function of v_i. Transfer characteristics can be easily constructed by evaluating slope $\Delta v_o/\Delta v_i$.

For $v_I \geq V_R + V_K$ from equation (1), $\mathbf{v_o = V_R + V_K = constant}$

$$\mathbf{\Delta v_o = 0}$$

$$\textbf{Hence slope } \frac{\Delta v_o}{\Delta v_i} = \mathbf{0} \text{ ---------- (3)}$$

for $v_i \leq V_R + V_K$, from equation (2), $\mathbf{v_o = v_i}$

$$\mathbf{\Delta v_o = \Delta v_i}$$

$$\textbf{Hence slope } \frac{\Delta v_o}{\Delta v_i} = \mathbf{1} \text{ ---------- (4)}$$

The Fig.1.5 shows the transfer characteristics of shunt clipper along with output waveform for sinusoidal input.

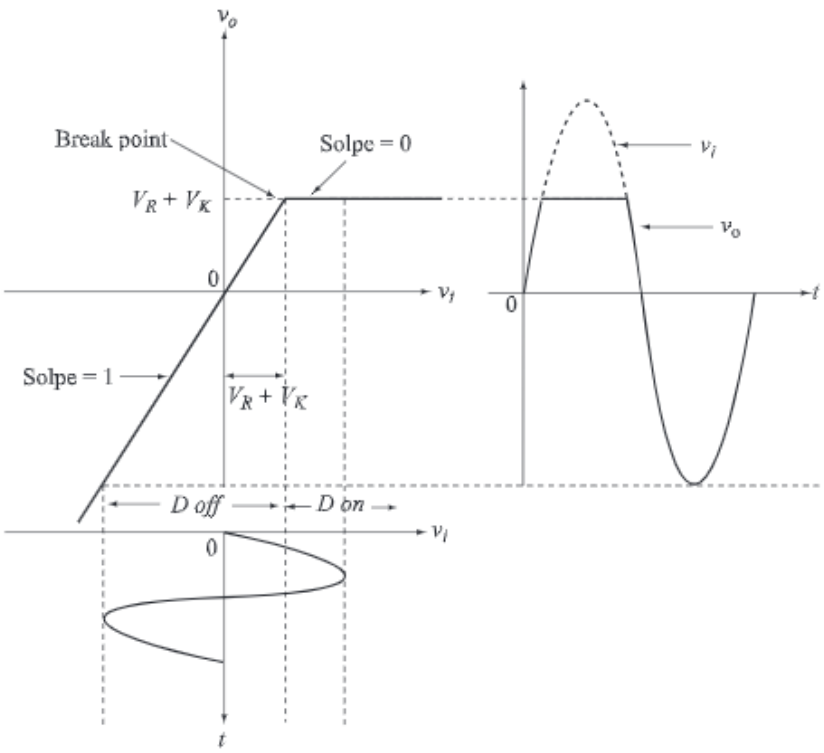


Fig.1.5: Transfer characteristics and output waveform of shunt clipper.

B. Series Clipper:

In series clipper the diode appears in series with the input or it appears in the series branch as shown in Fig.1.6. The voltage on diode terminals is shown in Fig.1.7.

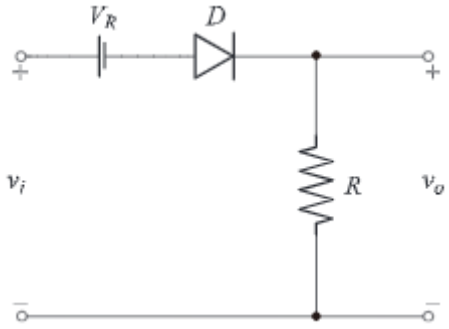


Fig.1.6: Series Clipper.

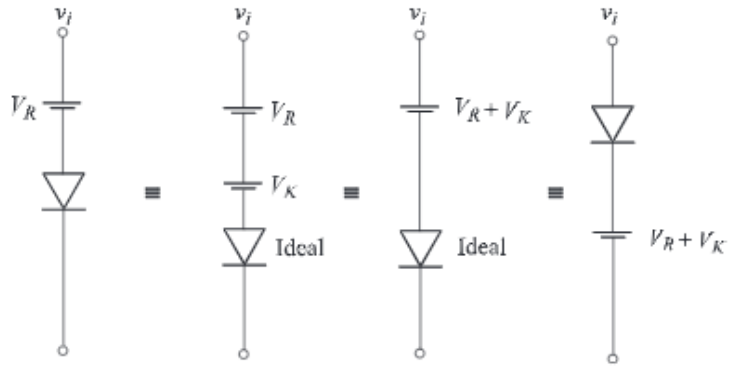


Fig.1.6: Voltage on Diode Terminals.

The diode conducts for $v_I \geq V_R + V_K$. The equivalent circuit during diode conduction is shown in Fig.1.7 (a).

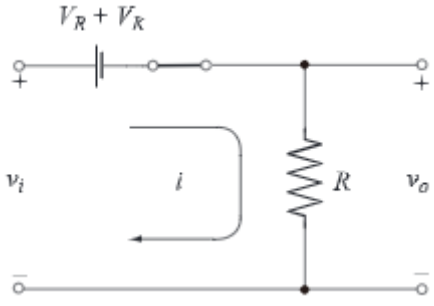


Fig.1.7 (a): Diode Conduction

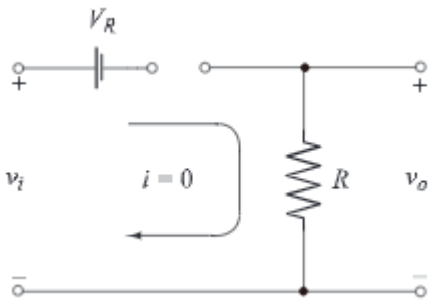


Fig.1.7 (b): Diode Off

Applying KVL to the circuit shown in Fig.1.7 (a) we have,

$$\mathbf{v_i - [V_R + V_K] - v_o = 0}$$

$$\mathbf{v_o = v_i - [V_R + V_K] \quad for\ v_I \geq V_R + V_K} \text{ ---------- } \mathbf{(5)}$$

Since $\mathbf{V_R + V_K}$ is constant

$$\mathbf{\Delta v_o = \Delta v_i}$$

$$\textbf{Hence slope } \frac{\Delta v_o}{\Delta v_i} = \mathbf{1}$$

From equation (5), when $v_i = v_m$,

$$\mathbf{v_o = v_m - [V_R + V_K]} \text{ ---------- (6)}$$

For $v_I \leq V_R + V_K$, the diode is off and the equivalent circuit is shown in Fig.1.7 (b). By applying KVL to the circuit we get,

$$\mathbf{v_o = iR = 0}$$

$$\textbf{Hence slope } \frac{\Delta v_o}{\Delta v_i} \mathbf{= 0} \text{ ---------- (7)}$$

The transfer characteristics and the output voltage waveform are shown in Fig.1.8.

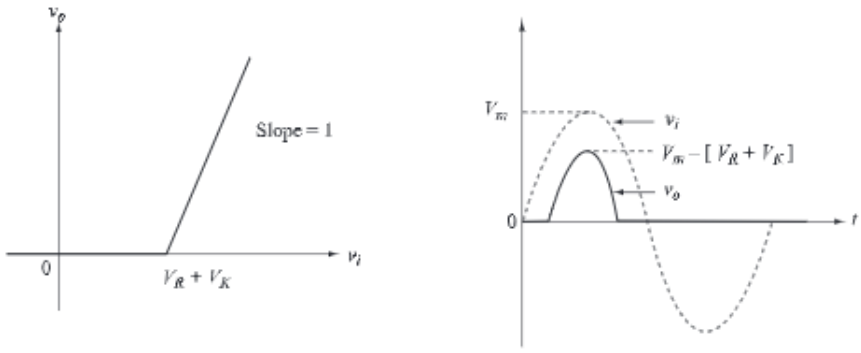


Fig.1.8: Transfer Characteristics and Output voltage Waveform.

C. Clipping at Two Independent Levels (Double ended clipper):

Two shunt clippers can be combined to obtain clipping at two independent levels. The Fig.1.9 shows the double ended clipper circuit which uses two reference voltages.

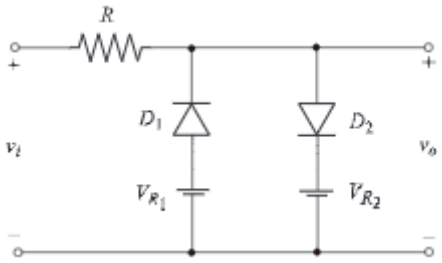


Fig.1.9: Double ended clipper circuit.

Note that V_{R1} and V_{R2} are positive. V_{R1} forward biases D_1 and V_{R2} reverse biases D_2 and also $V_{R2} > V_{R1}$. The voltages on the terminals of diode D_1 is shown in Fig.1.10.

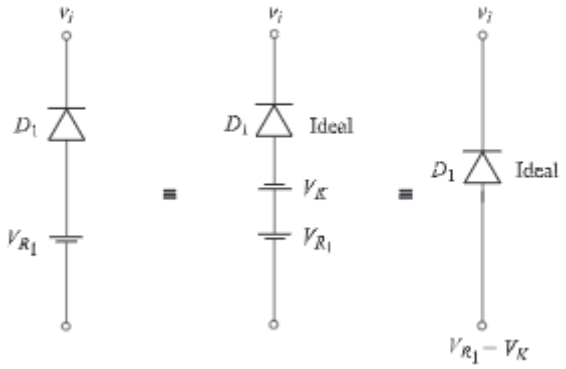


Fig.1.10: Terminal Voltages on D_1

The diode D_1 conducts for $\mathbf{v_I \leq V_{R1} - V_K}$. The equivalent circuit is shown in Fig.1.11 (a). We can find that;

$$\mathbf{v_o = V_{R1} - V_K \quad for\ v_I \leq V_{R1} - V_K}$$

$$\mathbf{Hence\ slope\ \frac{\Delta v_o}{\Delta v_i} = 0\ \text{---------- (8)}}$$

The diode D_2 conducts for $\mathbf{v_I \geq V_{R2} + V_K}$. The equivalent circuit is shown in Fig.1.11 (b). We can find that;

$$\mathbf{v_o = V_{R2} + V_K\ for\ v_I \geq V_{R2} + V_K}$$

$$\mathbf{Hence\ slope\ \frac{\Delta v_o}{\Delta v_i} = 0\ \text{---------- (9)}}$$

For $\mathbf{(V_{R1} - V_K) < v_i < (V_{R2} + V_K)}$, neither $\mathbf{D_1}$ nor $\mathbf{D_2}$ conducts. The equivalent circuit is shown in Fig.1.11 (c). From the circuit we get;

$$\mathbf{v_o = v_i}$$

$$\mathbf{Hence\ slope\ \frac{\Delta v_o}{\Delta v_i} = 1\ \text{---------- (10)}}$$

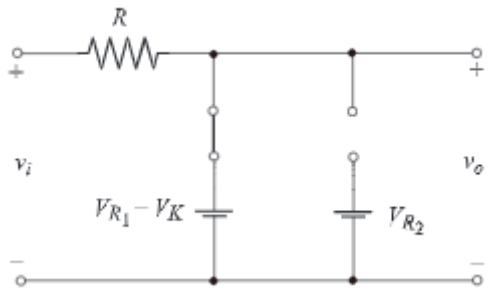


Fig.1.11 (a): Equivalent circuit for $v_I \leq V_{R1} - V_K$

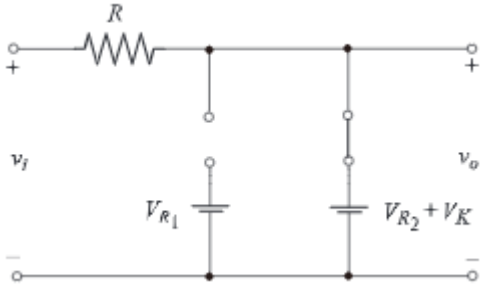


Fig.1.11 (b): Equivalent circuit for $v_I \geq V_{R2} + V_K$

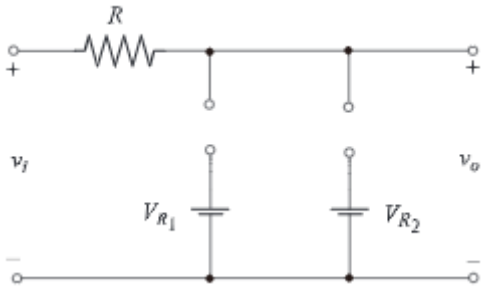


Fig.1.11 (c): Equivalent circuit for (V_{R1} - V_K) < v_i < (V_{R2} + V_K).

Table 1.1: Summary on Operation of Double ended clipper.

Input voltage	*Diode status*	*Output voltage*	*Slope*
$v_i \leq V_{R_1} - V_K$	D_1 on D_2 off	$v_o = V_{R_1} - V_K$	0
$V_{R_1} - V_K < v_i < V_{R_2} + V_K$	D_1 off D_2 off	$v_o = v_i$	1
$v_i \geq V_{R_2} + V_K$	D_1 off D_2 on	$v_o = V_{R_2} + V_K$	0

The transfer characteristics along with output waveforms are shown in Fig.1.12.

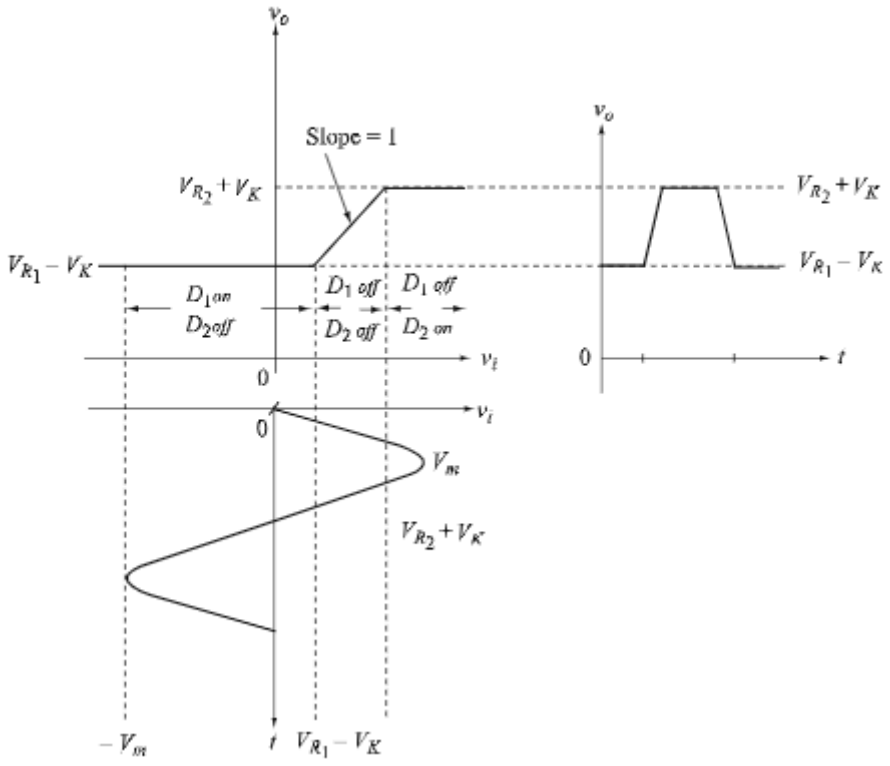


Fig.1.12: Transfer characteristics and output voltage waveform.

1.1.2. Clamping Circuits:

Clamping circuits are used to **add dc level** to the input signal. Clamping circuits are also called as **dc inserters or dc restorers**. Clamping circuits uses **diode, resistor and capacitor**.

A. Negative Clamper:

The circuit of negative clamper is shown in Fig.1.13. A simple negative clamper circuit is used to add a negative level to the ac output. The following assumptions are made while analysing the clamper circuit.

1. The diode is ideal in behaviour.
2. The time constant $\tau = RC$ is designed to very large by selecting large values of **R and C.**

Fig.1.13: Negative clamper circuit.

The input is square wave which swings between the $\pm V_M$ with a period of **T = 1/f.** During the positive half cycle of the input the diode conducts and charges the capacitor. The charging time constant is $\tau_f = r_f C$. Since the diode resistance is very small $\tau_f << T/2$ and hence capacitor gets charged quickly to the peak value V_M of the input signal V_I. The equivalent circuit during diode conduction is shown in Fig.1.14 (a).

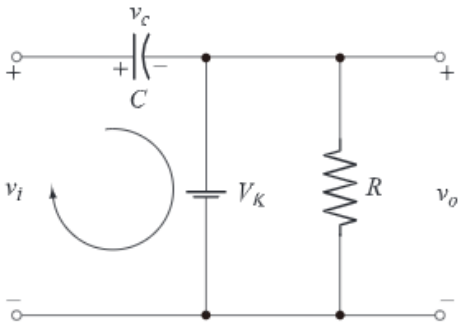


Fig.1.14 (a): Diode is ON

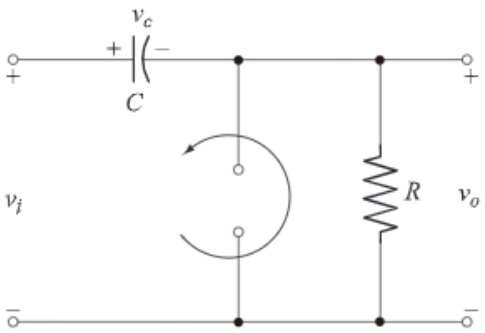


Fig.1.14 (b): Diode is OFF

Apply KVL to the circuit shown in Fig.1.14 (a) we get;

$$v_i - v_c - V_K = 0 \text{ ---------- (11)}$$

$$v_c = V_K - v_i$$

$$\text{When } v_i = V_M;\ v_c = V_K - V_M \text{ ---------- (12)}$$

During the negative half cycle of the input supply, the diode turns off. Now the capacitor discharges into R. The discharge time constant is $\tau = RC$. The capacitor should not loose much of charge during discharge. To meet this requirement, the values of R & C are selected such that $5\tau >> T/2 = 5RC >> T/2$.

The equivalent circuit during the capacitor discharge is shown in Fig.1.14 (b). Apply the KVL for the circuit we get;

$$v_i - v_c - v_o = 0 \text{ ---------- (13)}$$

$$v_o = v_i - v_c$$

$$\text{When } v_c = V_M - V_K;\ v_o = v_i - [V_M - V_K] \text{ ---------- (14)}$$

Table 1.2: Output voltage levels of negative clamper

Input voltage level v_i	*Output voltage level*	
	Practical diode $v_o = v_i - [V_m - V_K]$	*Ideal diode* $v_o = v_i - V_m$
0	$-[V_m - V_K]$	$-V_m$
V_m	V_K	0
$-V_m$	$-2V_m + V_K$	$-2V_m$

The output voltage waveforms of negative clamper circuit are shown in Fig.1.15. From the waveforms we can observe that;

Peak to peak input voltage = peak to peak output voltage = 2 V_M

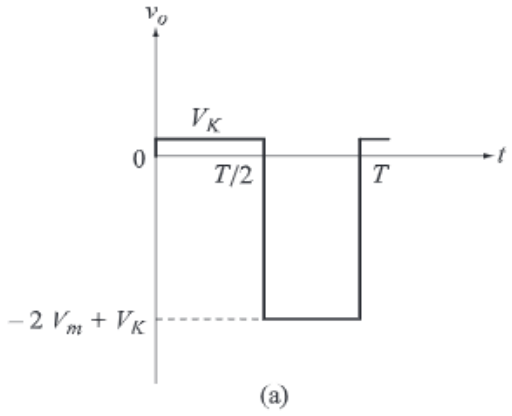


Fig.1.15 (a): Output waveform for Practical diode

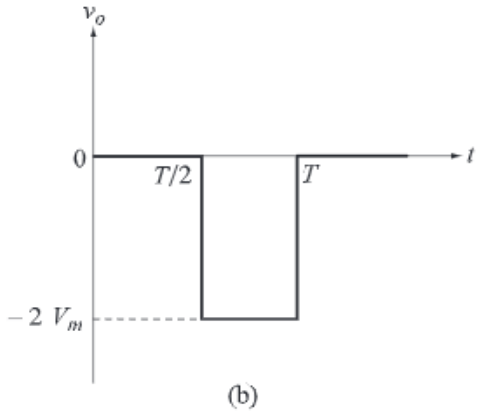


Fig.1.14 (b): Output waveform for Ideal diode

B. Positive Clamper:

The positive clamper circuit is obtained by **reversing the diode** direction in the negative clamper circuit. The positive clamper circuit is shown in Fig.1.16. The positive clamper circuit adds the **positive dc level** to the input signal.

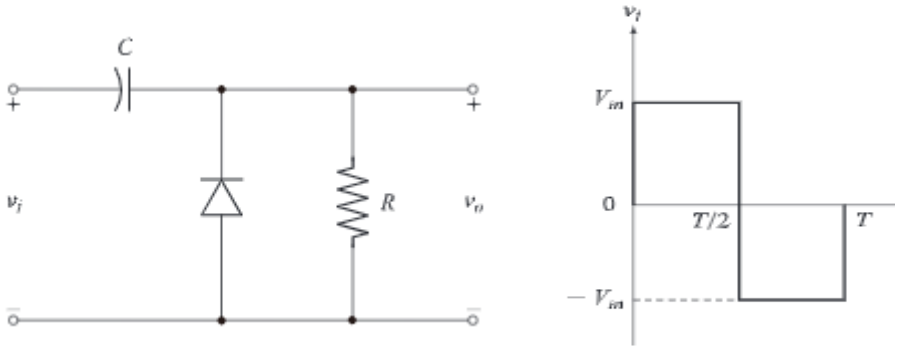


Fig.1.16: Positive clamper circuit

During the negative half cycle of the input supply, the diode gets forward biased and almost instantaneously capacitor gets charged equal to the maximum value V_M of the input signal. The capacitor once charged acts as a battery of voltage V_M. This is because RC time constant is very large hence capacitor holds its entire charge all the time.

In the positive half cycle the diode is reverse biased and the capacitor gets discharging through load resistance. Due to large time constant, it hardly gets discharged during the positive half cycle of the input supply. The waveforms of positive clamper circuit are shown in Fig.1.17.

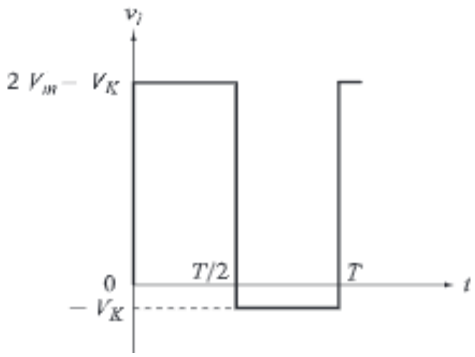


Fig.1.17 (a): Output waveform for Practical diode

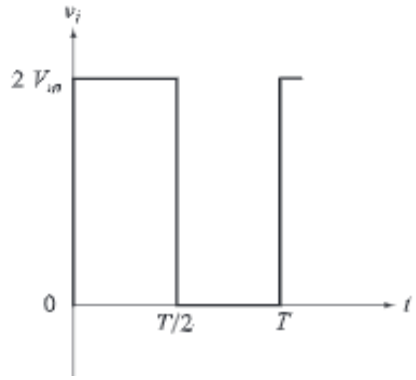


Fig.1.17 (b): Output waveform for Ideal diode

Table 1.3: Output voltage levels of negative clamper

Input voltage level v_i	*Output voltage level*	
	Practical diode $v_o = v_i + [V_m - V_K]$	*Ideal diode* $v_o = v_i + V_m$
0	$V_m - V_K$	V_m
V_m	$2V_m - V_K$	$2V_m$
$-V_m$	$-V_K$	0

1.2. Transistor Biasing and Stabilization

The biasing of a bipolar junction transistor is to establish the desired value of **collector to emitter voltage V_{CE} and Collector current I_C,** to ensure that the amplifier will have proper gain and input impedance with undistorted output voltage swing. **The values of V_{CE} and I_C together are known as operating point or quiescent point (Q-point).** The operating point must be stable for proper operation of the transistor. However, the operating point shifts with changes in transistor parameters such as **β (Current Gain), I_{CO} & V_{BE}**.

1.2.1. Operating Point

The transistor can be operated in three regions cut-off, active and saturation regions. In order to operate transistor in the desired region we have to apply external dc voltages of correct polarity and magnitude to the two junctions of the transistor. This is nothing but the biasing of the transistor. Let us consider the common emitter configuration of NPN transistor and its output characteristics as shown in Fig.1.18.

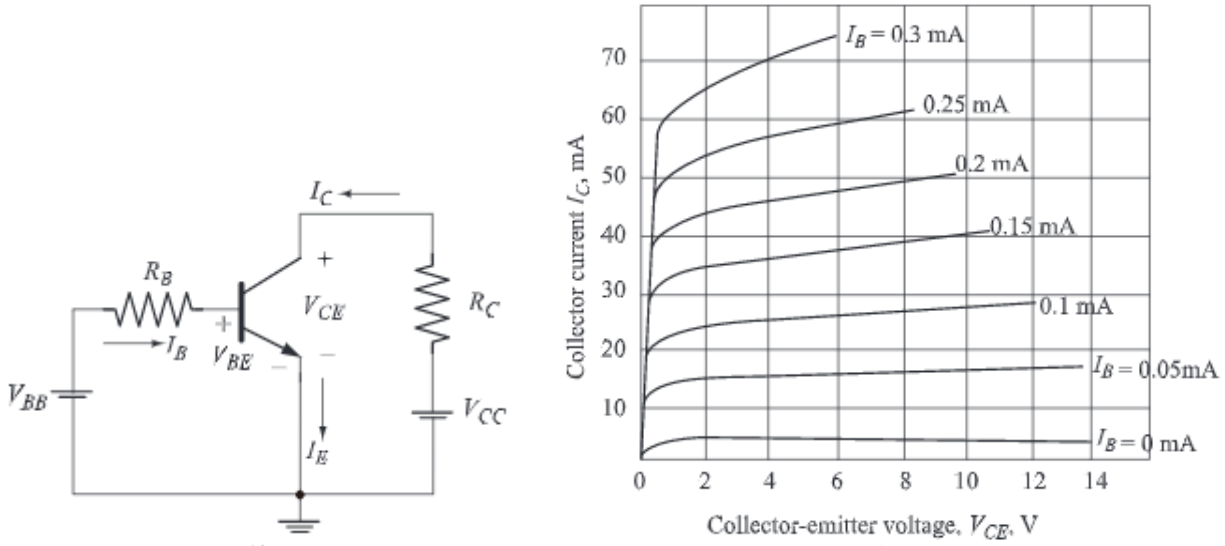


Fig.1.18: Common-Emitter configuration and its output characteristics.

The region in the characteristics above I_B = 0 mA and to the right of the few tenths of volts of V_{CE} is the active region. In this region the collector current increases with increase in the base current. The base-emitter junction is forward biased and base-collector junction is reverse biased in this region.

The region where the base-emitter junction is reverse biased below 0.1V for germanium and below 0V for silicon is the cut-off region. In this region base-emitter junction and base-collector junction is reverse biased. The emitter current is zero and the transistor is non-conducting in this region.

The region very close to V_{CE} = 0 where all curves appear to merge and fall rapidly to the origin is called saturation region. In this region base-emitter and base-collector junctions are forward biased. The collector current is considerably large and V_{CE} is few tenths of volts.

The transistor is required to be biased from cut-off to saturation and vice-versa when it is being used as a switch. It must be biased in the active region when it is being used as an amplifier. The transistor functions linearly when its operation is restricted to the active region.

There are several circuit configurations through which the transistor current and voltage can be adjusted in order to fix the operating point. Fixed bias, emitter bias or self-bias and voltage divider bias are some configurations.

1.2.2. Fixed Bias Configuration:

The fixed bias circuit is shown in Fig.1.19 (a). It is the simplest dc bias configuration. For the dc analysis we can replace capacitor with an open circuit (since capacitor blocks dc) because the reactance of capacitor is infinity. The dc equivalent circuit is shown in Fig.1.19 (b).

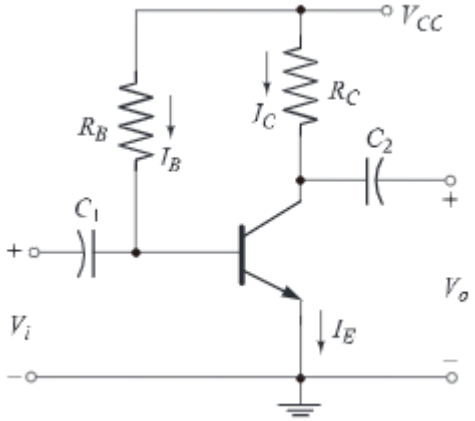


Fig.1.19 (a): Fixed bias circuit

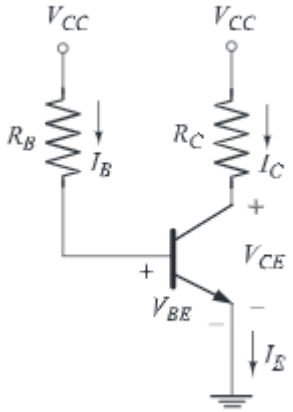


Fig.1.19 (b): DC equivalent circuit of fixed bias

Apply KVL to the base circuit we get;

$$\mathbf{V_{CC} - I_B R_B - V_{BE} = 0}$$

$$\boldsymbol{I_B = \frac{V_{CC} - V_{BE}}{R_B}} \text{ ---------- (15)}$$

The magnitudes of collector current and base current neglecting I_{CO} are related by,

$$\mathbf{I_C = \beta I_B} \text{ ---------- (16)}$$

Where, β = dc current gain of Common Emitter configuration. I_B is decided by R_B and I_C is decided by β. Thus R_C has no role in the value of I_C when the transistor is in active region.

Applying KVL to the circuit shown in Fig.1.19 (a) we get;

$$\mathbf{V_{CC} = I_C R_C + V_{CE}}$$

$$\mathbf{V_{CE} = V_{CC} - I_C R_C} \text{ ---------- (17)}$$

The transistor circuit operating in saturation region is shown in Fig.1.19 (c). Apply KVL to the circuit we get;

$$V_{CC} - I_{C(sat)}R_C - V_{CE(sat)} = 0$$

$$I_{C(sat)} = \frac{V_{CC} - V_{CE(sat)}}{R_C} \text{ --------- (18)}$$

But $V_{CE(sat)} \approx 0$

$$I_{C(sat)} \approx \frac{V_{CC}}{R_C} \text{ ---------- (19)}$$

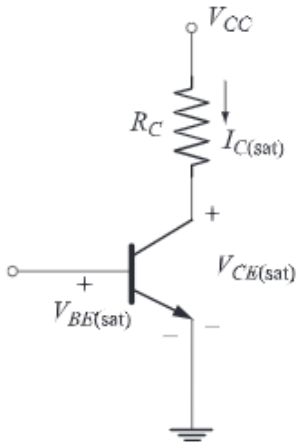
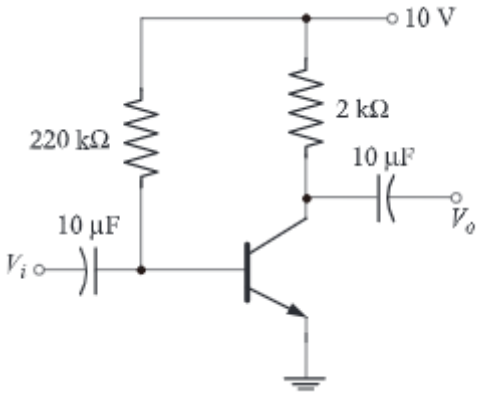


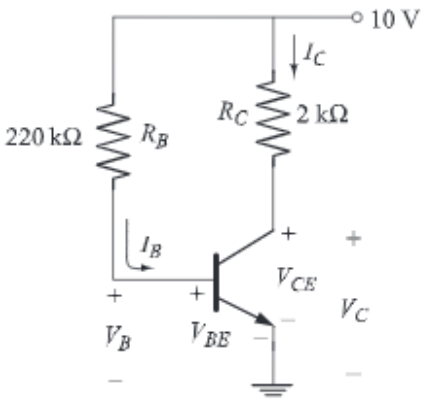
Fig.1.19 (c): Transistor operating in Saturation region.

Solved Examples:

1. **For the fixed bias circuit shown, assuming VBE = 0.7V and β = 60 find:**
   - **a. Quiescent values of base and collector currents.**
   - **b. Quiescent value of V_{CE}.**
   - **c. Base-ground and collector-ground voltages.**
   - **d. Base-collector voltage**
   - **e. Quiescent values of I_C and V_{CE} for β = 110.**



Solution: Consider the coupling capacitors as open circuit and mention various currents and voltages in the circuit as shown below.



a. Quiescent values of base current and collector current.

$$I_{BQ} = \frac{V_{CC} - V_{BE}}{R_B} = \frac{10\,\text{V} - 0.7\,\text{V}}{220\,\text{kW}} = 42.27\ \mu\text{A}$$

$$I_{CQ} = \beta I_{BQ} = 60 \times 42.27\ \mu\text{A} = 2.54\ \text{mA}$$

b. Quiescent value of V_{CE}.

$$V_{CC} = I_C R_C + V_{CE}$$

$$V_{CEQ} = V_{CC} - I_{CQ} R_C = 10 - (2.54\ \text{mA})(2\ \text{k}\Omega) = 4.92\ \text{V}$$

c. Base and collector voltages with respect to ground.

$$V_B = V_{BE} = 0.7\ \text{V}$$

$$V_C = V_{CE} = 4.92\ \text{V}$$

d. Base-collector voltage.

$$V_{BC} = V_B - V_C = 0.7\ \text{V} - 4.92\ \text{V} = -4.22\ \text{V}$$

e. When β = 110.

I_{BQ} is not affected by change in β.

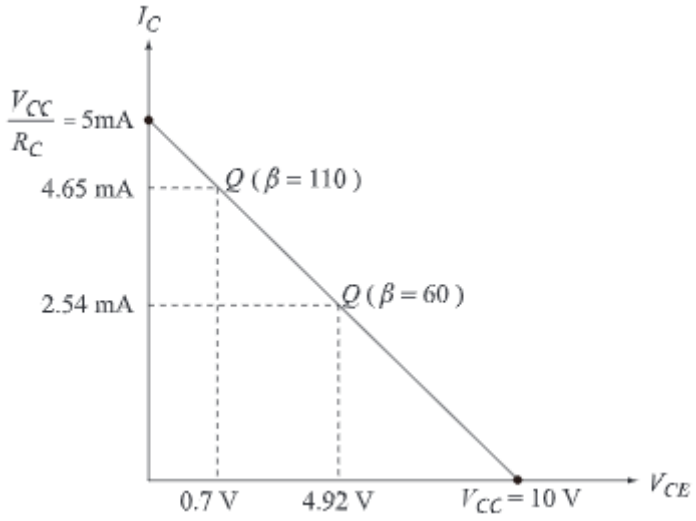
$$I_{BQ} = 42.27\ \mu\text{A} \quad \text{[as obtained in part (a)]}$$

$$I_{CQ} = \beta I_{BQ} = 110 \times 42.27\ \mu\text{A} = 4.65\ \text{mA}$$

$$V_{CEQ} = V_{CC} - I_{CQ} R_C = 10\ \text{V} - (4.65\ \text{mA} \times 2\ \text{k}\Omega) = 0.7\ \text{V}$$

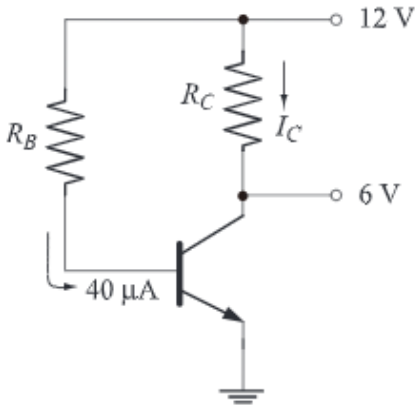
β	I_{BQ}	I_{CQ}	V_{CEQ}
60	42.27 μA	2.54 mA	4.92 V
110	42.27 μA	4.65 mA	0.7 V

The Q-points are indicated in the dc load line as shown in the figure.



Observe that when β changes from 60 to 110, the Q-point shift from the middle of the active region to near saturation region. Therefore the fixed bias circuit has very poor stability of operating point.

2. **For the fixed bias circuit shown, find collector current, collector resistance, base resistance and V_{CE}. Assume β = 80 and V_{BE} = 0.7V**



Solution:

Collector current:

$$I_C = \beta I_B = (80)\ (40\ \mu A) = 3.2\ mA$$

Collector resistance:

$$V_C = 6\ V$$

$$V_{CE} = V_C = 6\ V$$

$$R_C = \frac{V_{CC} - V_{CE}}{I_C} = \frac{12\,V - 6\,V}{3.2\,mA} = 1.875\ k\Omega$$

Base Resistance:

$$R_B = \frac{V_{CC} - V_{BE}}{I_B} = \frac{12\,\text{V} - 0.7\,\text{V}}{40\,\mu\text{A}} = 282.5\,\text{k}\Omega$$

V_{CE} = Voltage from collector to emitter
$= V_C = 6$ V.

1.2.3. Emitter Stabilized Bias Configuration

To improve the stability of the biasing circuit over a fixed bias circuit, the emitter resistance is connected in the biasing circuit. Such biasing circuit is known as **emitter bias circuit.** The circuit of emitter bias configuration is shown in Fig.1.20 (a).

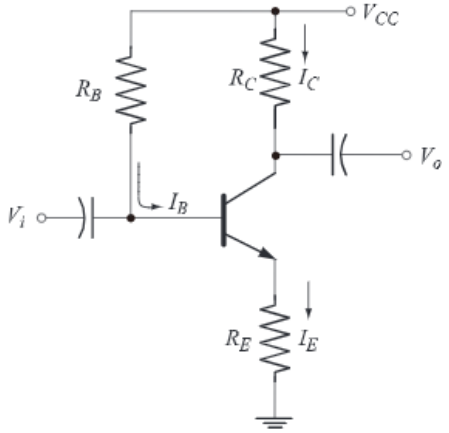


Fig.1.20 (a): Emitter Bias Circuit.

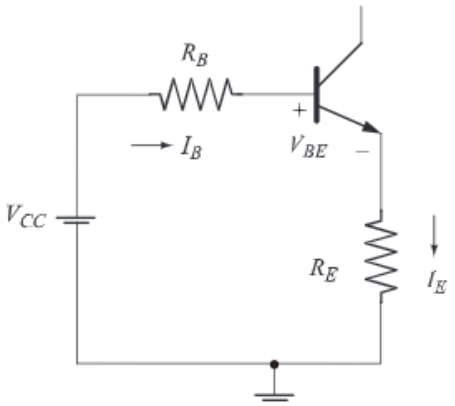


Fig.1.20 (b): Base-Emitter Circuit.

Circuit Analysis: The base emitter circuit is shown in Fig.1.20 (b)**.** Applying KVL to the base-emitter circuit we get;

$$V_{CC} = I_B R_B + V_{BE} + I_E R_E$$
$$I_E = I_C + I_B \qquad \text{---------- (20)}$$

Using $I_C = \beta I_B$;

$$I_E = \beta I_B + I_B$$
$$I_E = (\beta + 1) I_B \qquad \text{---------- (21)}$$

$$V_{CC} = I_B R_B + V_{BE} + (\beta + 1) I_B R_E$$
$$V_{CC} - V_{BE} = I_B [R_B + (\beta + 1) R_E]$$
$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1) R_E} \qquad \text{------- (22)}$$

The collector-emitter circuit is shown in Fig.1.20 (c).

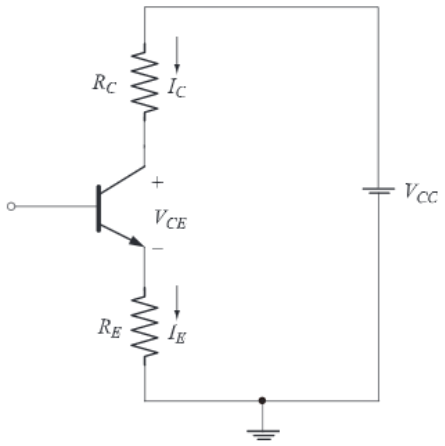


Fig.1.20 (c): Collector-Emitter Circuit

Applying KVL to the collector-emitter circuit we get;

$$V_{CC} = I_C R_C + V_{CE} + I_E R_E \quad \text{---------- (22)}$$

Substituting $I_E = I_C$.

$$V_{CE} = V_{CC} - I_C (R_C + R_E) \quad \text{---------- (23)}$$

Let,

V_C = Voltage from collector to ground

V_B =Voltage from base to ground

V_E = Voltage from emitter to ground

Therefore, V_E = Voltage across R_E

$$V_E = I_E R_E \quad \text{---------- (24)}$$

$$V_C = V_{CE} + V_E$$
$$= V_{CE} + I_E R_E \quad \text{-------- (25)}$$

From equation 22, Substitute for (V_{CE}+$I_E R_E$) we get;

$$V_B = V_{CC} - I_B R_B \quad \text{--------- (26)}$$

Saturation Level: When transistor is in saturation

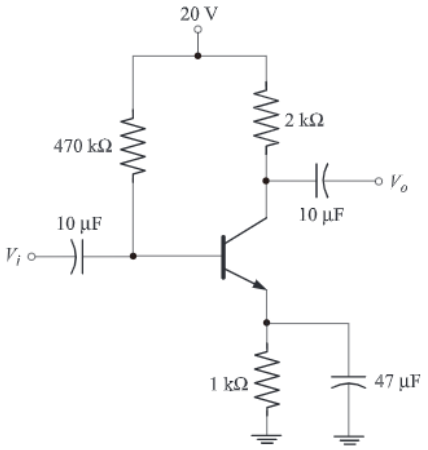
$$V_{CE} = V_{CE\,(sat)} \approx 0\ \text{V}$$
$$I_C = I_{C\,(sat)}$$

Substituting this condition in equation 22 and taking $I_E = I_C$ we have;

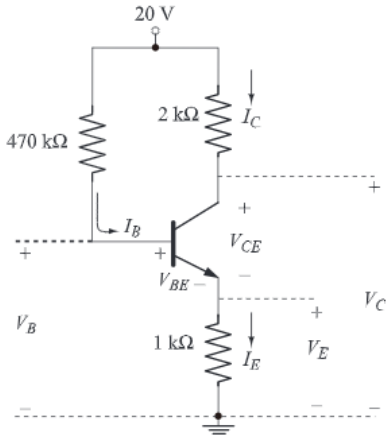
$$V_{CC} = I_{C\,(sat)}\,[R_C + R_E]$$
$$I_{C\,(sat)} = \frac{V_{CC}}{R_C + R_E} \qquad \text{---------- (27)}$$

Solved Examples:

1. **For the emitter-bias shown using silicon transistor with VBE = 0.7 V and β = 60, find;**
   a. **Base current and collector current**
   b. **Collector-Emitter voltage**
   c. **Collector, emitter and base voltages to ground**
   d. **Base-collector voltage**



Solution: For dc analysis the capacitors are acts as open circuit.



a. Base current and collector current

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (1+\beta)R_E} = \frac{20 - 0.7}{470k + (1+60)1k} = \mathbf{36.34\mu A}$$

$I_C = \beta I_B = 60 * 36.34\ \mu =$ **2.18 mA**

b. Collector-emitter voltage

$$\begin{aligned} V_{CE} &= V_{CC} - I_C (R_C + R_E) \\ &= 20\ \text{V} - 2.18\ \text{mA}\ [2\ \text{k}\Omega + 1\ \text{k}\Omega] \\ &= 13.46\ \text{V} \end{aligned}$$

c. Collector, emitter and base voltages to ground

$$V_C = V_{CC} - I_C R_C = 20\ \text{V} - (2.18\ \text{mA} \times 2\ \text{k}\Omega) = 15.64\ \text{V}$$

$$V_E = V_C - V_{CE} = 15.64\ \text{V} - 13.46\ \text{V} = 2.18\ \text{V}$$

$$V_B = V_{BE} + V_E = 0.7\ \text{V} + 2.18\ \text{V} = 2.88\ \text{V}$$

d. Base-collector voltage

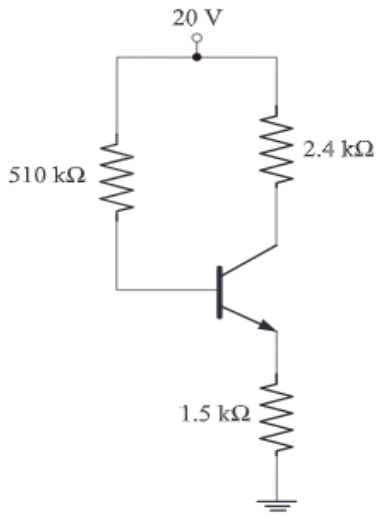
$$\mathbf{V_{BC} = V_B - V_C}$$

$$\mathbf{V_{BC} = 2.88 - 15.64 = -12.76\ V}$$

2. For the emitter bias circuit shown using silicon transistor VBE = 0.7 V and β = 100. Find;

a. Quiescent values of base current, collector current and collector to emitter voltage.

b. Voltage at collector, base and emitter with respect to ground.



Solution:

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (1+\beta)R_E} = \frac{20 - 0.7}{510k + (1+100)1.5k} = \mathbf{29.18\mu A}$$

$I_C = \beta I_B = 100 * 29.18\ \mu =$ **2.92 mA**

$V_{CE} = V_{CC} - I_C\ (R_C + R_E) = 20 - 2.92m\ (2.4k + 1.5k) =$ **8.61V**

$V_E = I_E R_E = [I_B + I_C]\ R_E = [29.18\mu + 2.92\ m]\ 1.5k =$ **4.42V**

$V_B = V_{BE} + V_E = 0.7 + 4.42 =$ **5.12V**

1.2.4. Voltage Divider Bias Configuration

In the fixed bias and the emitter bias circuits, the collector current and collector-emitter voltage that is operating point is a function of **dc current gain β** of the transistor. The current gain is sensitive to **temperature and its value keeps varying**. A biasing circuit independent or less dependent on β such as the **voltage divider bias circuit** is desirable. The voltage divider circuit is shown in Fig.1.21 (a).

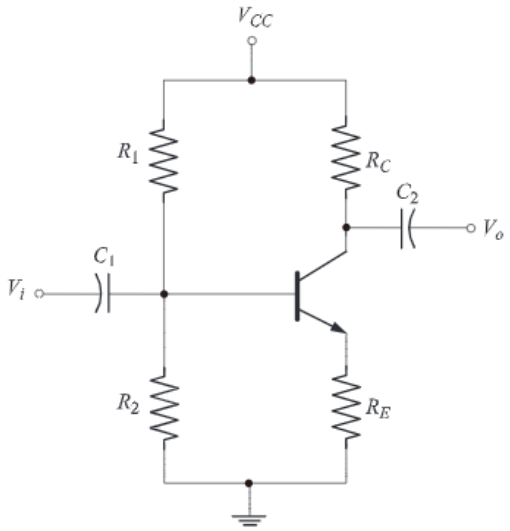


Fig.1.21 (a): Voltage divider bias circuit

Exact Analysis: The base circuit is redrawn as shown in Fig.1.21 (b) for the dc analysis. The Thevenin equivalent circuit is shown in Fig.1.22 (a).

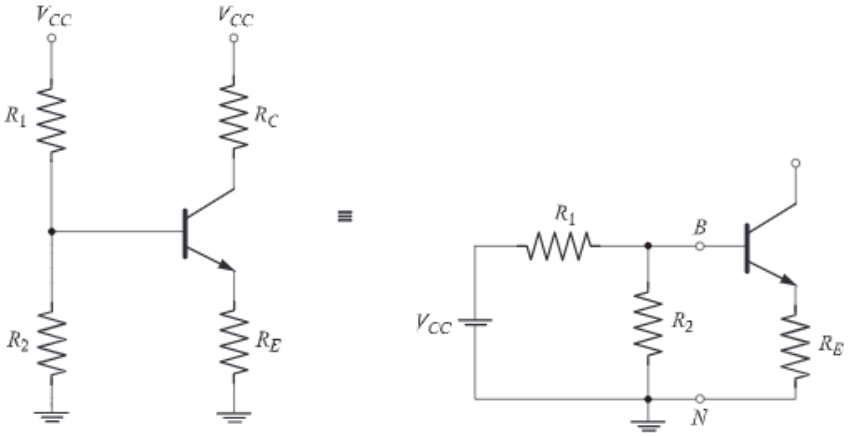


Fig.1.21 (b): Base circuit of Voltage divider bias configuration

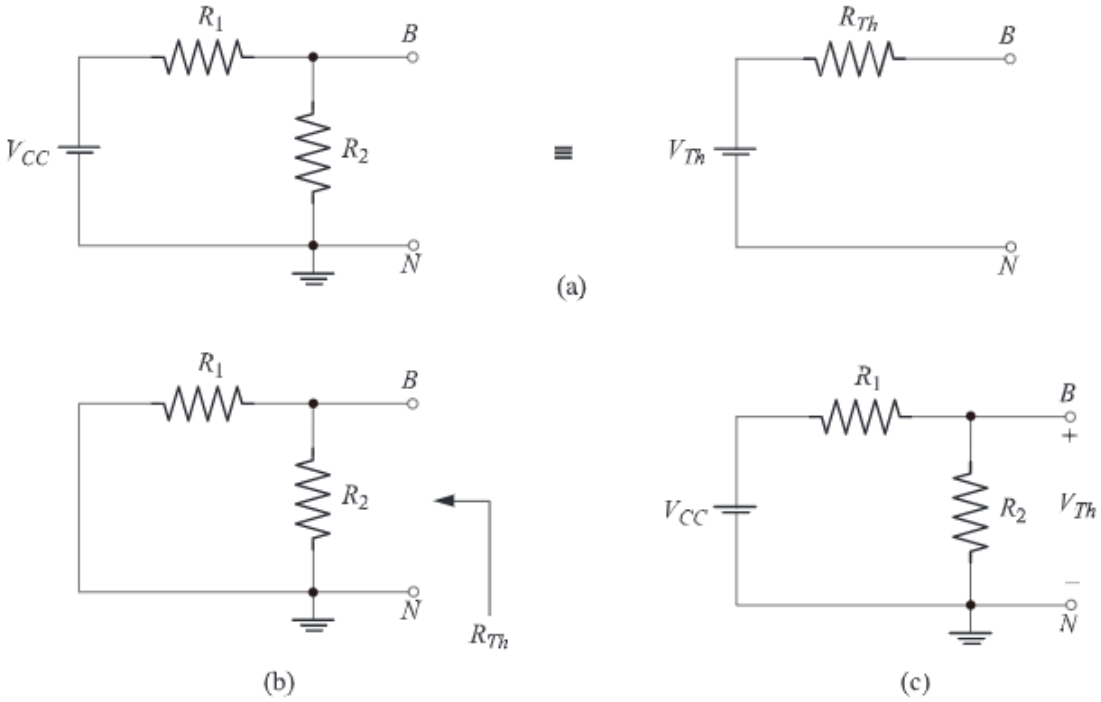


Fig.1.22: a. Thevenin Equivalent b. Determination of R_{Th} c. Determination of V_{Th}

To find Thevenin resistance R_{Th}, V_{CC} is reduced to zero in the circuit of Fig.1.22 (a). The resulting circuit is shown in Fig.1.22 (b).

$$R_{Th} = R_1 \| R_2$$

$$R_{Th} = \frac{R_1 R_2}{R_1 + R_2}$$

From the Fig.1.22 (c), the Thevenin Voltage can be obtained,

$$V_{Th} = V_{CC} \frac{R_2}{R_1 + R_2}$$

The circuit shown in Fig.1.21 (b) can be redrawn as shown in Fig.1.23 after substituting the Thevenin equivalent between B and N.

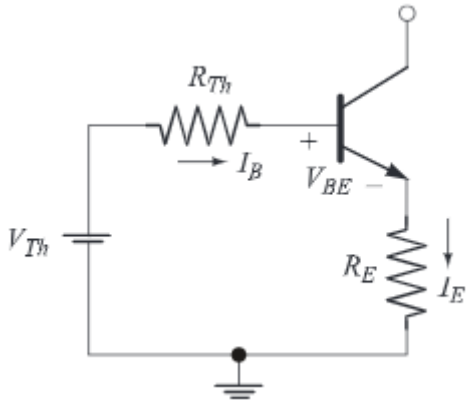


Fig.1.23: Base circuit with Thevenin Equivalent

Apply KVL to the base circuit shown in Fig.1.23 we get;

$$V_{Th} - I_B R_{Th} - V_{BE} - I_E R_E = 0$$

$$V_{Th} = I_B R_{Th} + V_{BE} + I_E R_E \quad \text{_____ (28)}$$

$$\text{Now, } I_E = I_C + I_B \quad \text{_____ (29)}$$

$$\mathbf{I_C = \beta I_B}$$

Substituting in equation 29 we get

$$\mathbf{I_E = \beta I_B + I_B = (1+\beta) I_B} \quad \text{_____ (30)}$$

$$V_{Th} = I_B R_{Th} + V_{BE} + (1+\beta) I_B R_E$$

$$V_{Th} - V_{BE} = I_B [R_{Th} + (1+\beta) R_E]$$

$$\boldsymbol{I_B = \frac{V_{Th} - V_{BE}}{R_{Th} + (1+\beta) R_E}} \quad \text{_____ (31)}$$

The collector circuit is shown in Fig.1.24. Apply KVL to the circuit we get;

$$V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0$$

$$V_{CC} = I_C R_C + V_{CE} + I_E R_E$$

$$I_E = I_C$$

$$\mathbf{V_{CE} = V_{CC} - I_C(R_C + R_E)} \quad \textbf{(32)}$$

Voltage across emitter:

$$V_E = I_E R_E \quad (33)$$

Collector to ground Voltage:

$$V_C = V_{CE} + I_E R_E = V_{CE} + V_E \quad (34)$$

Base to ground Voltage:

$$V_B = V_{BE} + V_E \quad (35)$$

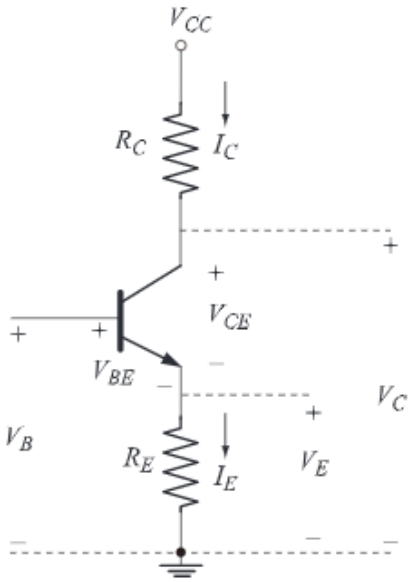


Fig.1.24: Collector circuit of Voltage Divider Bias Configuration

Transistor Saturation: When transistor is in saturation, $V_{CE} = V_{CE(sat)} \approx 0$ and $I_C = I_{C(sat)}$. From equation (32) we get;

$$V_{CC} = I_{C(sat)}[R_C + R_E]$$

$$\boldsymbol{I_{C(sat)} = \frac{V_{CC}}{R_C + R_E}} \quad \textbf{(36)}$$

Approximate Analysis:

The resistance R_E in the emitter circuit gets reflected as $\mathbf{(1+\beta)R_E}$ in the base circuit. Therefore the circuit between base and ground of Fig.1.21 (b) can be replaced by an equivalent resistance $\mathbf{R_i = (1+\beta)R_E}$ as shown in Fig.1.25.

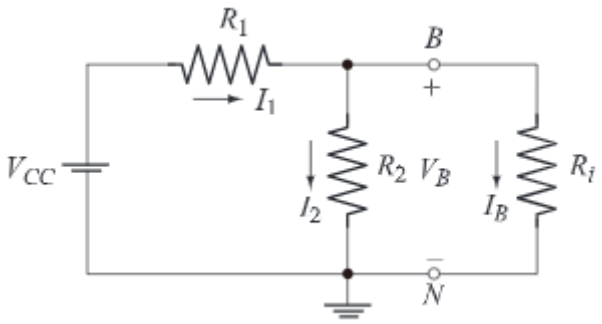


Fig.1.25: Input circuit of Approximate Analysis

Apply KCL to the above circuit we get;

$$I_1 = I_2 + I_B$$

$$R_i = (1+\beta)\, R_E \approx \beta R_E, \quad \text{since } \beta >> 1$$

$$I_B = \frac{V_B}{R_i} \quad and \quad I_2 = \frac{V_B}{R_2}$$

If $\mathbf{R_i = (1+\beta)\, R_E >> 10\, R_2}$, _____ (37)

Then $I_B << 0.1 * I_2$, We neglect I_B, as a result we get;

$$\mathbf{I_1 \approx I_2}$$

Apply KVL to the above circuit we get;

$$V_{CC} = I_1R_1 + I_2R_2$$

$$V_{CC} = I_2(R_1+R_2)$$

$$I_2 = \frac{V_{CC}}{R_1 + R_2}$$

$$V_B = I_2 * R_2$$

$$\boldsymbol{V_B = \frac{V_{CC}R_2}{R_1+R_2}} \quad \text{\_\_\_\_\_ (38)}$$

$$V_B = V_{BE} + V_E$$

$$V_E = V_B - V_{BE}$$

The emitter current IE is given by;

$$I_E = \frac{V_E}{R_E}$$

And $I_C \approx I_E$

From KVL equation of collector-emitter circuit we get;

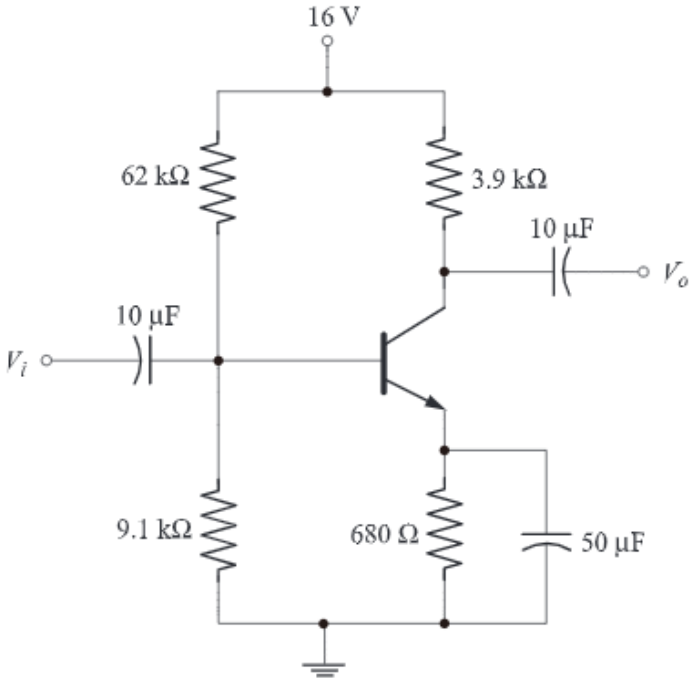
$$V_{CE} = V_{CC} - I_C R_C - I_E R_E$$

$$\mathbf{V_{CE} = V_{CC} - I_C (R_C + R_E)} \quad \text{(39)}$$

Solved Examples:

Example 1:

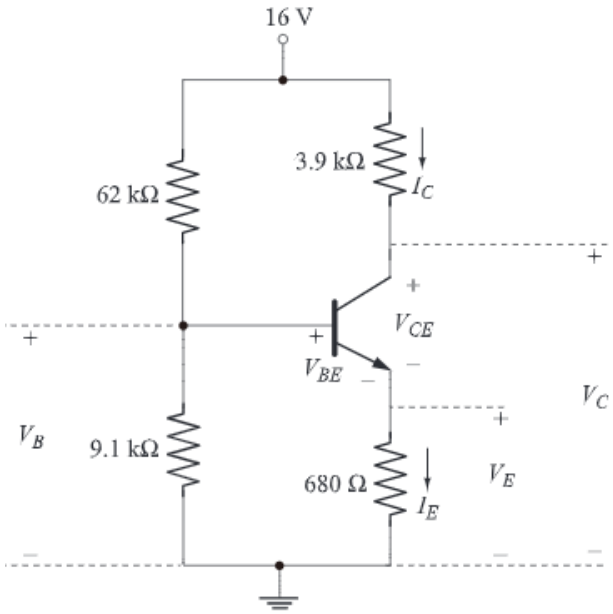
a. **Find the quiescent base current, collector current and V_{CE} for the circuit shown using silicon transistor with V_{BE} = 0.7V and β = 80.**
b. **Determine the values of collector, emitter and base voltages with respect to ground.**
c. **Repeat (a) for β = 150.**
d. **Draw the dc load line and locate the Q-points corresponding to two 'β' values.**



Solution:

Given Data: **V_{CC} = 16V, R_1 = 62kΩ, R_2 = 9.1k Ω, R_C = 3.9k Ω, R_E = 680 Ω, C_1 = C_2 = 10μF, C_E = 50μF, V_{BE} = 0.7V and β = 80.**

The dc equivalent circuit is shown below.



a. Base current, Collector current and Collector-Emitter Voltage.

$$R_{Th} = \frac{R_1 R_2}{R_1 + R_2} = \frac{62k * 9.1k}{62k + 9.1k} = \mathbf{7.94}\boldsymbol{k}\Omega$$

$$V_{Th} = \frac{V_{CC} R_2}{R_1 + R_2} = \frac{16 * 9.1k}{62k + 9.1k} = \mathbf{2.05}\boldsymbol{V}$$

$$I_B = \frac{V_{Th} - V_{BE}}{R_{Th} + (1+\beta)R_E} = \frac{2.05 - 0.7}{7.94k + (1+80)680} = \mathbf{21.42}\mu\boldsymbol{A}$$

$I_C = \beta I_B = 80 * 21.42\ \mu =$ **1.71 mA**

$V_{CE} = V_{CC} - I_C (R_C + R_E) = 16 - 1.71m\ (3.9k+680) =$ **8.17V**

b. Collector, emitter and base voltages with respect to ground.

$V_C = V_{CC} - I_C R_C = 16 - (1.71m * 3.9k) =$ **9.33 V**

$V_E = I_E R_E \approx I_C R_C = (1.71m * 3.9k) =$ **1.16 V**

$V_B = V_{BE} + V_E = 0.7 + 1.16 =$ **1.86V**

c. For β = 150: Base current, Collector current and Collector-Emitter Voltage.

$$I_B = \frac{V_{Th} - V_{BE}}{R_{Th} + (1+\beta)R_E} = \frac{2.05 - 0.7}{7.94k + (1+150)680} = \mathbf{12.2}\mu\boldsymbol{A}$$

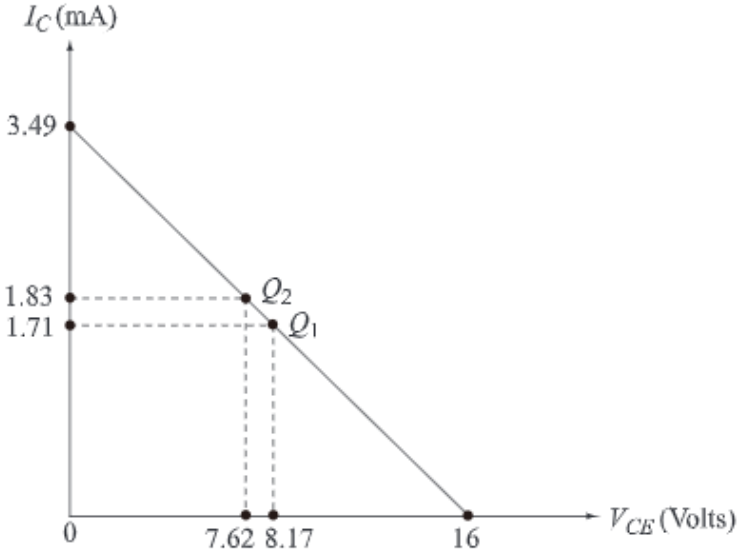
$I_C = \beta I_B = 150 * 12.2\ \mu =$ **1.83 mA**

$V_{CE} = V_{CC} - I_C (R_C + R_E) = 16 - 1.83m\ (3.9k+680) =$ **7.62V**

d. DC load line curve:

$$I_{C(sat)} = \frac{V_{CC}}{R_C + R_E} = \frac{16}{3.9k + 680} = \mathbf{3.49mA}$$

β	I_{BQ}	I_{CQ}	V_{CEQ}
80	21.42 µA	1.71 mA	8.17 V
150	12.2 µA	1.83 mA	7.62 V



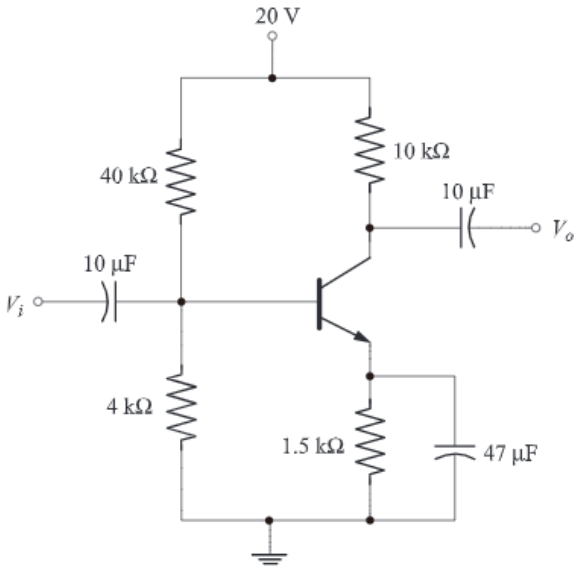
DC load line curve

Example 2:

For the voltage divider bias configuration shown below, Find

a. **IC and VCE using exact analysis**
b. **IC and VCE using approximate analysis**
c. **IC(sat)**
d. **Compare the results obtained in (a) and (b) and comment**

Assume silicon transistor with β = 150.



Solution:

Given Data: **V_{CC} = 20V, R_1 = 40kΩ, R_2 = 4k Ω, R_C = 10k Ω, R_E = 1.5k Ω, C_1 = C_2 = 10μF, C_E = 47μF, V_{BE} = 0.7V and β = 150.**

a. **Exact Analysis:**

$$R_{Th} = \frac{R_1 R_2}{R_1 + R_2} = \frac{40k * 4k}{40k + 4k} = \mathbf{3.63}\boldsymbol{k}\Omega$$

$$V_{Th} = \frac{V_{CC} R_2}{R_1 + R_2} = \frac{20 * 4k}{40k + 4k} = \mathbf{1.82}\boldsymbol{V}$$

$$I_B = \frac{V_{Th} - V_{BE}}{R_{Th} + (1+\beta)R_E} = \frac{1.82 - 0.7}{3.63k + (1+150)1.5k} = \mathbf{4.86}\mu\boldsymbol{A}$$

$I_C = \beta I_B = 150 * 4.86\ \mu =$ **0.729 mA**

$V_{CE} = V_{CC} - I_C (R_C + R_E) = 20 - 0.729m\ (10k+1.5k) =$ **11.62V**

b. Approximate Analysis:

$\beta R_E = 150*1.5k = \mathbf{225k\Omega}$

$10R_2 = 10*4k = \mathbf{40k\Omega}$

Note that $\beta R_E > 10R_2$, hence we can use approximate analysis.

$$V_B = \frac{V_{CC}R_2}{R_1+R_2} = \mathbf{1.82\,V} \quad \text{(Same as } V_{Th}\text{)}$$

$V_E = V_B - V_{BE} = 1.82 - 0.7 = \mathbf{1.12\ V}$

$$I_E = \frac{V_E}{R_E} = \frac{1.12}{1.5k} = \mathbf{0.746\,mA}$$

$$\mathbf{I_C \approx I_E}$$

$V_{CE} = V_{CC} - I_C\,(R_C+R_E) = 20 - 0.746m\,(10k+1.5k) = \mathbf{11.42V}$

c.

$$I_{C(sat)} = \frac{V_{CC}}{R_C + R_E} = \frac{20}{10k + 1.5k} = \mathbf{1.74mA}$$

d. The results of exact and approximate analysis are compared in the following table.

Parameter	*Exact analysis*	*Approximate analysis*
I_C	0.729 mA	0.746 mA
V_{CE}	11.62 V	11.42 V

1.2.5. Transistor Switching Networks and Switching Characteristics

To operate BJT as s switch, it is to be operated in two regions namely, **cut-off and saturation region**. In cut-off region both the junctions are reverse biased and only reverse current flows which is very small and can be neglected. Thus no current flows through transistor in cut-off region, hence it acts as **open switch**. (Figure.1.26)

In saturation region both the junctions are forward biased. The voltage V_{CE} drops to very small value about **0.2V to 0.3V**. The collector current is very large and controlled by external resistance in collector circuit. Thus the transistor acts as a **closed switch.** (Figure 1.27)

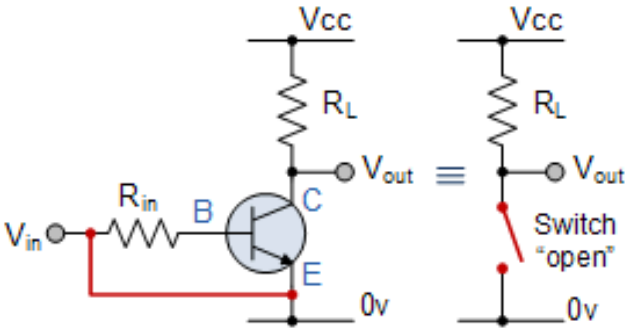


Fig.1.26: Cut-off region (Open switch)

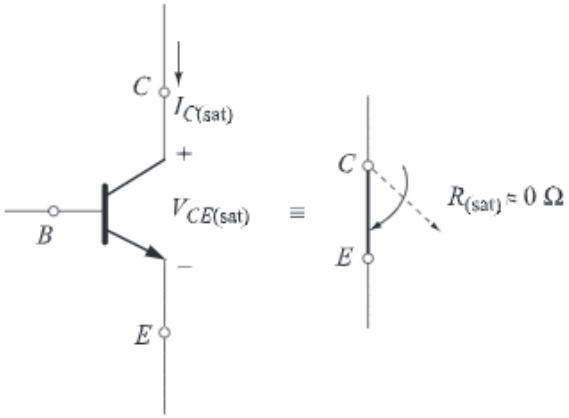


Fig.1.27: Saturation region (Closed switch)

Switching Characteristics:

When the base current is applied, the transistor does not switch on immediately. This is because of **junction capacitance and the transition time of electrons** across the junctions. The time between the application of input pulse and the commencement of current flow is termed as **delay time, T_d.** The time required for the collector current to reach **90% of its maximum level** from 10% level is called **rise time, T_r.** The turn-on time is the addition of rise time and delay time **($T_{on} = T_d + T_r$)**.

When the input current is switched off, the collector current does not go to zero level immediately. It goes to zero level after turn-off time, **which is the sum of storage time T_s, and fall time T_f.** The fall time is specified as the time required for collector current to go from 90% to 10% of its maximum level. **The switching characteristic of transistor is shown in figure 1.28.**

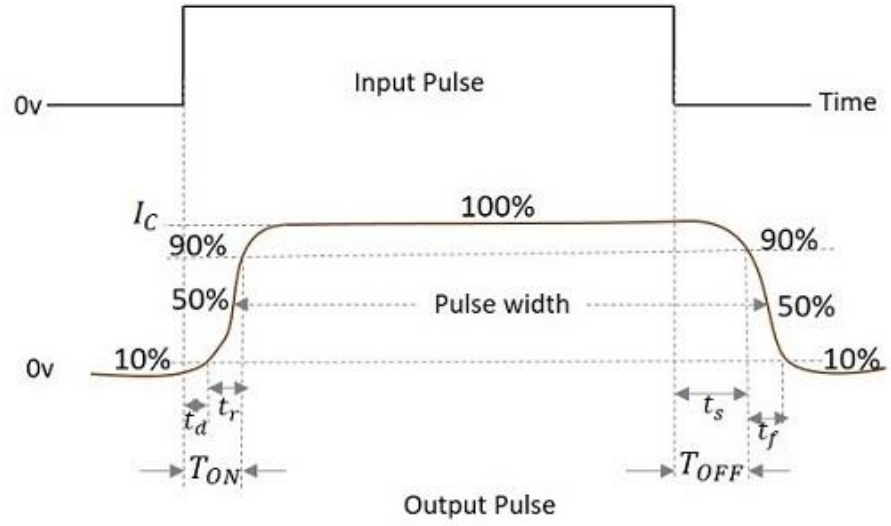


Fig.1.28: Transistor switching characteristics

1.2.6. Stability factors

The operating point of the transistor is affected by the parameters **reverse leakage current I_{CO}, current gain β and Base-emitter voltage drop V_{BE}** with variation in temperature. The transistor biasing circuits are to provide stability of collector current against the variations in I_{CO}, β and V_{BE}. The stability factor indicates the **degree of change in operating point due to variation in temperature.**

$$\boldsymbol{S(I_{CO})} = \frac{\boldsymbol{\partial I_C}}{\boldsymbol{\partial I_{CO}}} = \frac{\boldsymbol{\Delta I_C}}{\boldsymbol{\Delta I_{CO}}}$$, β and V_{BE} are constant

$$\boldsymbol{S(V_{BE})} = \frac{\boldsymbol{\partial I_C}}{\boldsymbol{\partial V_{BE}}} = \frac{\boldsymbol{\Delta I_C}}{\boldsymbol{\Delta V_{BE}}}$$, β and I_{CO} are constant

$$\boldsymbol{S(\beta)} = \frac{\boldsymbol{\partial I_C}}{\boldsymbol{\partial \beta}} = \frac{\boldsymbol{\Delta I_C}}{\boldsymbol{\partial \beta}}$$, V_{BE} and I_{CO} are constant

Stability factor (S_{ICO}): General expression

For common emitter configuration;

$$\mathbf{I_C = I_{CEO} + \beta * I_B}$$

$$\mathbf{I_C = (1+\beta) I_{CBO} + \beta * I_B}$$

When I_{CBO} changes by ∂I_{CBO}, I_B changes by ∂I_B and I_C changes by ∂I_C we get;

$$\boldsymbol{\partial I_C = (1+\beta)\, \partial I_{CBO} + \beta * \partial I_B}$$

$$1 = (1+\beta)\frac{\partial I_{CBO}}{\partial I_C} + \beta * \frac{\partial I_B}{\partial I_C}$$

$$1 - \beta * \frac{\partial I_B}{\partial I_C} = (1+\beta)\frac{\partial I_{CBO}}{\partial I_C}$$

$$\frac{\partial I_{CBO}}{\partial I_C} = [1 - \beta * \frac{\partial I_B}{\partial I_C}] \ / (1+\beta)$$

$$S(I_{CO}) = \frac{\partial I_C}{\partial I_{CO}} = \frac{(1+\beta)}{1-\beta\frac{\partial I_B}{\partial I_C}} \text{ ---------- (40)}$$