ATME COLLEGE OF ENGINEERING

13th Km Stone, Bannur Road, Mysore - 570028

DEPARTMENT OF ELECTRICAL & ELECTRONICS ENGINEERING

(ACADEMIC YEAR 2024-25)

LABORATORY MANUAL

BEE303-Analog Electronic Circuits

Prepared By	Verified By	Approved by
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Vision of the Institute

Development of academically excellent, culturally vibrant, socially responsible and globally competent human resources.

Mission of the Institute

- To keep pace with advancements in knowledge and make the students competitive and capable at the global level.
- To create an environment for the students to acquire the right physical, intellectual, emotional and moral foundations and shine as torch-bearers of tomorrow's society.
- To strive to attain ever-higher benchmarks of educational excellence

Vision of the Department

To create Electrical and Electronics Engineers who excel to be technically competent and fulfill the cultural and social aspirations of the society.

Mission of the Department

- To provide knowledge to students that builds a strong foundation in the basic principles of electrical engineering, problem solving abilities, analytical skills, soft skills and communication skills for their overall development.
- To offer outcome based technical education.
- To encourage faculty in training & development and to offer consultancy through research & industry interaction.

BEE303-Analog Electronic Circuits

IPCC Course Code	BEE303	CIE Marks	25
Number of Practical Hours/Week	03	Total Hours/ Sessions	10 Lab slots

Credits - 04

Sl. No	Experiments
01	Experiments on series, shunt and double ended clippers and clampers.
02	Design and Testing of Full wave – centre tapped transformer type and Bridge type rectifier circuits with and without Capacitor filter. Determination of ripple factor, regulation and efficiency
03	Static Transistor characteristics for CE, CB and CC modes and determination of h parameters
04	Frequency response of single stage BJT and FET RC coupled amplifier and determination of half power points, bandwidth, input and output impedances.
05	Design and testing of BJT-RC phase shift oscillator for given frequency of oscillation.
06	Design and testing of Hartley and Colpitt's oscillator for given frequency of oscillation.
07	Determination of gain, input and output impedance of BJT Darlington emitter follower with and without bootstrapping.
08	Design and testing of Class A and Class B power amplifier and to determine conversion efficiency.
09	Design, simulation (MATLAB) and testing of Wien bridge oscillator for given frequency of oscillation.
10	Design and simulation of Full wave – centre tapped transformer type and Bridge type rectifier circuits with and without Capacitor filter using MATLAB. Determination of ripple factor, regulation and efficiency.

Conduct of Practical Examination:

1. All laboratory experiments are to be included for practical examination.
2. Breakup of marks and the instructions printed on the cover page of answer script to be strictly adhered by the examiners.

3. Students can pick one experiment from the questions lot prepared by the examiners.
4. Change of experiment is allowed only once and 15% Marks allotted to the procedure part to be made zero.

Sl. No	Cycle –I Experiments
01	Experiments on series, shunt and double ended clippers and clampers.
02	Design and Testing of Full wave – centre tapped transformer type and Bridge type rectifier circuits with and without Capacitor filter. Determination of ripple factor, regulation and efficiency
03	Static Transistor characteristics for CE, CB and CC modes and determination of h parameters
04	Frequency response of single stage BJT and FET RC coupled amplifier and determination of half power points, bandwidth, input and output impedances.
05	Design and testing of BJT-RC phase shift oscillator for given frequency of oscillation.
	Cycle –II Experiments
06	Design and testing of Hartley and Colpitt's oscillator for given frequency of oscillation.
07	Determination of gain, input and output impedance of BJT Darlington emitter follower with and without bootstrapping.
08	Design and testing of Class A and Class B power amplifier and to determine conversion efficiency.
09	Design, simulation (MATLAB) and testing of Wien bridge oscillator for given frequency of oscillation.
10	Design and simulation of Full wave – centre tapped transformer type and Bridge type rectifier circuits with and without Capacitor filter using MATLAB. Determination of ripple factor, regulation and efficiency.

Program Outcomes (PO's)

PO1:Engineering Knowledge: Apply the knowledge of mathematics, science, engineering fundamentals and an engineering specialization to the solution of complex engineering problems.

PO2: Problem Analysis: Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.

PO3: Design / Development of Solutions: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.

PO4: Conduct Investigations of Complex Problems: Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.

PO5: Modern Tool Usage: Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.

PO6: The Engineer and Society: Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.

PO7: Environment and Sustainability: Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.

PO8: Ethics: Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.

PO9: Individual and Team Work: Function effectively as an individual and as a member or leader in diverse teams, and in multidisciplinary settings.

PO10: Communication: Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.

PO11: Project Management and Finance: Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.

PO12: Life-Long Learning: Recognize the need for and have the preparation and ability to engage in independent and lifelong learning in the broadest context of technological change.

Program Specific Outcomes (PSO's)

PSO1: Apply the concepts of Electrical & Electronics Engineering to evaluate the performance of power systems and also to control industrial drives using power electronics.

PSO2: Demonstrate the concepts of process control for Industrial Automation, design models for environmental and social concerns and also exhibit continuous self- learning.

Program Educational Objectives (PEO's)

PEO1: To produce competent and ethical Electrical and Electronics Engineers who will exhibit the necessary technical and managerial skills to perform their duties in society.

PEO2: To make graduates continuously acquire and enhance their technical and socio-economic skills.

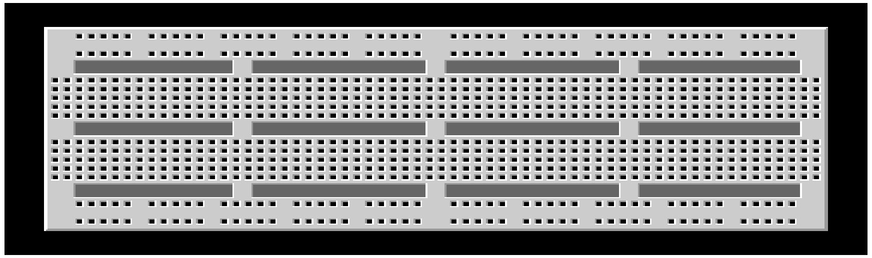
PEO3: To aspire graduates on R&D activities leading to offering solutions and excel in various career paths.

PEO4: To produce quality engineers who have the capability to work in teams and contribute to real time projects.

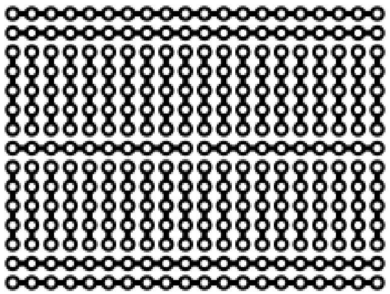
Identification of Circuit Components

Breadboards:

in order to temporarily construct a circuit without damaging the components used to build it, we must have some sort of a platform that will both hold the components in place and provide the needed electrical connections. In the early days of electronics, most experimenters were amateur radio operators. They constructed their radio circuits on wooden breadboards. Although more sophisticated techniques and devices have been developed to make the assembly and testing of electronic circuits easier, the concept of the breadboard still remains in assembling components on a temporary platform.



a. Typical breadboard

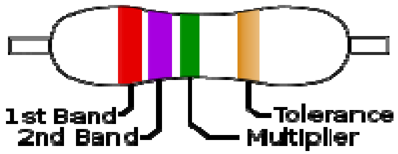


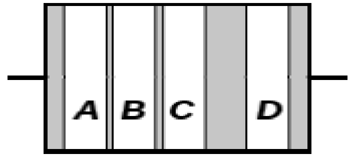
b. Connection details

A real breadboard is shown in Fig. 1(a) and the connection details on its rear side are shown in Fig. 1(b). The five holes in each individual column on either side of the central groove are electrically connected to each other, but remain insulated from all other sets of holes. In addition to the main columns of holes, however, you'll note four sets or groups of holes along the top and bottom. Each of these consists of five separate sets of five holes each, for a total of 25 holes. These groups of 25 holes are all connected together on either side of the dotted line indicated on Fig.1(a) and needs an external connection if one wishes the entire row to be connected. This makes them ideal for distributing power to multiple ICs or other circuits.

Resistors:

Band Color	Digit	Multiplier	Tolerance
Black	0	1	---
Brown	1	10	±1%
Red	2	100	±2%
Orange	3	1,000	±3%
Yellow	4	10,000	±4%
Green	5	100,000	---
Blue	6	1,000,000	---
Violet	7	10,000,000	---
Gray	8	100,000,000	---
White	9	---	---
Gold	---	0.1	±5%
Silver	---	0.01	±10%
None	---	---	±20%





- band A is first significant figure of component value
- band B is the second significant figure
- band C is the decimal multiplier
- band D if present, indicates tolerance of value in percent (no color means 20%)

For example, a resistor with bands of yellow, violet, red, and gold will have first digit 4 (yellow in table below), second digit 7 (violet), followed by 2 (red) zeros: 4,700 ohms. Gold signifies that the tolerance is ±5%, so the real resistance could lie anywhere between 4,465 and 4,935 ohms.

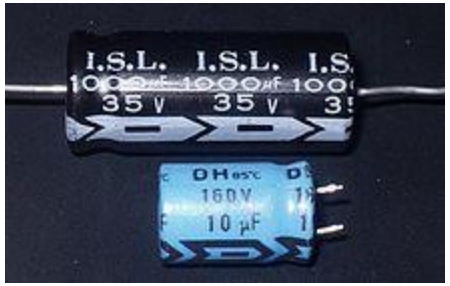
Tight tolerance resistors may have three bands for significant figures rather than two, and/or an additional band indicating temperature coefficient, in units of ppm/K. For large power resistors and potentiometers, the value is usually written out implicitly as "10 kΩ", for instance.

Capacitors:

You will mostly use electrolytic and ceramic capacitors for your experiments.

Electrolytic capacitors

An electrolytic capacitor is a type of capacitor that uses an electrolyte, an ionic conducting liquid, as one of its plates, to achieve a larger capacitance per unit volume than other types. They are used in relatively high-current and low-frequency electrical circuits. However, the voltageapplied to these capacitors must be polarized; one specified terminal must always have positive potential with respect to the other. These are of two types, axial and radial capacitors as shown in adjacent figure. The arrowed stripe indicates the polarity, with the arrows pointing towards the negative pin.



Warning: connecting electrolytic capacitors in reverse polarity can easily damage or destroy the capacitor. Most large electrolytic capacitors have the voltage, capacitance, temperature ratings, and company name written on them without having any special color coding schemes.

Axial electrolytic capacitors have connections on both ends. These are most frequently used in devices where there is no space for vertically mounted capacitors.

Radial electrolytic capacitors are like axial electrolytic ones, except both pins come out the same end. Usually that end (the "bottom end") is mounted flat against the PCB and the capacitor rises perpendicular to the PCB it is mounted on. This type of capacitor probably accounts for at least 70% of capacitors in consumer electronics.

Ceramic capacitors are generally non-polarized and almost as common as radial electrolytic capacitors. Generally, they use an alphanumeric marking system. The number part is the same as for SMT resistors, except that the value represented is in pF. They may also be written out directly, for instance, 2n2 = 2.2 nF.

Diodes:

A standard specification sheet usually has a brief description of the diode. Indescription is the type of diode, the major area of application, and any specific particular interest is the specific application for which the diode is suited. Theyalso provides a drawing of the diode which gives dimension, weight, and, if approximate identification marks. In addition to the above data, the following information is provided: a static operating table (giving spot values of parameters under fixsometimes a characteristic curve (showing how parameters vary over the range), and diode ratings (which are the limiting values of operating conditionscould cause diode damage). Manufacturers specify these various diode operations

and characteristics with "letter symbols" in accordance with fixed definitions.

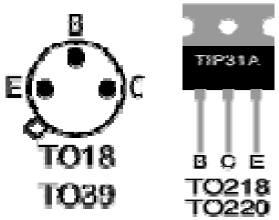
Transistors:

Transistor are identified by a Joint-Navy (JAN) designation printed directly on thecase of the transistor. If in doubt about a transistor's markings, always replace a transistor with one having identical markings, or consult an equipment or transistor manual to ensure that an identical replacement or substitute is used.

Example:

2	N	130	A
NUMBER OF JUNCTIONS	SEMICONDUCTOR	IDENTIFICATION	FIRST MODIFICATION

Identifying the transistor



Testing with a multimeter

Transistor Resistance Values for the PNP and NPN transistor types

Between Transistor Terminals		PNP	NPN
Collector	Emitter	R_{HIGH}	R_{HIGH}
Collector	Base	R_{LOW}	R_{HIGH}
Emitter	Collector	R_{HIGH}	R_{HIGH}
Emitter	Base	R_{LOW}	R_{HIGH}
Base	Collector	R_{HIGH}	R_{LOW}
Base	Emitter	R_{HIGH}	R_{LOW}

Experiment No: 01 **Date:**

Experiments on series, shunt and double ended clippers and clampers.

Objective: To design and test diode clipping circuits for peak clipping and peak detection and Design and test positive and negative clamping circuit for a given reference voltage

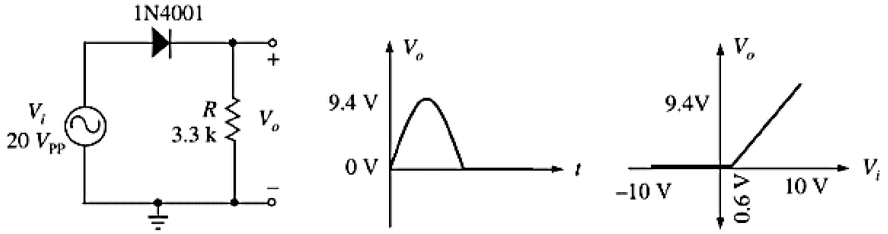
Apparatus Required:

SL. No	Particular	Range	Quantity
1	Bread board		1
2	CRO		1
3	Power supply	DC 0-30V	2
5	Diodes	1N4007	1
6	Resistors	1KΩ	1
7	Function generator		
8	Connecting wire and prob		As required

Theory:

A transistor is a three terminal device. The terminals are emitter, base, collector. In common emitter configuration, input voltage is applied between base and emitter terminals and output is taken across the collector and emitter terminals. Therefore the emitter terminal is common to both input and output. The input characteristics resemble that of a forward biased diode curve. This is expected since the Base-Emitter junction of the transistor is forward biased. As compared to CB arrangement I_B increases less rapidly with V_{BE} .Therefore input resistance of CE circuit is higher than that of CB circuit. The output characteristics are drawn between Ic and V_{CE} at constant $I_{B.}$ the collector current varies with V_{CE} unto few volts only. After this the collector current becomes almost constant, and independent of V_{CE}. The value of V_{CE} up to which the collector current changes with V_{CE} is known as Knee voltage. The transistor always operated in the region above Knee voltage, I_C is always constant and is approximately equal to I_B.

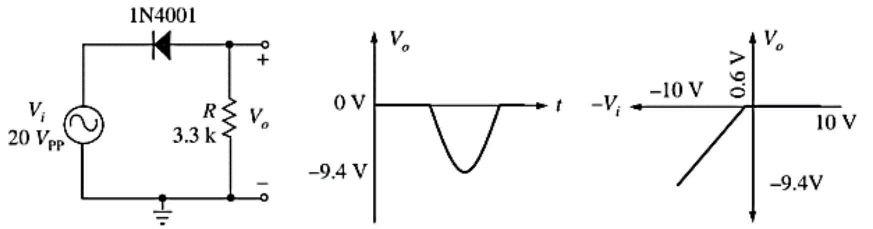
Series Negative Clipper Circuit (Unbiased)



(a) Circuit diagram (b) Output waveform (c) Transfer characteristics

$V_{in(p-p)}$	$V_{o+(p)}$	$V_{o-(p)}$
8V 12V 20V		

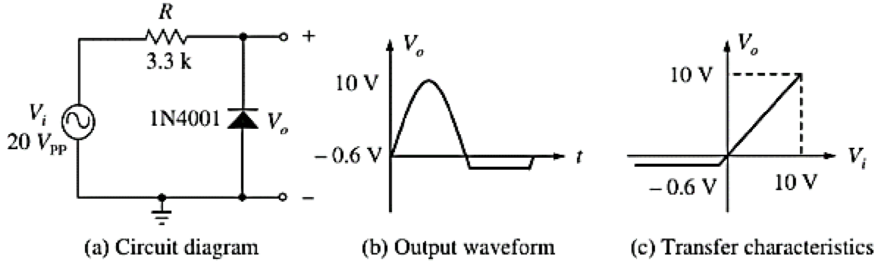
Series Positive Clipper Circuit (Unbiased)



(a) Circuit diagram (b) Output waveform (c) Transfer characteristics

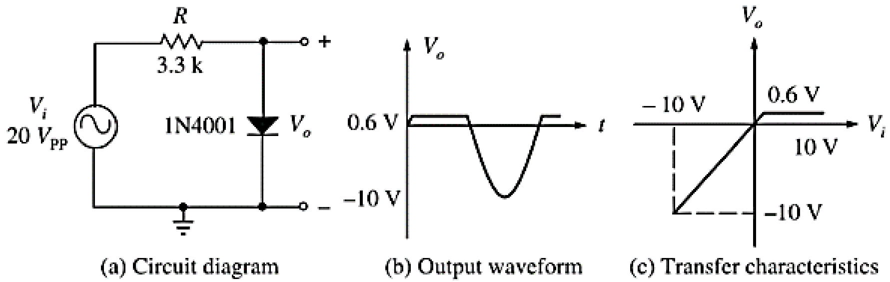
$V_{in(p-p)}$	$V_{o+(p)}$	$V_{o-(p)}$
8V 12V 20V		

Shunt Negative Clipper Circuit (Unbiased)



$V_{in(p-p)}$	$V_{o+(p)}$	$V_{o-(p)}$
8V 12V 20V		

Shunt Positive Clipper Circuit (Unbiased)



$V_{in(p-p)}$	$V_{o+(p)}$	$V_{o-(p)}$
8V 12V 20V		

Diode shunt clipping (Positive peak clipping with positive bias voltage)

Circuit diagram:

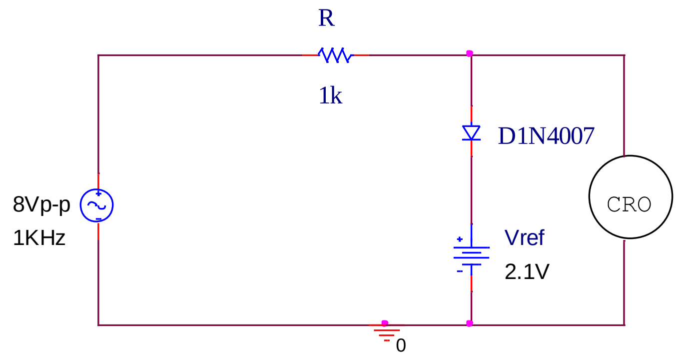


Fig.1.1: Circuit diagram of Diode shunt clipping (Positive peak clipping with positive bias voltage)

Design:

Let the output voltage to be clipped at 2.8V i,e Vo(max)=2.8V

But Vo(max)=Vd+Vref

Where Vd= diode forward voltage drop=0.7V

$$\therefore V_{ref} = V_{o(max)} - V_d = 2.8 - 0.7 = 2.1V$$

Choose the value of R such that the current in the circuit must lie between 1mA to 10mA.

Let current be 1mA

$$\text{Then} \quad R = \frac{V_{i(max)} - V_{o(max)}}{I} = \frac{4 - 2.8}{1.5m} = 800\Omega$$

Choose R=1KΩ

Expected waveform:

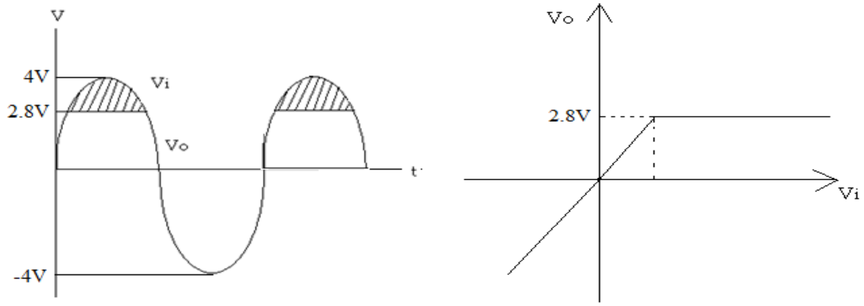


Fig. 1.2: output waveform and transfer characteristics

Tabular column:

$V_{i(p-p)}$	V_{ref}	$V_{o+(p)}$	$V_{o-(p)}$
6V	2.1		
8V	2.1		
10V	2.1		
12V	2.1		

Diode shunt clipping (Negative peak clipping with Negative bias voltage)

Circuit diagram:

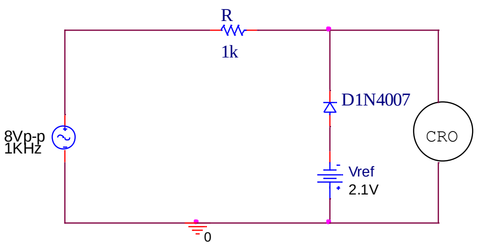


Fig.1.5: Diode shunt clipping (Negative peak clipping)

Design:

Let the output voltage to be clipped at 2.8V i,e $V_{o(max)}$= - 2.8V

But $V_{o(min)}$= - (V_d+V_{ref})

Where V_d= diode forward voltage drop=0.7V

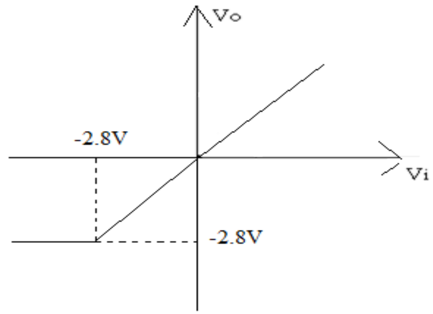
$$\therefore -V_{ref} = V_{o(min)} - V_d = -2.8 + 0.7 = -2.1V$$

Choose the value of R such that the current in the circuit must lie between 1mA to 10mA.

Let current be 1mA

Then

$$R = \frac{V_{i(max)} - V_{o(max)}}{I} = \frac{4-2.8}{1.5m} = 800\Omega$$



Choose R=1KΩ

Expected waveform:

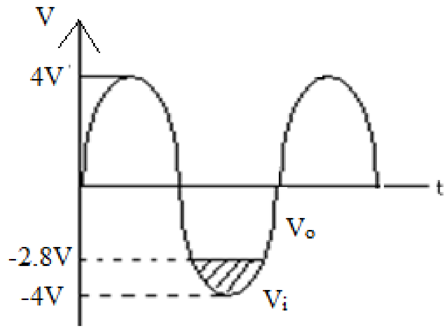


Fig. 1.6: Output waveform and transfer characteristics

Tabular column:

$V_{i(p-p)}$	V_{ref}	$V_{o+(p)}$	$V_{o-(p)}$
6V	2.1		
8V	2.1		
10V	2.1		
12V	2.1		

Diode series clipping (Positive peak clipping with Positive bias voltage)

Circuit diagram:

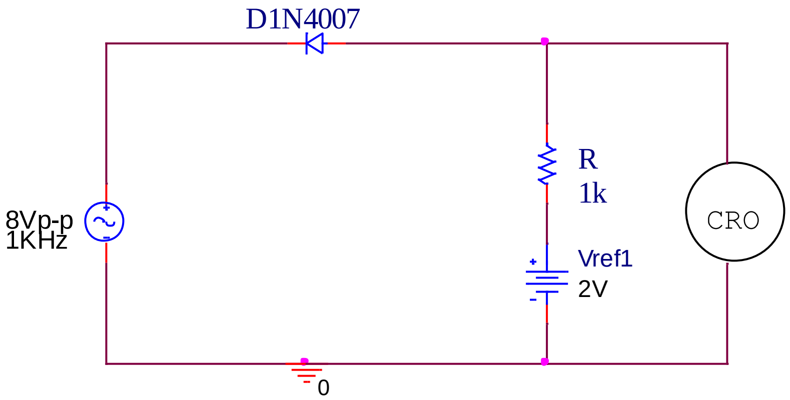


Fig. 1.7: Diode series clipping circuit (Positive peak clipping with Positive bias voltage)

Design:

Let the output voltage to be clipped at 2V i,e $V_{o(max)}=V_{ref}=2V$

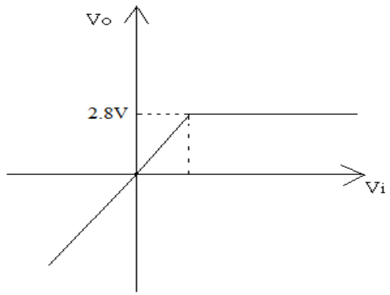
Choose the value of R such that the current in the circuit must lie between 1mA to 10mA.

Let current be 2mA

Then

$$R = \frac{V_{i(max)} - V_{o(max)}}{I} = \frac{4-2}{2m} = 1000\Omega$$

Choose R=1KΩ



Expected waveform:

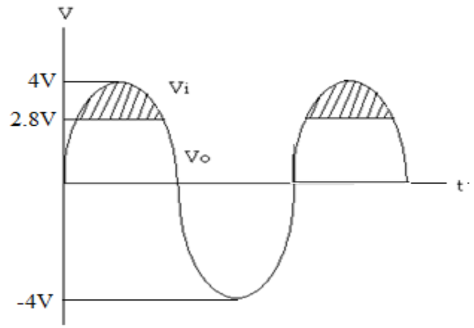


Fig. 1.8: Output waveform and transfer characteristics

Tabular column:

$V_{i(p-p)}$	V_{ref}	$V_{o+(p)}$	$V_{o-(p)}$
6V	2.0		
8V	2.0		
10V	2.0		
12V	2.0		

Diode series clipping (Negative peak clipping with Negative bias voltage)

Circuit diagram:

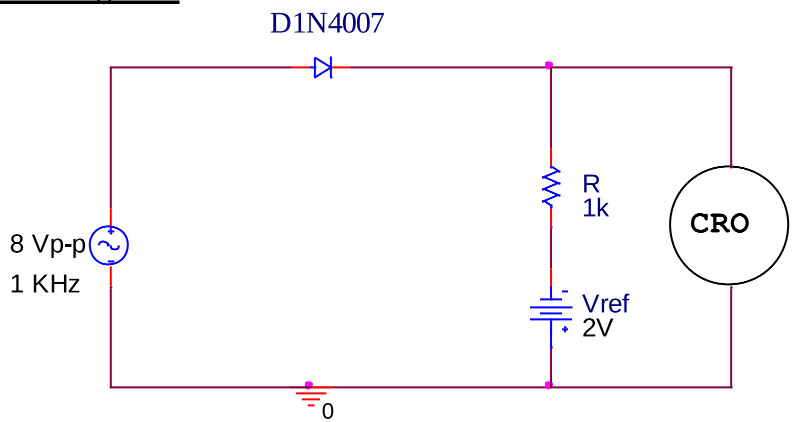


Fig. 1.9: Diode series clipping circuit (Negative peak clipping with Negative bias voltage)

Design:

Let the output voltage to be clipped at 2V i,e $V_{o(max)}=V_{ref} = 2V$

Choose the value of R such that the current in the circuit must lie between 1mA to 10mA.

Let current be 2mA

Then $R = \frac{V_{i(max)} - V_{o(max)}}{I} = \frac{4-2}{2m} = 1000\Omega$

Choose R=1KΩ

Expected waveform:

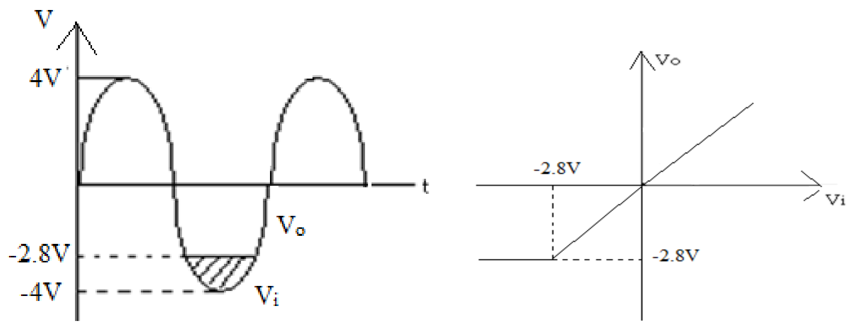


Fig. 1.10: Output waveform and transfer characteristics

Tabular column:

$V_{i(p-p)}$	V_{ref}	$V_{o+(p)}$	$V_{o-(p)}$
6V	-2.0		
8V	-2.0		
10V	-2.0		
12V	-2.0		

Clipping at two independent levels

Circuit diagram:

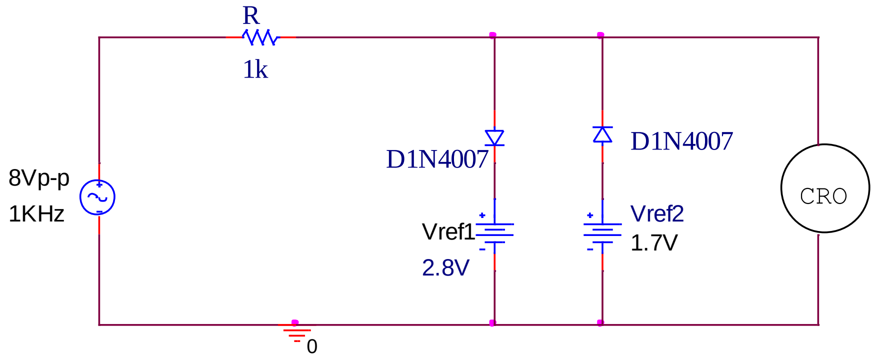


Fig. 1.11: Two independent level clipping circuit.

Design:

To obtain a slice of input voltage between 1V and 3V

Let $V_{ref1} > V_{ref2}$

$V_{o(max)} = 3.5V$

And $V_{o(max)} = V_d - V_{ref1}$

$\therefore V_{ref1} = V_{o(max)} + V_d = 1.7V.$

$V_{o(min)} = 1V$

And $V_{o(min)} = V_d + V_{ref2}$

$\therefore V_{ref2} = V_{o(max)} - V_d = 2.8V.$

Choose the value of R such that the current in the circuit must lie between 1mA to 10mA.

Let current be 1mA

Then $R = \frac{V_{i(max)} - V_{o(max)}}{I} = \frac{4 - 3.5}{1m} = 500\Omega$

Choose R=470Ω

Expected waveform:

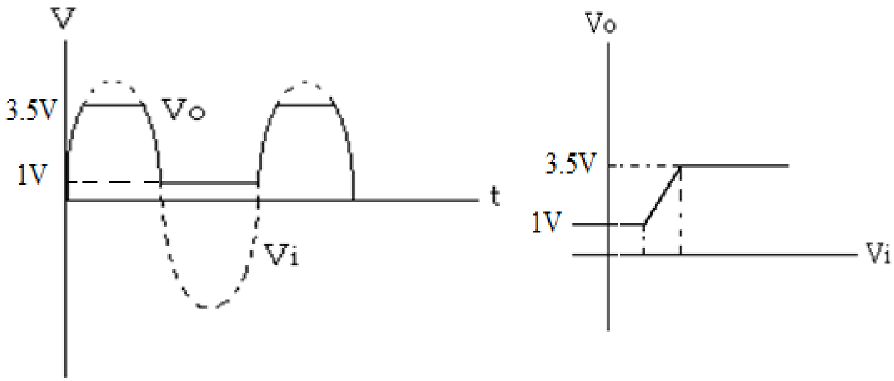


Fig. 1.12: Output waveform and transfer characteristics

Double ended clipping (symmetrical square wave generator)

Circuit diagram:

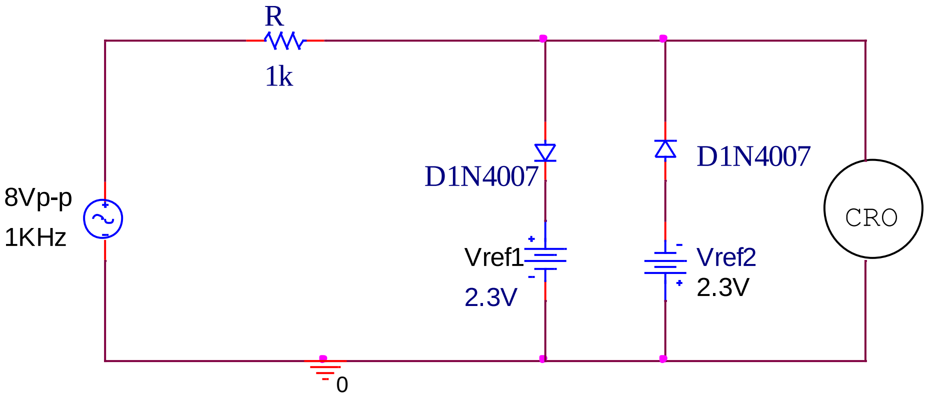


Fig. 1.13: Double ended clipping circuit (symmetrical square wave generator)

Design:

To generate a symmetrical square wave of $\pm 3V$

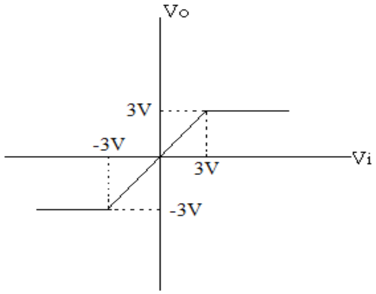
i.e $V_{o(max)} = 3V$ & $V_{o(min)} = -3V$

$V_{o(max)} = V_d + V_{ref1}$

$V_{ref1} = V_{o(max)} - V_d = 3.0 - 0.7 = 2.3V$

$V_{o(min)} = V_d + V_{ref2}$

$V_{ref2} = V_{o(min)} - V_d = 3.0 - 0.7 = 2.3V$



Choose the value of R such that the current in the circuit must lie between 1mA to 10mA.

Let current be 1mA

$$\text{Then } R = \frac{V_{i(max)} - V_{o(max)}}{I} = \frac{4-3}{1m} = 1000\Omega$$

Choose R=1KΩ

Expected waveform:

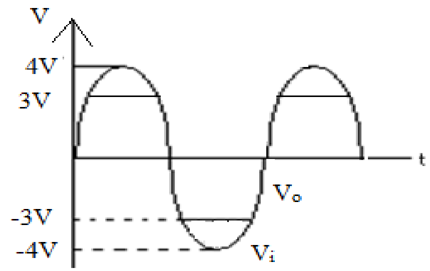


Fig. 1.14: Output waveform and transfer characteristics

Procedure:

- Make the Connections as per the circuit diagram
- Apply sinusoidal input V_i of 1 KHz frequency and of amplitude $8V_{p-p}$ and set the reference voltage as per the design.
- Observe the output signal in the CRO and verify it with given waveforms.
- Apply Vi and Vo to the X and Y channel of CRO and observe the transfer characteristic waveform and verify it.
- Trace the input, output waveforms and the transfer characteristics on a trace sheet.

Result: The clipping circuits are design and output waveforms are verified.

Outcome: at the end of the experiment, Student learns the technique removing any unwanted portion in a given wave form. He/she understands the concept of wave shaping in general

CLAMPER CIRCUITS

Objective: Design and test positive and negative clamping circuit for a given reference voltage

Apparatus Required:

SL. No	Particular	Range	Quantity
1	Bread board		
2	CRO		
3	Power supply	DC 0-20V	
5	Resistors	10KΩ	
6	Capacitor	1µF	
7	Diodes	1N4007	
8	Function generator		As required

Negative clamper

Circuit diagram:

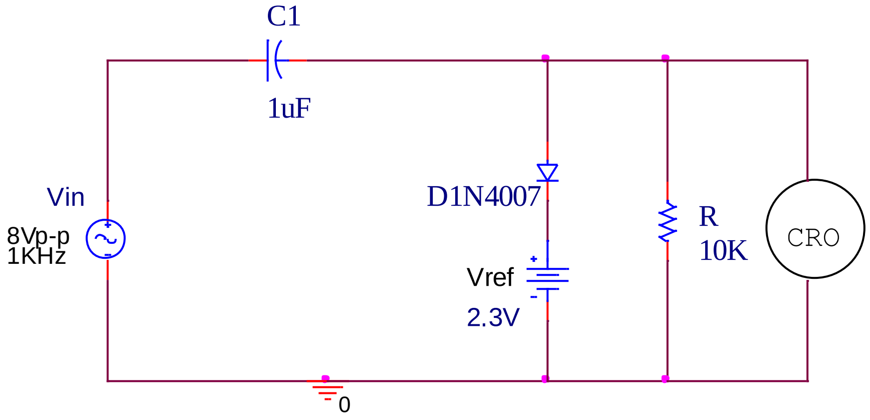


Fig. 1.15: Negative clamper circuit

Design:

To design a clamping circuit to clamp negative peak of output voltage at 3V

$V_{o(max)}=V_{ref}+V_d=3V$

$V_{ref}=V_{o(max)}-V_d=2.3V$

Given frequency =1KHz.

$$\therefore T=\frac{1}{f}=1msec$$

The value of R and C must be selected such that RC >> T

Let RC=10T=10*1msec=10msec.

Let C=1μF then R=10KΩ

Expected waveforms:

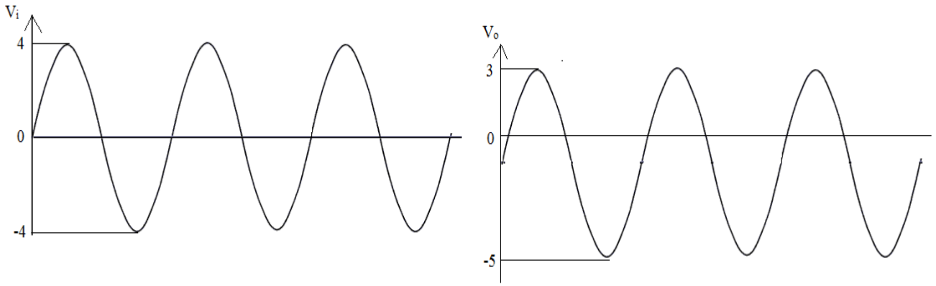


Fig. 1.16: Input & output Waveforms of negative clamping circuit

Procedure:

- Make the connection as per the circuit diagram.
- Apply sinusoidal input signal of 8V P-P from signal generator and set the reference voltage to the designed value.
- Observe the output waveform in the CRO and trace the input and output waveforms on trace sheet.
- Note down the readings from the CRO and compare it with the expected values.

Positive clamper

Circuit diagram:

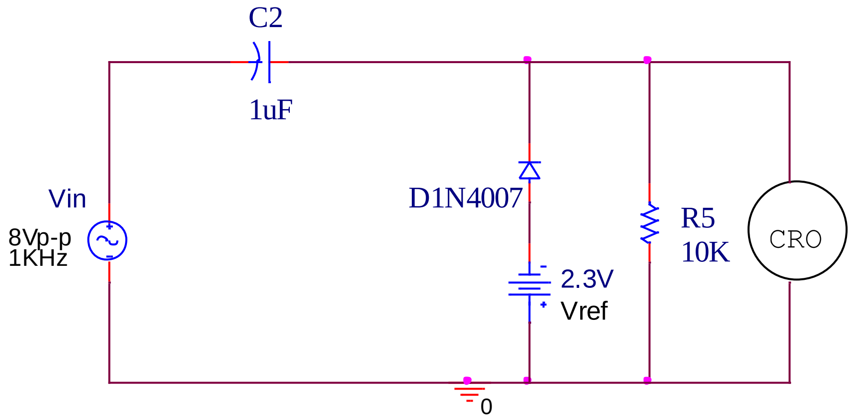


Fig. 1.17: Positive clamper circuit

Design:

To design a clamping circuit to clamp negative peak of output voltage at 3V

$V_{o(max)}=V_{ref}+V_d=5V$

$V_{ref}=V_{o(max)}-V_d=2.3V$

Given frequency =1 KHz.

$$\therefore T=\frac{1}{f}=1msec$$

The value of R and C must be selected such that RC >> T

Let RC=10T=10*1msec=10msec.

Let C=1μF then R=10KΩ

Waveforms:

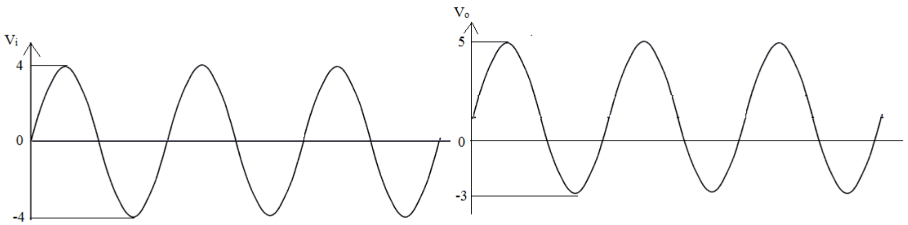


Fig. 1.18: Input & output Waveforms of positive clamping circuit

Procedure:

- Make the connection as per the circuit diagram.
- Apply sinusoidal input signal of 8V P-P from signal generator and set the reference voltage to the designed value.
- Observe the output waveform in the CRO and trace the input and output waveforms on trace sheet.
- Note down the readings from the CRO and compare it with the expected values.

Result: The clipping circuits are design and output waveforms are verified.

Outcome: at the end of the experiment, Student learns how to shift a given waveform to the specific dc level by manipulation of the active devices.

Experiment No: 02 Date:

Design and Testing of Full wave –centre tapped transformer type and Bridge type rectifier circuits with and without Capacitor filter. Determination of ripple factor, regulation and efficiency

objective: -To design and testing of Full wave –centre tapped transformer type and Bridge type rectifier circuits with and without Capacitor filter. Determination of ripple factor, regulation and efficiency

Apparatus Required:

SL.No	Particular	Range	Quantity
1	Transformer	12V/19V	01
2	Diode(IN4001)	-	4
3	Resistor and capacitors	1KΩ, 100μF	2
4	Multimeter	-	1
5	CRO Probes	-	2 set
6	Bread Board and connecting wires	-	1

Theory

Rectifier is a circuit which converts AC to pulsating DC. Rectifiers are used in construction of DC power supplies. There are three types of rectifiers namely Half wave rectifier, Centre tap full wave rectifier and bridge rectifier.

In half wave rectification, either the positive or negative half of the AC wave is passed, while the other half is blocked. Because only one half of the input waveform reaches the output, it is very inefficient if used for power transfer.

A full-wave rectifier converts the whole of the input waveform to one of constant polarity (positive or negative) at its output. Full-wave rectification converts both polarities of the input waveform to DC (direct current), and is more efficient. Fullwave rectification can be obtained either by using center tap transformer or by using bridge rectifier.

The output of a rectifier is not a smooth DC it consists of ac ripples therefore to convert this pulsating DC in to smooth DC we use a circuit called filter. There are many types of filters like C filter, L filter, LC filter, multiple LC filter, πfilter etc..of all these C filter is the most fundamental filter.

Circuit Diagram:

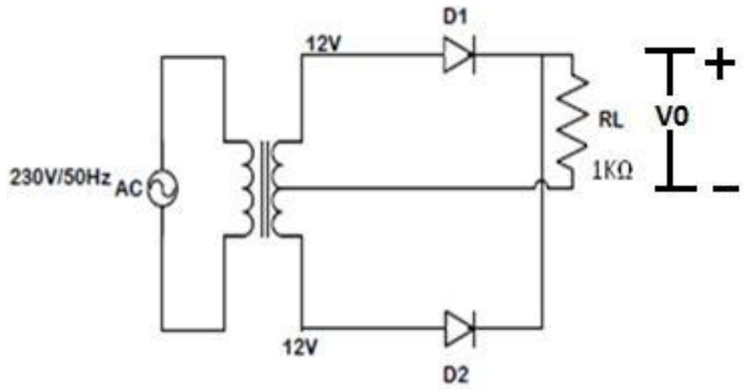


Fig. 1.1 Circuit of full wave rectifier without filter

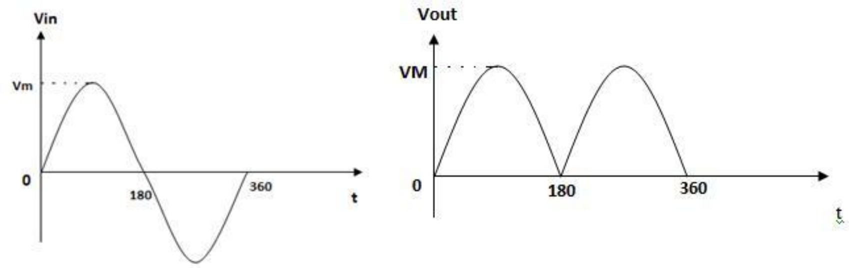


Fig. 1.2 Waveform for full wave rectifier without filter

Calculations: <u>Full wave rectifier without filter</u>

Under No Load

$V_{M\,(NL)}$ = ___________V (Peak value of voltage from CRO)

V_{DC} is dc (average) value, $V_{DC\,(NL)} = \left(\frac{2V_{M(NL)}}{\pi}\right)$ = ____________ V

Full-Load readings:

Peak Output Voltage, V_M = _________V

Average value $V_{DC} = \frac{2V_M}{\pi}$ = $V_{DC(FL)}$ = -------------------- V

$V_{RMS} = \frac{V_M}{\sqrt{2}}$

$V_{AC} = \sqrt{V_{RMS}^2 - V_{DC}^2}$

Ripple Factor $\gamma = V_{AC} / V_{DC}$ =

$P_{DC} = V_{DC}^2 / R_L$ =

$P_{AC} = V_{RMS}^2 / R_L$ =

% $\eta = (P_{DC} / P_{AC}) * 100$

% Regulation = $\frac{V_{DC(NL)} - V_{DC(FL)}}{V_{DC(FL)}} * 100 =$

The peak inverse voltage for each diode is PIV = $2V_{p(out)} + 0.7$ V =

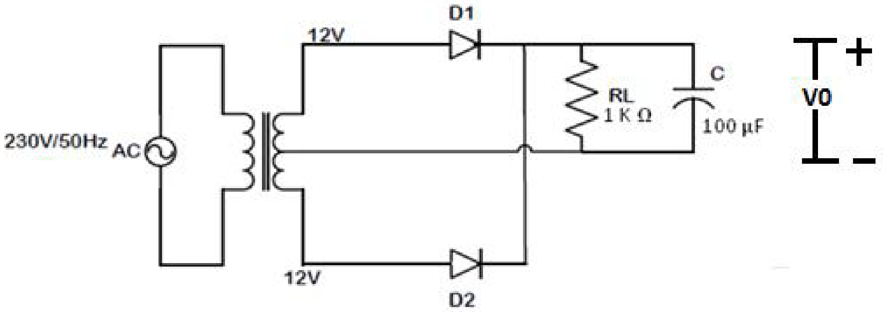


Fig. 1.3 Circuit of full wave rectifier with capacitor filter

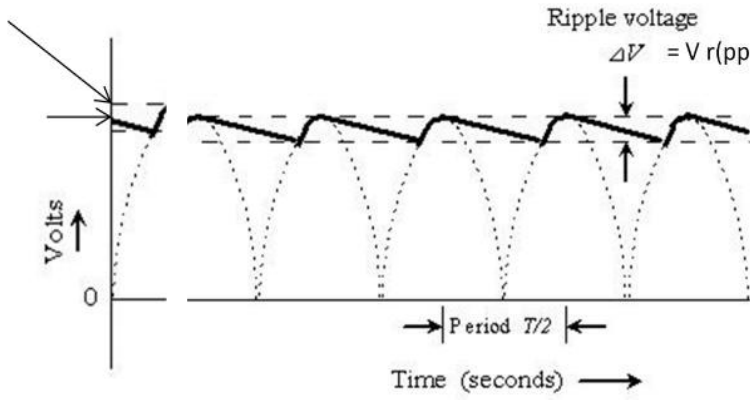


Fig. 1.4 Waveform for full wave rectifier with filter

Full wave rectifier with filter

$V_{(NL)}$ = ___________V

Full-Load readings:

Peak Output Voltage, V_M = _________V

Ripple Factor $\gamma = V_{AC}/ V_{DC}$

$V_{DC} = \frac{2V_M}{\pi} = V_{DC(FL)} =$

$R=R_L$

$V_{AC} = \frac{Vr(p-p)}{2\sqrt{3}}$

$V_{RMS}=\sqrt{V_{AC}^2 + V_{DC}^2}$

$P_{DC} = V_{DC}^2/ R_L =$

$P_{AC} = V_{RMS}^2/R_L =$

$\% \eta = (P_{DC}/ P_{AC})*100$

$\% \text{ Regulation} = \frac{V_{DC(NL)} - V_{DC(FL)}}{V_{DC(FL)}} * 100 =$

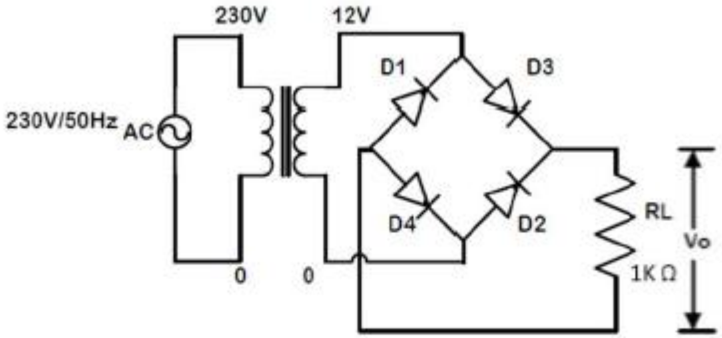


Fig. 1.5 Circuit of bridge rectifier without capacitor filter

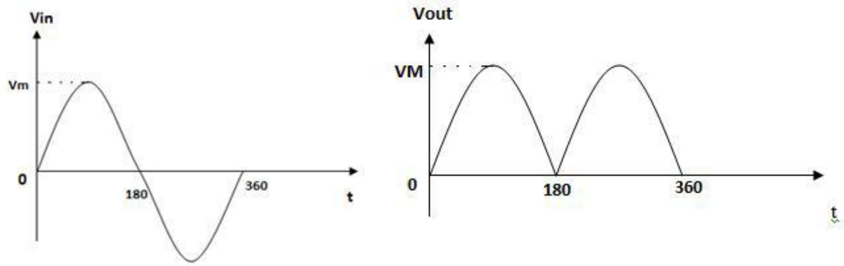


Fig. 1.6 Waveform for bridge rectifier with without filter

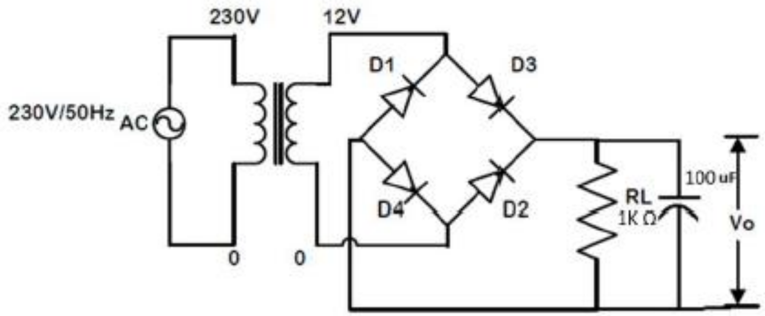
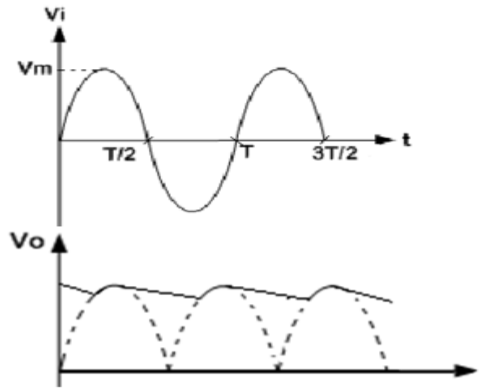


Fig. 1.7 Circuit of bridge rectifier with capacitor filter



Calculation and formula are same as full wave bridge rectifier.

Procedure:

Without Capacitor:

1. Connections are made as shown in the circuit diagram.
2. Measure the voltage across the terminals when the resistor is open circuited (No Load:-take it as V_{NL}).
3. Connect the load resistor across the output terminals and note, the peak voltage from DSO (V_M)
4. Repeat the above procedure for full wave rectifier and bridge rectifier.
5. Switch off the supply

With Capacitor:

1. Connections are made as shown in the Figure 2 for half wave rectifier circuit with Capacitor.
2. Using DSO measure the voltage across the terminals when the resistor is open circuited (No load: - take it as VNL) but capacitor is connected.
3. Connect the load resistor across the output terminals and note, the peak voltage from DSO (VM)
4. Repeat the above procedure for full wave rectifier and bridge rectifier with Capacitor.
5. Switch off the supply and remove the connections

Result:

Table 1.1 Comparison of Rectifier

Rectifier Type	Without Filter			Without Filter		
	Ripple factor	Efficiency	Regulation	Ripple factor	Efficiency	Regulation
FWR						
BR						

Conclusions:

Vive Voce

1. What is the function of a bridge rectifier?
2. Why do we need ripple factor?
3. Why capacitor is used in bridge rectifier?

Preparation(4)	Conduction(4)	Result/Conclusion(5)	Total(13)

Signature with date

Experiment No: 03 **Date:**

Static Transistor characteristics for CE, CB and CC modes and determination of h parameters

Objective: To determine the h-parameters of CE, CB and CC modes of transistor with the help of static characteristics.

Common Emitter Configuration:

Apparatus Required:

SL.No	Particular	Range	Quantity
1	Bread board		1
2	CRO		1
3	Power supply	DC 0-30V	2
5	Transistor	CL100/SL100	1
6	Resistors	100kΩ, 100Ω	1
	Voltmeters	0-20V	2
	Ammeters	0-200mA	1
9	Connecting wire and prob		As required

Theory:

A transistor is a three terminal device. The terminals are emitter, base, collector. In common emitter configuration, input voltage is applied between base and emitter terminals and output is taken across the collector and emitter terminals. Therefore the emitter terminal is common to both input and output. The input characteristics resemble that of a forward biased diode curve. This is expected since the Base-Emitter junction of the transistor is forward biased. As compared to CB arrangement I_B increases less rapidly with V_{BE} .Therefore input resistance of CE circuit is higher than that of CB circuit. The output characteristics are drawn between Ic and V_{CE} at constant $I_{B.}$ the collector current varies with V_{CE} unto few volts only. After this the collector current becomes almost constant, and independent of V_{CE}. The value of V_{CE} up to which the collector current changes with V_{CE} is known as Knee voltage. The transistor always operated in the region above Knee voltage, I_C is always constant and is approximately equal to I_B.

Circuit diagram:

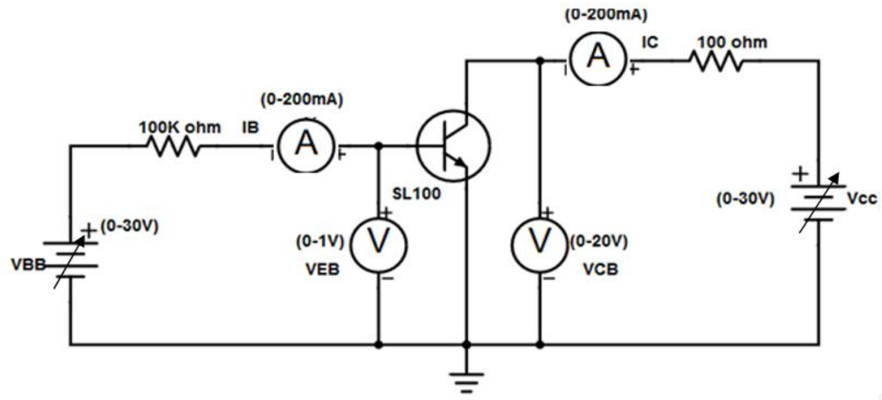


Fig.2.1: Circuit diagram of Transistor Common Emitter Configuration

Procedure:

Input Characteristics:

1. Connect the circuit as per the circuit diagram.
2. For plotting the input characteristics the output voltage V_{CE} is kept constant at 1V and for different values of V_{BE}. Note down the values of I_C
3. Repeat the above step by keeping V_{CE} at 2V and 4V.
4. Tabulate all the readings.
5. plot the graph between V_{BE} and I_B for constant $V_{CE.}$

Output Characteristics:

1. Connect the circuit as per the circuit diagram
2. For plotting the output characteristics the input current I_B is kept constant at 10μA and for different values of V_{CE} note down the values of I_C
3. Repeat the above step by keeping I_B at 75 μA 100 μA
4. Tabulate the all the readings
5. Plot the graph between V_{CE} and I_C for constant $I_{B,}$

Tabular Column:

Input characteristics

Sl. No	$V_{BB}(V)$	V_{CE} =1V		V_{CE} =2V		V_{CE} =5V	
		V_{BE}(V)	I_B(μA)	V_{BE}(V)	I_B(μA)	V_{BE}(V)	I_B(μA)
	0.1						
	0.2						
	0.3						
	0.4						
	0.5						
	0.6						
	0.7						
	0.8						
	0.9						
	1						
	2						
	3						
	10						

Output Characteristics:

Sl. No	V_{CC}	I_B =10μA V_{BB} =		I_B =50μA V_{BB} =		I_B =75μA V_{BB} =		I_B =100μA V_{BB} =	
		V_{CE}(V)	I_C(μA)	V_{CE}(V)	I_C(μA)	V_{CE}(V)	I_C(μA)	V_{CE}(V)	I_C(μA)
		0.1		0.1		0.1		0.1	
		0.2		0.2		0.2		0.2	
		0.3		0.3		0.3		0.3	
		0.4		0.4		0.4		0.4	
		0.5		0.5		0.5		0.5	
		0.6		0.6		0.6		0.6	
		0.7		0.7		0.7		0.7	
		0.8		0.8		0.8		0.8	
		0.9		0.9		0.9		0.9	
		1		1		1		1	
		2		2		2		2	
		20		20		20		20	

Typical Graph:

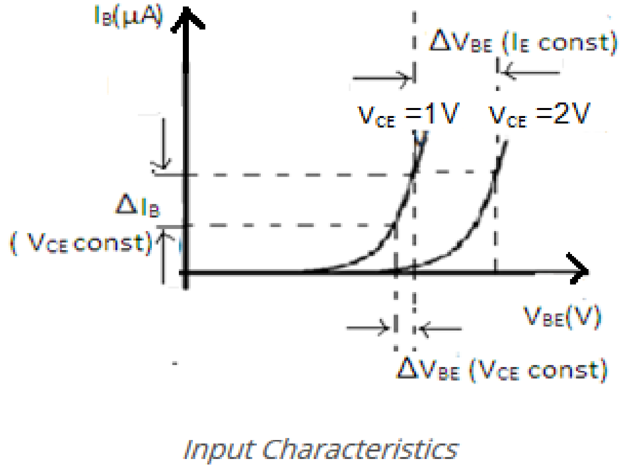


Fig.2.2: Input Characteristics

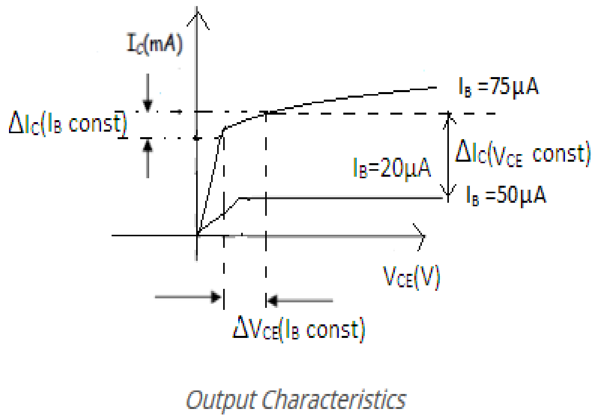


Fig.2.3: Output Characteristics

Calculations:

1. **Input Characteristics:** To obtain input resistance find ΔV_{BE} and ΔI_B for a constant $\mathbf{V_{CE}}$ on one of the input characteristics.
   Input impedance = $h_{ie} = R_i = \Delta \mathbf{V_{BE}} / \Delta \mathbf{I_B}$ ($\mathbf{V_{CE}}$ is constant)
   Reverse voltage gain = $h_{re} = \Delta \mathbf{V_{EB}} / \Delta \mathbf{V_{CE}}$ ($\mathbf{I_B}$ = constant)

2. **Output Characteristics:** To obtain output resistance find $\Delta \mathbf{I_C}$ and $\Delta \mathbf{V_{CB}}$ at a constant $\mathbf{I_B}$.
   Output admittance $1/hoe = R_o = \Delta \mathbf{I_C} / \Delta \mathbf{V_{CE}}$ (I_B is constant)
   Forward current gain = $hfe = \Delta \mathbf{I_C} / \Delta \mathbf{I_B}$ ($\mathbf{V_{CE}}$ = constant)

h - Parameter Model:

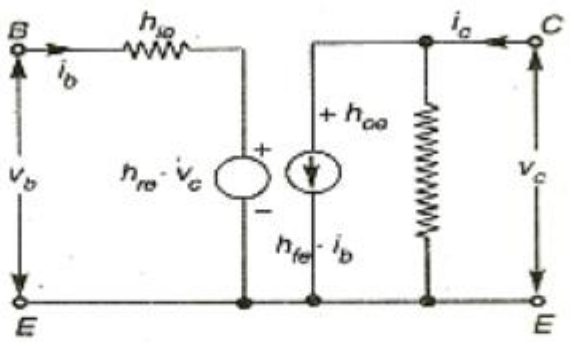


Fig.2.4: h – parameter model of common emitter configuration

Common Base Configuration

Circuit diagram:

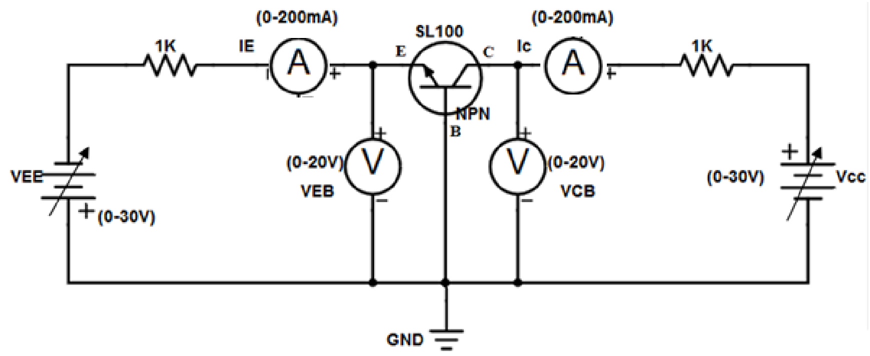


Fig.2.5: Circuit diagram of Transistor Common Base Configuration

Procedure:

Input Characteristics:

1. Connect the circuit as shown in the circuit diagram.
2. Keep output voltage V_{CB} = 0V by varying V_{CC}.
3. Varying V_{EE} gradually, note down emitter current I_E and emitter-base voltage (V_{BE}).
4. Step size is not fixed because of nonlinear curve. Initially vary V_{EE} in steps of 0.1 V. Once the current starts increasing vary V_{EE} in steps of 1V up to 12V.
5. Repeat above procedure (step 3) for V_{CB} =2V and 4V.

Output Characteristics:

1. Connect the circuit as shown in the circuit diagram.
2. Keep emitter current I_E = 5mA by varying V_{EE}.
3. Varying V_{CC} gradually in steps of 1V up to 12V and note down collector current I_C and collector-base voltage (V_{CB}).
4. Repeat above procedure (step 3) for I_E = 10mA

Tabular Column:

Input characteristics

Sl. No.	$V_{EE}(V)$	$V_{CB} = 0$		$V_{CB} = 1V$	
		$V_{EB}(V)$	$I_E(mA)$	$V_{EB}(V)$	$I_E(mA)$

Output Characteristics:

Sl. No.	$V_{CC}(V)$	$I_E = 5\,mA$		$I_E = 10\,mA$	
		V_{CB} in Volts	I_c in m Amps	V_{CB} in Volts	I_C in m Amps

Typical Graph:

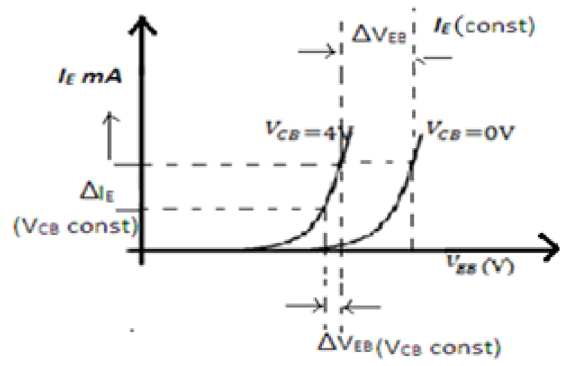


Fig.2.6: Input Characteristics

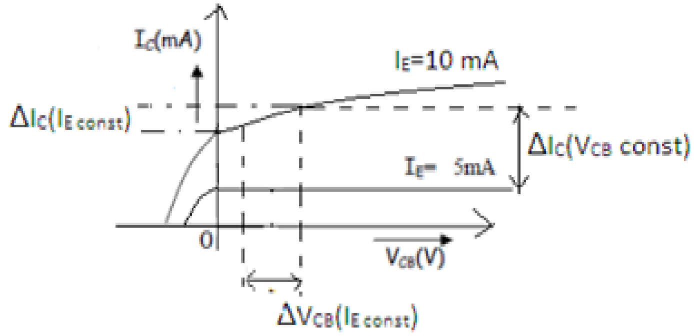


Fig.2.7: Output Characteristics

Calculations:

1. **Input Characteristics:** To obtain input resistance, find ΔV_{EE} and ΔI_E for a constant V_{CB} on one of the input characteristics.
   Input impedance = $h_{ib} = R_i = \Delta V_{EE} / \Delta I_E$ (V_{CB} = constant)
   Reverse voltage gain = hrb = $\Delta V_{EB} / \Delta V_{CB}$ (I_E = constant)

2. **Output Characteristics:** To obtain output resistance, find ΔI_C and ΔV_{CB} at a constant I_E.
   Output admitance = $h_{ob} = 1/Ro = \Delta I_C / \Delta V_{CB}$ (I_E = constant)
   Forward current gain = $h_{fb} = \Delta I_C / \Delta I_E$ (V_{CB} = constant)

h - Parameter Model:

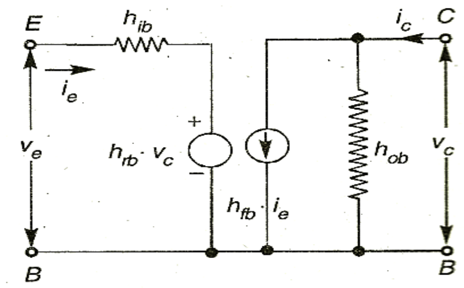


Fig.2.8: h – parameter model of common base configuration

Common Collector Configuration

Circuit diagram:

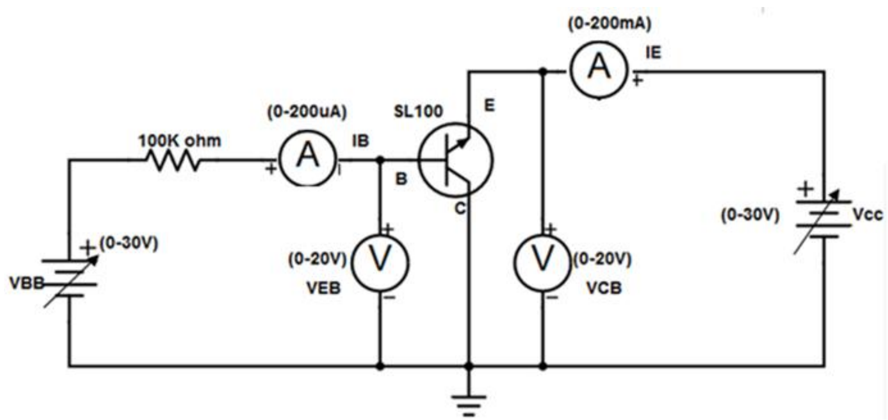


Fig.2.9: Circuit diagram of Transistor Common Collector Configuration

Procedure:

Input Characteristics:

1. Connect the circuit as shown in the circuit diagram.
2. Keep output voltage $\mathbf{V_{CE}}$ = 0V by varying $\mathbf{V_{CC}}$.
3. Varying $\mathbf{V_{BB}}$ gradually, note down base current $\mathbf{I_B}$ and base-emitter voltage $\mathbf{V_{BE}}$.
4. Step size is not fixed because of non linear curve. Initially vary $\mathbf{V_{BB}}$ in steps of 0.1V. Once the current starts increasing vary $\mathbf{V_{BB}}$ in steps of 1V up to 12V.
5. Repeat above procedure (step 3) for $\mathbf{V_{CE}}$ = 5V.

Output Characteristics:

1. Connect the circuit as shown in the circuit diagram.
2. Keep emitter current $\mathbf{I_B}$ = 20μA by varying $\mathbf{V_{BB}}$.
3. Varying $\mathbf{V_{CC}}$ gradually in steps of 1V up to 12V and note down collector current $\mathbf{I_C}$ and Collector-Emitter Voltage($\mathbf{V_{CE}}$).
4. Repeat above procedure (step 3) for $\mathbf{I_B}$ = 60μA, 0μA.

OBSERVATIONS:

Input Characteristics:

$V_{BB}(V)$	$V_{CE} = 0$		$V_{CE} = 5V$	
	$V_{BE}(V)$	$I_B(\mu A)$	$V_{BE}(V)$	$I_B(\mu A)$

Output Characteristics:

$V_{CC}(V)$	$I_B = 20\mu A$		$I_B = 20\mu AA$	
	$V_{CE}(V)$	$I_c(mA)$	$V_{CE}(V)$	$I_c(mA)$

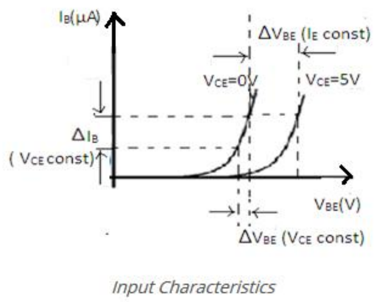


Fig.2.10: Input Characteristics

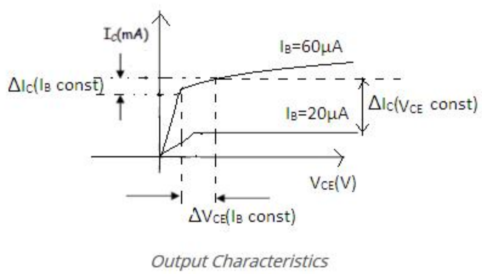


Fig.2.11: Output Characteristics

Calculations from Graph:

1. **Input Characteristics:** To obtain input resistance find ΔV_{BE} and ΔI_B for a constant $\mathbf{V_{CE}}$ on one of the input characteristics.

   Input impedance = $h_{ie} = R_i = \Delta \mathbf{V_{BE}} / \Delta \mathbf{I_B}$ ($\mathbf{V_{CE}}$ is constant)

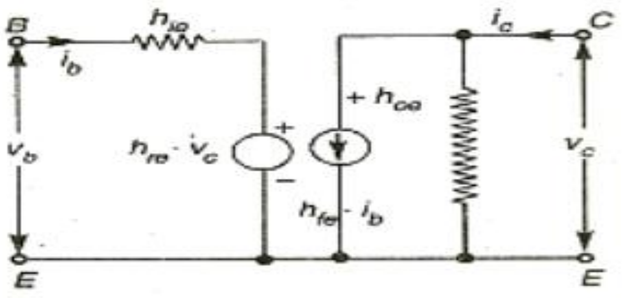
Reverse voltage gain = h_{re} = Δ**V_{EB}** / Δ**V_{CE}** (**I_B** = constant)

2. **Output Characteristics:** To obtain output resistance find Δ **I_C** and Δ**V_{CB}** at a constant **I_B**.

Output admittance 1/hoe = R_o = Δ**I_C** / Δ**V_{CE}** (I_B is constant)

Forward current gain = h_{fe} = Δ**I_C** / Δ**I_B** (**V_{CE}** = constant)

h – Parameter model of CE transistor:



Conclusion:

Preparation(4)	Conduction(4)	Result/Conclusion(5)	Total(13)

Signature with date

Vive Voce

1. Give the comparison between CB and CC Configuration.
2. Mention the differences between CE and CC Configuration.
3. Mention the advantages of CE configuration.

Experiment No: 04 **Date:**

Frequency response of single stage BJT RC coupled amplifier and determination of half power points, bandwidth, input and output impedances.

Objective: To design RC coupled single stage amplifier using BJT and determining gain frequency response, input & output impedances.

Apparatus Required:

SL.No	Particular	Range	Quantity
1	Bread board		1
2	CRO		1
3	Power supply	DC 0-20V	1
4	Signal generator	0-2MHz	1
5	Transistor	CL100/SL100	1
6	Resistors	47KΩ, 8.1KΩ, 2.2 KΩ, 560Ω	
7	Capacitors	47uF, 0.47uF	
8	DRB	1-100MΩ	1
9	Connecting wire and probes		As required

Design:

Let us consider V_{CC}=12V, β=145, I_C=2mA to make transistor to work in active region.

Approximations

$$I_E \cong I_C$$

$$V_E \cong \frac{V_{CC}}{10} = 1.2V$$

$$V_{CE} \cong \frac{V_{CC}}{2} = 6V$$

$V_B=V_{BE}+V_E=1.2+0.7=1.9V$

To find R_E:

W.K.T $V_E=I_E R_E$

$$R_E = \frac{V_E}{I_C} = 600$$

Choosing R_E=560Ω

To find R_C:

Applying KVL to output circuit

$V_{CC}=I_C R_C+V_{CE}+I_E R_E$

$$R_C = \frac{V_{CC} - V_{CE} - I_C R_E}{I_C} = 2400\Omega$$

Choosing R_C=2.2KΩ

To find R_1 & R_2:

$$R_2 \le \frac{\beta R_E}{10}$$

$$R_2 \le \frac{560 \times 145}{10} = 8120\Omega$$

Choosing R_2=8.1KΩ

From the circuit $V_B = \frac{V_{CC} \times R_2}{R_1 + R_2}$

R_2=43058Ω

Choosing R_2=47KΩ

To find coupling capacitors C_C:

$$f_L = \frac{1}{2\pi(R_i + R_S)C_C}$$
$$\text{usually } R_S << R_i$$

$$R_i = R_1 ll\, R_2 ll\, \beta r_e$$
$$r_e = \frac{26mV}{I_E} = 13$$
$$R_i = 47K ll\, 8.1K ll\, (145*13)$$
$$R_i = 1.5K$$

Let f_L=100Hz

$$\therefore C_{in} = \frac{1}{2\pi \times R_i \times f_L} = 1.06\mu F$$

Choosing C_C=1μF

To find Bypass capacitor C_E:

$$X_{CE} \leq 0.1R_E$$
$$\text{i.e } \frac{1}{2\pi C_E f} \leq 0.1R_E$$
$$\therefore C_E \geq \frac{1}{0.2\,\pi f R_E} = 28.4\mu 8$$

Choosing C_E=47μF

Voltage gain:

$$A_V = -\frac{R_C}{r_e} = -\frac{2.2K}{13} = -169$$

Negative sign indicates the phase shift of 180° between input & output

$V_o=A_V*V_{in}$

For $V_{in(p-p)}$=20mV $V_{o(p-p)}$= -3.38 V

Circuit diagram:

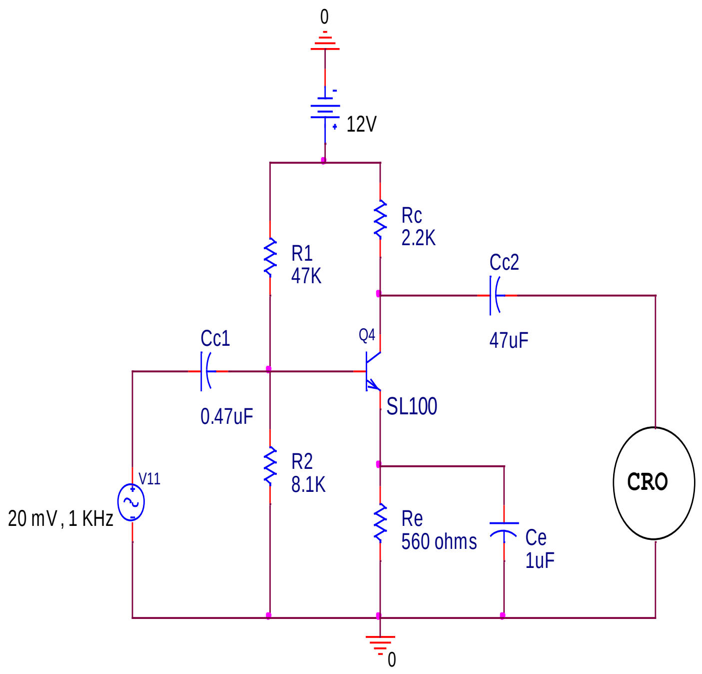


Fig. 3.1: Circuit diagram for RC Coupled amplifier.

Table 3.1: Table for RC Coupled amplifer

V_i= 20mV

Frequency in Hz	$V_{o(p-p)}$	$A_V = \frac{V_o}{V_i}$	Gain in dB=$20\log_{10}(V_o/V_i)$
500Hz			
1MHz			

Expected Waveform:

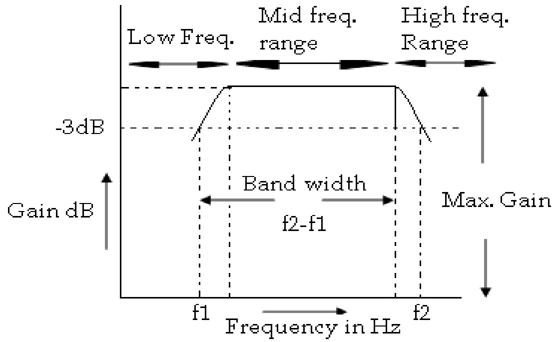


Fig. 3.2: Frequency response graph for RC Coupled amplifier.

Calculations:

Lower cut off frequency f_L=------Hz

Upper cut off frequency f_U=------Hz

Bandwidth BW=f_U-f_L

Procedure:

1. Connections are made as shown in circuit diagram
2. Set Vcc as 12V, and check the DC biasing conditions such that V_{CE} should be approximately equal to (V_{CC}/2) i,e 6V and V_{BE}=0.7V
3. If the DC biasing conditions satisfy then set the signal generator (input-voltage) amplitude (peak-to-peak sine wave) as 20mV
4. Vary the frequency of the input from lower range to higher range(i,e from 100Hz to 1MHz). Observe both input and output simultaneously on the CRO. Note the outputs voltage (peak to peak value) corresponding to the variation in frequencies of the input signal at different intervals. The output voltage remains constant at mid frequency range.
5. Calculate the gain and gain in DB corresponding to different values of frequencies
6. Plot the graph with frequency along X-axis and gain dB along Y-axis on semi log graph sheet
7. From the graph determine the bandwidth.

Procedure to find input impedance

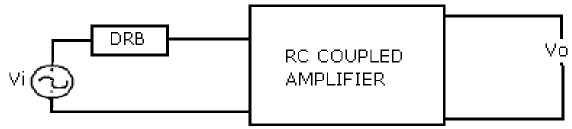


Fig. 3.3: Circuit diagram for finding input impedance of a RC Coupled amplifier

1. Connect the circuit as shown in above figure.
2. Set the following
   - DRB to 0Ω
   - Input sine wave frequency to any mid frequency.
3. Measure amplitude of output voltage waveform (Peak to peak Value). And denote it by V_a.
4. Increase DRB from minimum value (keeping V_i constant) till $V_o=\frac{Va}{2}$ .The corresponding DRB reading gives the input impedance Z_i in RC coupled amplifier.

Procedure to find Output impedance

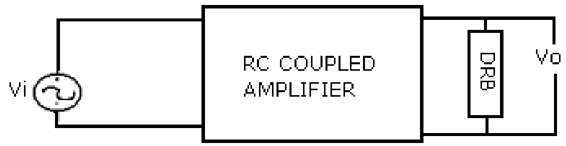


Fig. 3.3: Circuit diagram for finding output impedance of a RC Coupled amplifier

1. Connect the circuit as shown in above figure.
2. Set the following
   - DRB to maximum value
   - Input sine wave frequency to any mid frequency.
3. Measure amplitude of output voltage waveform (Peak to peak Value). And denote it by V_b.
4. Decrease DRB from maximum value (keeping V_i constant) till $V_o = \frac{Vb}{2}$. The corresponding DRB gives output impedance, Z_o of Amplifier.

Conclusion:

Viva Questions:

1. What is Amplification?
2. What is transistor biasing?
3. What are different types of transistor biasing?
4. What are the Different types of Amplifiers?
5. State the Differences between BJT and FET?
6. Define operating point?
7. What are the different regions of operations of Transistor?
8. What is Stability Factor?
9. What are the different types of stability factors?

Preparation(4)	Conduction(4)	Result/Conclusion(5)	Total(13)

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Signature with date

Experiment No: 05 **Date:**

Design and testing of BJT-RC phase shift oscillator for given frequency of oscillation

objective: To design and test the performance of BJT RC phase shift oscillator for f_0=10 KHz

Apparatus Required:

SL.No	Particular	Range	Quantity
1	Bread board		
2	CRO		
3	Power supply	DC 0-20V	
4	Transistor	SL100	
5	Resistors	47KΩ, 8.1KΩ, 2.2 KΩ, 560Ω	
6	Potentiometer	10K	
7	Capacitors	47uF, 1uF,	

Theory: The oscillators are an important class of circuits that are used in almost every electronics systems. These are used to produce sinusoidal and square wave forms. The square wave is used as clocks in computers & other digital systems. Oscillators are basically an amplifier with positive feedback. No input signal is required to start oscillator only certain conditions are required to be fulfilled for sustained oscillation, they are.

- The loop gain of the circuit must be equal to 1
- The phase shift around the circuit is zero

These two condition is called barkhausen criteria.

The RC phase shift oscillators are low frequency oscillators. These will generate oscillations in audio frequency range. The feedback network consist of three identical RC sections. The R &C values must be selected such that each RC section should provide a phase shift of 60° at desired frequency of oscillation. Hence 180° phase shift will be introduced from 3 RC sections.

The frequency of oscillation is given by,

$$f = \frac{1}{2\pi RC\sqrt{6+4\frac{R_C}{R}}}$$

For closed loop gain to be equal to one, the current gain of the transistor (h_{fe}) must satisfy the condition

$$h_{fe} \geq 23 + 29\frac{R}{R_C} + 4\frac{R_C}{R}$$

Circuit diagram:

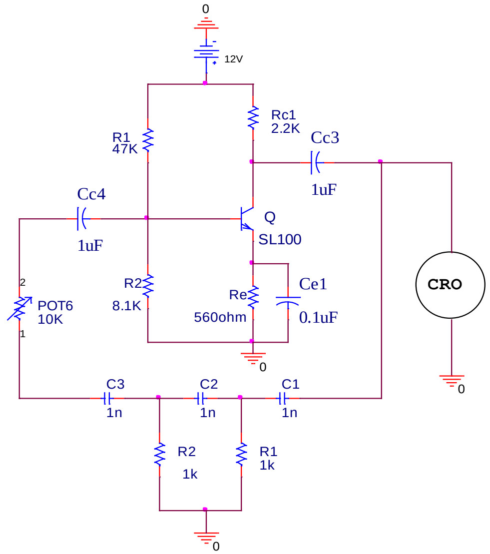


Fig4.1: RC phase shift oscillator

Design:

Let us consider V_{CC}=12V, β=145, I_C=2mA to make transistor to work in active region.

Approximations

$$I_E \cong I_C$$

$$V_E \cong \frac{V_{CC}}{10} = 1.2V$$

$$V_{CE} \cong \frac{V_{CC}}{2} = 6V$$

$V_B=V_{BE}+V_E$=1.2+0.7=1.9V

To find R_E:

W.K.T $V_E=I_ER_E$

$$R_E = \frac{V_E}{I_C} = 600$$

Choosing R_E=560Ω

To find R_C:

Applying KVL to output circuit

$V_{CC}=I_CR_C+V_{CE}+I_ER_E$

$$R_C = \frac{V_{CC} - V_{CE} - I_C R_E}{I_C} = 2400\Omega$$

Choosing R_C=2.2KΩ

To find R_1 & R_2:

$$R_2 \le \frac{\beta R_E}{10}$$

$$R_2 \le \frac{560 \times 145}{10} = 8120\Omega$$

Choosing R_2=8.1KΩ

From the circuit $V_B = \frac{V_{CC} \times R_2}{R_1 + R_2}$

R_2=43058Ω

Choosing R_2=47KΩ

To find coupling capacitors C_C:

$$f_L = \frac{1}{2\pi(R_i + R_S)C_C}$$

$$\text{usually } R_S << R_i$$

$$R_i = R_1 ll\ R_2 ll\ \beta r_e$$

$$r_e = \frac{26mV}{I_E} = 13$$

$$R_i = 47K ll\ 8.1K ll\ (145*13)$$

$$R_i = 1.5K$$

Let f_L=100Hz

$$\therefore C_{in} = \frac{1}{2\pi \times R_i \times f_L} = 1.06\mu F$$

Choosing C_C=1μF

To find Bypass capacitor C_E:

$$X_{CE} \le 0.1R_E \quad \text{i.e} \quad \frac{1}{2\pi\pi f_E} \le 0.1R_E$$

$$\therefore C_E \ge \frac{1}{0.2\pi.2\ _E} = 28.4\mu F$$

Choosing C_E=47μF

Feedback network:

The R &C values must be selected such that each RC section should provide a phase shift of 60° at desired frequency of oscillation. Hence 180° phase shift will be introduced from 3 RC sections.

From phasor diagram $\phi = \tan^{-1}\left(\frac{X_C}{R}\right)$

$$\therefore \frac{X_C}{R} = \tan 60 = 1.73$$

Choose C=1nF then X_C=15915Ω

$$R = \frac{15915}{1.73} = 9188\Omega$$

Choosing R=8.1KΩ

Check condition for sustained oscillation

$$h_{fe} \ge 23 + 29\frac{R}{R_C} + 4\frac{R_C}{R}$$

$$145 \ge 131$$

Hence the condition is satisfied.

Procedure:

1. Make the Connections as shown in circuit diagram.
2. Set Vcc as 12V, and check the DC biasing conditions such that V_{CE} should be approximately equal to (V_{CC}/2) i,e 6V and V_{BE}=0.7V.
3. Vary 10KΩ potentiometer so as to get an undistorted sine wave at the output.
4. Note the phase shift between 3 sections of RC network with respect to the output wave.
5. Sketch the output wave and waveforms at 3 sections of RC network.

Result

F_o in KHz	θ_1	θ_2	θ_3
Theoretical	**60**	**120**	**180**
Practical			

Observation: The RC phase shift oscillator circuit is designed and studied. The crystal frequency and practical frequency of oscillations was found to be almost matching

Vive Voce

1. Define Oscillator.
2. Give the difference between positive feedback and negative feedback.
3. Mention the types of oscillator circuits.

Preparation(4)	Conduction(4)	Result/Conclusion(5)	Total(13)

Signature with date

EXPERIMENT NO. 6:

Design and testing of Hartley and Colpitt's oscillator for given frequency of oscillation

Objective: To design and test the performance of BJT colpitts and Hartley oscillator for radio frequency range of f_0=100 Khz.

Components required:

Component	Specification
Bread board	
CRO	
Power supply	DC 0-20V
Signal generator	0-2Mhz
Transistor	SL100
Resistors	47KΩ, 8.1KΩ, 2.2 KΩ, 560Ω
Capacitors	47uF, 1uF,
DIB	
DCB	

Theory: These are basically tuned oscillators. These oscillators are used to generate oscillations in frequency ranging from 100KHz to hundred of MHz. The split capacitor or inductor arrangement is called the tank circuit and this introduces the required 180° phase shift for output voltage.

Hartley oscillator:

Circuit diagram:

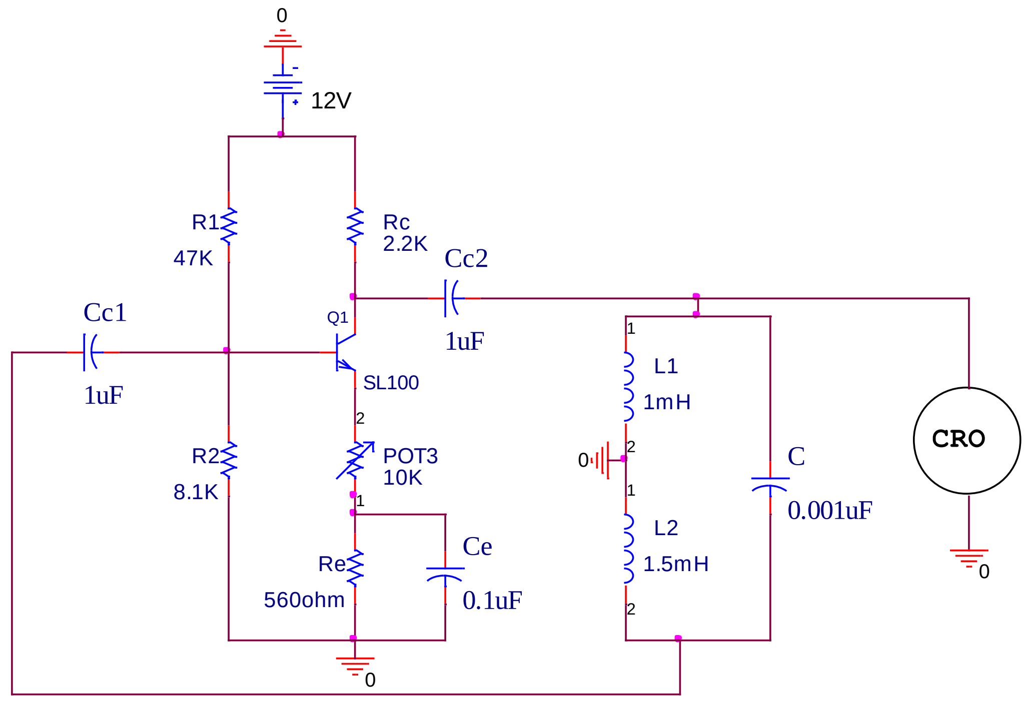


Fig. 9.1: Hartley oscillator circuit

Design:

Let us consider V_{CC}=12V, β=145, I_C=2mA to make transistor to work in active region.

Approximations

$$I_E \cong I_C$$

$$V_E \cong \frac{V_{CC}}{10} = 1.2V$$

$$V_{CE} \cong \frac{V_{CC}}{2} = 6V$$

$V_B=V_{BE}+V_E=1.2+0.7=1.9V$

To find R_E:

W.K.T $V_E=I_ER_E$

$$R_E = \frac{V_E}{I_C} = 600$$

Choosing $R_E=560\Omega$

To find R_C:

Applying KVL to output circuit

$V_{CC}=I_CR_C+V_{CE}+I_ER_E$

$$R_C = \frac{V_{CC} - V_{CE} - I_C R_E}{I_C} = 2400\Omega$$

Choosing $R_C=2.2K\Omega$

To find R_1 & R_2:

$$R_2 \le \frac{\beta R_E}{10}$$

$$R_2 \le \frac{560 \times 145}{10} = 8120\Omega$$

Choosing $R_2=8.1K\Omega$

From the circuit $V_B = \frac{V_{CC} \times R_2}{R_1 + R_2}$

$R_2=43058\Omega$

Choosing $R_2=47K\Omega$

To find coupling capacitors C_C:

$$f_L = \frac{1}{2\pi\pi(_i + R_S)C_C}$$

usually $R_S << R_i$

$R_i = R_1 ll\, R_2 ll\, \beta r_e$

$$r_e = \frac{26mV}{I_E} = 13$$

$R_i = 47Kll\, 8.1Kll\, (145*13)$

$R_i = 1.5K$

Let $f_L=100Hz$

$$\therefore C_{in} = \frac{1}{2\pi \times R_i \times f_L} = 1.06\mu F$$

Choosing $C_C=1\mu F$

To find Bypass capacitor C_E:

$X_{CE} \le 0.1R_E$

$$\text{i.e } \frac{1}{2\pi\pi f_E} \le 0.1R_E$$

$$\therefore C_E \ge \frac{1}{0.2\pi.2_E} = 28.4\mu 8$$

Choosing $C_E=47\mu F$

Tank circuit:

The frequency of oscillation is determined by LC tank circuit

$$f = \frac{1}{2\pi\sqrt{L_{eq}C}} \text{ where } L_{eq} = L_1 + L_2$$

for f=100Khz, Let C=0.001µF

$$L_{eq} = \frac{1}{4\pi^2 f^2 C}$$

By solving the above equation we get L_1=1mH and L_2=1.5mH

Procedure:

- Make the connections as shown in the circuit diagram.
- Initially set potentiometer to minimum value.
- Set Vcc as 12V, and check the DC biasing conditions such that V_{CE} should be approximately equal to ($V_{CC}/2$) i,e 6V and V_{BE}=0.7V
- Set the designed values of inductors and capacitor in DIB and DCB respectively.
- Vary 10KΩ potentiometer so as to get an undistorted sine wave at the output.
- Note down the frequency of the output wave and compare it with the theoretical frequency of oscillation.

Observation:

Theoretical value of f_o	Practical value of f_o	Amplitude of sine wave
100Khz		

Colpitts oscillator:

Circuit diagram:

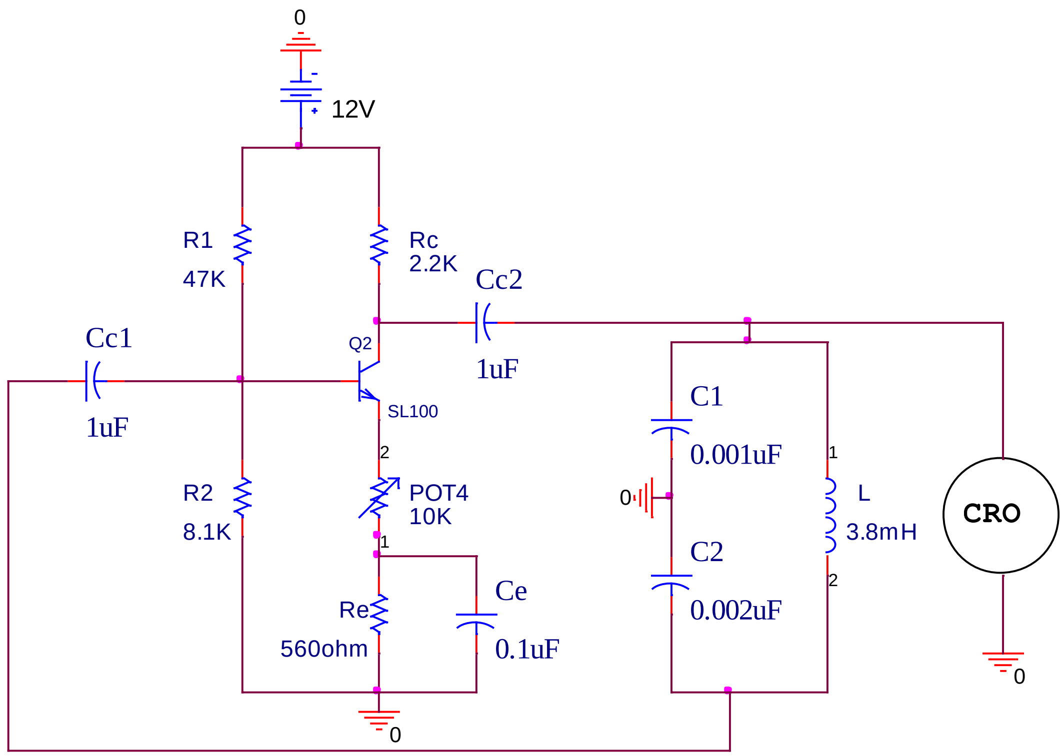


Fig. 9.2: Colpitts oscillator circuit

Tank circuit design:

The frequency of oscillation is determined by LC tank circuit

$$f = \frac{1}{2\pi\sqrt{LC_{eq}}} \text{ where } C_{eq} = C_1 \| C_2$$

for f=100Khz, Let C_1=0.001μF and C_2=0.002μF then C_{eq}=0.661nF

$$L_{eq} = \frac{1}{4\pi^2 f^2 C}$$

By solving the above equation we get L=3.8mH

Procedure:

- Connections are made as shown in circuit diagram.
- Initially set potentiometer to minimum value.
- Set Vcc as 12V, and check the DC biasing conditions such that V_{CE} should be approximately equal to (V_{CC}/2) i,e 6V and V_{BE}=0.7V
- Set the designed values of inductor and capacitor in DIB and DCB respectively.
- Vary 10KΩ potentiometer so as to get an undistorted sine wave at the output.
- Note down the frequency of the output wave and compare it with the theoretical frequency of oscillation.

Observation:

Theoretical value of f_o	Practical value of f_o	Amplitude of sine wave
100Khz		

Result:

The Hartley and colpitts oscillator was designed and studied. The theoretical and practical frequency of oscillations was found to be almost matching

Outcome: at the end of the experiment,

- It helps the students to learn the basic working of LC circuits.
- On completion of the experiment the student understands why LC oscillators are used for high frequency range.

Experiment No: 07 **Date:**

Determination of gain, input and output impedance of BJT Darlington emitter follower with and without bootstrapping

Objective: To Design a BJT Darlington emitter follower and determine the gain, input and output impedances.

Apparatus Required:

SL.No	Particular	Range	Quantity
1	Bread board		1
2	transistor	NPN SL100/CL100	1
3	Resistor		1
4	Power supply	DC 0-20V	1
5	Signal generator	0-2MHz	1
6	CRO		1
7	DRB	0-1MΩ	1
8	Connecting wires an probe		1
9	Capacitors	47uF, 0.47uF	2

Design:

Let V_{CC}= 12V, I_{C2} = 10mA, and β = 100

$$V_{E2} = \frac{V_{CC}}{2}$$

$$= \frac{12}{2} = 6V$$

$$R_E = \frac{V_{E2}}{I_{C2}}$$

$$= \frac{6}{10mA} = 600\Omega = 560\Omega$$

$V_{R2} = V_{BE1} + V_{BE2} + V_{E2} = 0.7+0.7+6=7.4V$

$V_{R1} = V_{CC} - V_{R2}$ = 12-7.4=4.6V

Assume 10 I_{B1} through R_1 and 9I_{B1} through R_2

i.e V_{R1}=10 I_{B1}* R_1

V_{R2}= 9I_{B1}* R_2--------- 1

To find I_{B1}, consider the circuit diagram from the circuit diagram I_{C1}= I_{E1}, but I_{E1} =I_{B2}.

Wkt I_{C2}=β I_{B2}

I_{B2} = I_{C2}/ β

I_{B2} = I_{C1}/ β = 1µA.

From equation 1 we have

R_1= 460KΩ

R_2= 822.22KΩ=822KΩ = 1MΩ

Assume C_{C1}= C_{C2}= 0.47µF.

Circuit diagram:

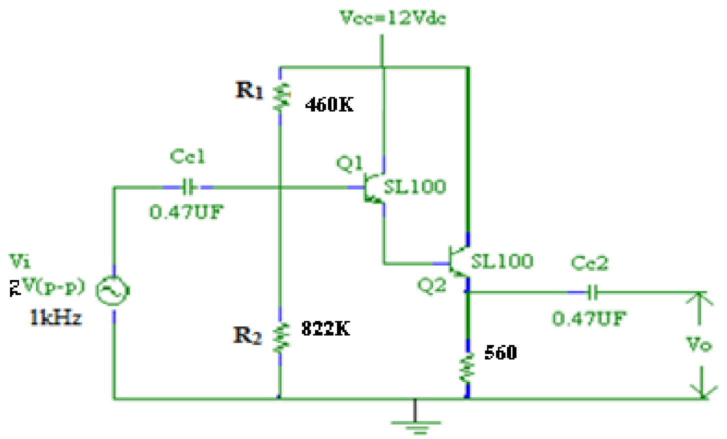


Fig.5.1: Darlington emitter follower without bootstrapping.

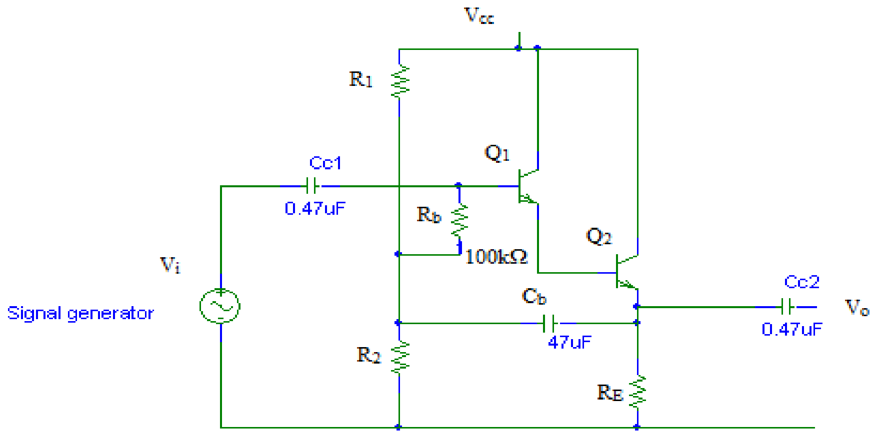


Fig.5.2: Darlington emitter follower with bootstrapping.

Procedure:

1. Connections are made as shown in circuit diagram
2. Set Vcc as 12V, and check the DC biasing conditions such that V_{CE} should be approximately equal to (V_{CC}/2) i,e 6V and V_{BE}=0.7V
3. If the DC biasing conditions satisfy then set the signal generator (input-voltage) amplitude (peak-to-peak sine wave) as 2 V (p-p)
4. Vary the frequency of the input from lower range to higher range(i,e from 100Hz to 1MHz). Observe both input and output simultaneously on the CRO. Note the outputs voltage (peak to peak value) corresponding to the variation in frequencies of the input signal at different intervals. The output voltage remains constant at mid frequency range.
5. Calculate the gain and gain in DB corresponding to different values of frequencies
6. Plot the graph with frequency along X-axis and gain dB along Y-axis on semi log graph sheet
7. From the graph determine the bandwidth.
8. Determine the input and output impedance as explained below.
9. Connect the bootstrap circuit R_b and C_b between the emitter and base as shown in the circuit. Repeat the steps

Procedure to find input impedance

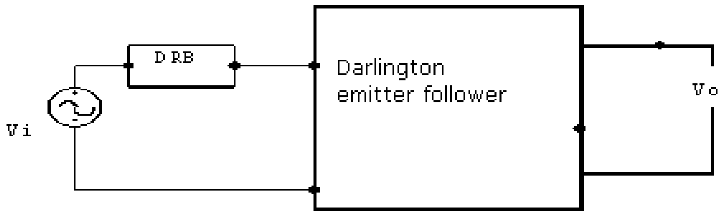


Fig.5.3: Circuit to find input impedance

1. Connect the circuit as shown in above figure.
2. Set the following
   - DRB to 0Ω
   - Input sine wave frequency to any mid frequency.

3. Measure amplitude of output voltage waveform (Peak to peak Value). And denote it by V_a.
4. Increase DRB from minimum value (keeping V_i constant) till $V_o = \frac{Va}{2}$ .The corresponding DRB reading gives the input impedance Z_i in RC coupled amplifier.

Procedure to find Output impedance

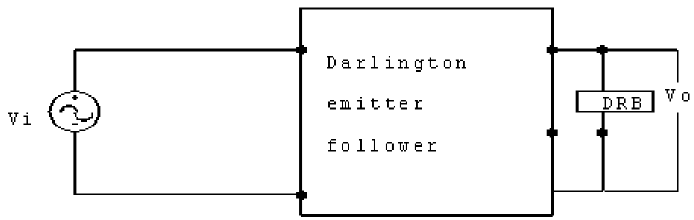


Fig.5.4: Circuit to find output impedance

1. Connect the circuit as shown in above figure.
2. Set the following
   - DRB to maximum value
   - Input sine wave frequency to any mid frequency.
3. Measure amplitude of output voltage waveform (Peak to peak Value). And denote it by V_b.
4. Decrease DRB from maximum value (keeping V_i constant) till $V_o = \frac{Vb}{2}$ .The corresponding DRB gives output impedance, Z_o of Amplifier.

Table 5.1: Table for RC Coupled amplifier without Boost strapping

Frequency in Hz	$V_{o(p-p)}$	$A_V = \frac{V_o}{V_i}$	Gain in dB=$20\log_{10}(V_o/V_i)$
500Hz			

Table 5.2: Table for RC Coupled amplifier with Boost strapping

Frequency in Hz	$V_{o(p-p)}$	$A_V = \frac{V_o}{V_i}$	Gain in dB=$20\log_{10}(V_o/V_i)$
500Hz			

Table 5.3: Table for Input and output impedance

Parameters	Z_i	Z_o
Without Bootstrap		
With bootstrap		

Expected Waveform:

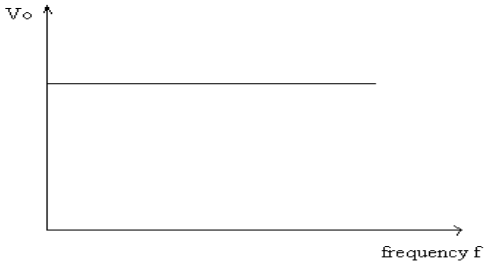


Fig. 3.2: Frequency response graph for Darlington amplifier.

Conclusion:

Vive Voce

1. What do you understand by Emitter Follower?
2. What are the applications of Emitter Follower?
3. Define Bootstrap?
4. Differentiate Emitter follower with and without Bootstrap?
5. Which type of biasing technique is used in emitter follower?
6. What's the Voltage gain of emitter follower?
7. What's the Current gain of emitter follower?
8. What is nature of frequency response of emitter follower?
9. What is the procedure to find input impedance?
10. What is the procedure to find input impedance?

Preparation(4)	Conduction(4)	Result/Conclusion(5)	Total(13)

Signature with date

EXPERIMENT NO: 8

Design and testing of Class A and Class B power amplifier and to determine conversion efficiency.
CLASS –B PUSH PULL POWER AMPLIFIER

Objective: To determine the conversion efficiency of Class A & Class B, Power Amplifier.

COMPONENTS/APPARATUS REQUIRED:

Component	Specification
Bread board	
CRO	
Signal Generator	
Power supply	DC 0-20V
Transistor	SL100 (2 nos)
Resistors	1K, 47K, 4.7K, 10K pot
Capacitors	0.1uF
Connecting Wires	

CIRCUIT DIAGRAM:

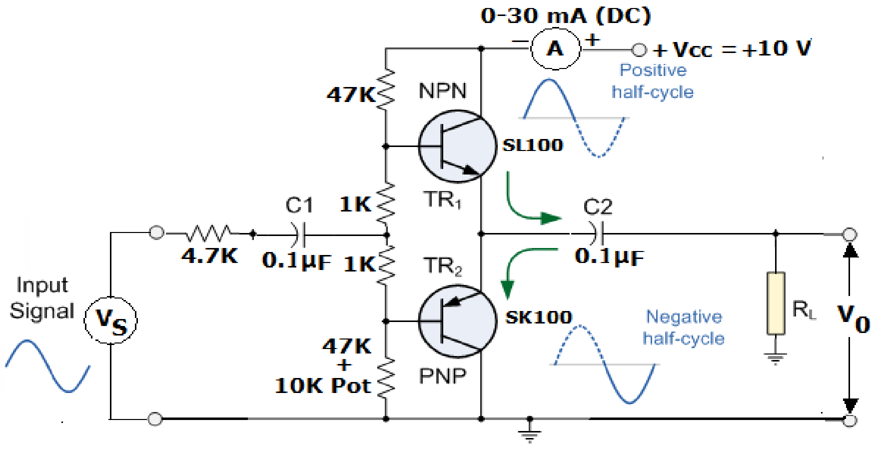


Fig 12.1: Circuit Set Up

Theory:

One of the main disadvantages of the Class B amplifier circuit is that it uses balanced center-tapped transformers in its design, making it expensive to construct. However, there is another type of Class B amplifier called a **Complementary-Symmetry Class B Amplifier** that does not use transformers in its design. Therefore it is transformer less, using instead complementary or matching pairs of power transistors. As transformers are not needed, this makes the amplifier circuit much smaller for the same amount of output. Also there are no stray magnetic effects or transformer distortion to affect the quality of the output signal. A "transformer less" Class B amplifier circuit is given in Fig 1.

The Class B amplifier circuit above uses complimentary transistors for each half of the waveform and while Class B amplifiers have a much high efficiency than the Class A types, one of the main disadvantages of class B type push-pull amplifiers is that they suffer from an effect known commonly as ***Crossover Distortion***. Remember from Basic knowledge of Transistors that it takes approximately 0.7 volts (measured from base to emitter) to get a bipolar transistor to start conducting. In a pure class B amplifier, the output transistors are not "pre-biased" to an "ON" state of operation.

This means that the part of the output waveform which falls below this 0.7 volt window will not be reproduced accurately as the transition between the two transistors (when they are switching over from one to the other), the transistors do not stop or start conducting exactly at the zero crossover point even if they are specially matched pairs. The output transistors for each half of the waveform (positive and negative) will each have a 0.7 volt area in which they will not be conducting resulting in both transistors being "OFF" at the same time. Fig 2 and Fig 3 illustrate the reason and concept of crossover distortion.

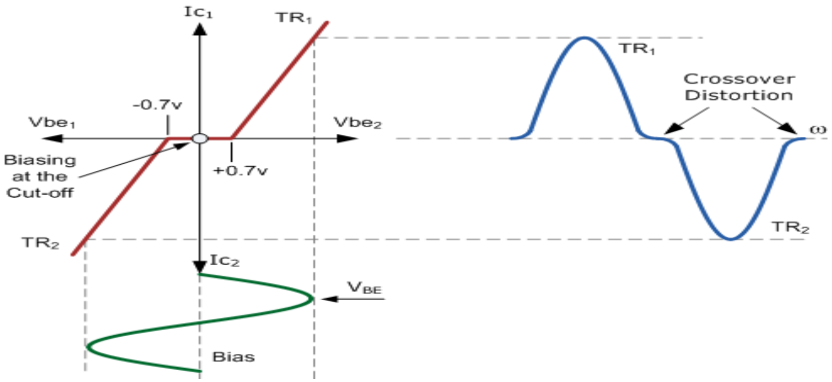


Fig 12.2: Nonlinear Characteristic of Class B Operation

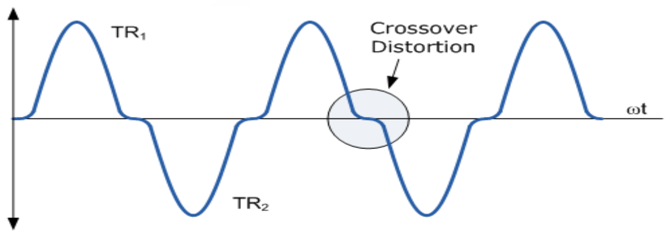


Fig 12.3 Illustrating Cross-over distortion

PROCEDURE:

1. Wire the circuit as in Fig 1.

2. Adjust the 10K pot to get $V_{CE1} = V_{CE2} = 5$ V

3. Measure and record V_{BE1} and V_{BE2}

4. Give a sine wave input of frequency 1 KHz and observe the output.

5. Determine the output impedance of the amplifier and record. (Say 60Ω)

6. Vary R_L in the range 30Ω to 80Ω in steps. (Take 5 readings on either side of R_0)

7. **For each value of R_L adjust the signal amplitude to get "Maximum Un – distorted Output"**

8.For each R_L setting, Record R_L, I_{dc}, V_o peak to peak and compute the conversion efficiency as shown in the table.

9. Plot a graph of η vs. R_L and determine the optimum load and maximum efficiency

TABULAR COLUMN

Sl.No	R_L In Ω	I_{dc} mA	V_o(P-P) in V	$P_{dc} = V_{cc} \times I_{dc}$	$P_o = [V_0(P-P)^2]/8R_L$	η = $(P_o/P_{dc}) \times 100$ %	Remarks
1	30						
2	40						
3	50						
4	60						
5	70						
6	80						

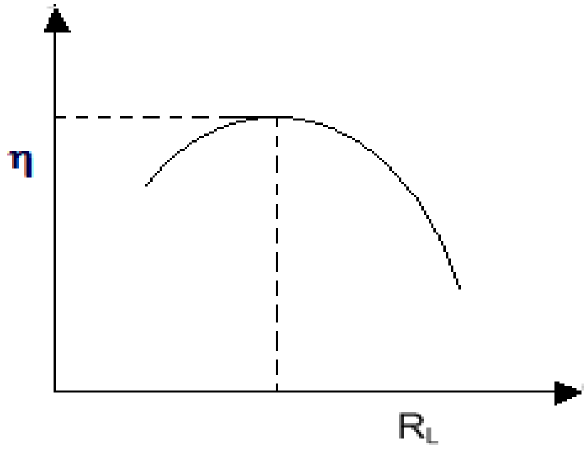
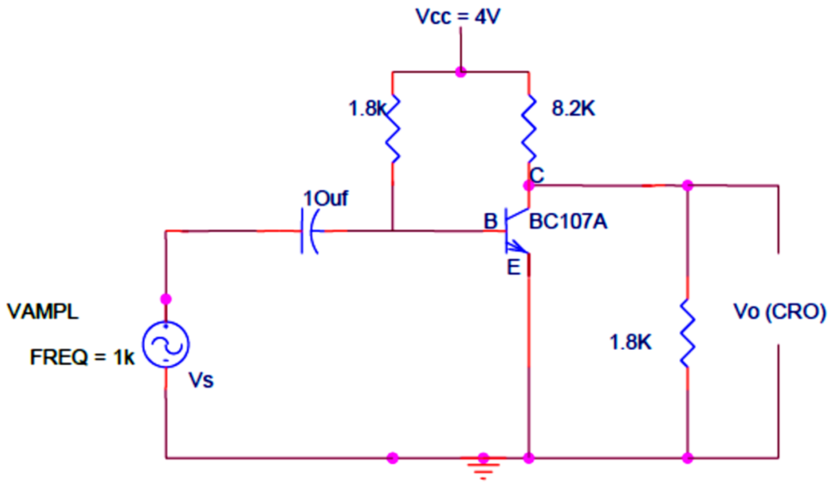


Fig 12.4: Efficiency versus Load graph

Class-A power amplifier



CIRCUIT DIAGRAM

PROCEDURE:

1. The circuit is connected as shown in figure
2. An input voltage of 1V and a frequency of 1KHz is applied with the help of signal generator
3. Observe the output undistorted waveform
4. Note the Vp-p value
5. Using Multimeter calculate the voltage across Rc and calculate the current Ic in RL
6. Now calculate the practical efficiency using formula given
7. Compare the practical efficiency and theoretical efficiency

$$\%\eta = \frac{Pac\,(\text{ac output power})}{Pdc\,(\text{dc input power})} * 100$$

The DC input power is provided by the supply

$P_{DC} = V_{CC} * I_{CQ}$

A.C. Output power delivered by the amplifier to the load expressed by

1. Using peak Value

$$P_{ac} = V_{rms} I_{rms} = \frac{V_m I_m}{2} = \frac{I_m 2 R_L}{2} = \frac{V_m 2}{2R_L} = \frac{V_{pp} 2}{8R_L}$$

Or

$$P_{ac} = \frac{I_{pp} 2\; RL}{8}$$

Experiment-9
Design, simulation (MATLAB) and testing of Wien bridge oscillator for given frequency of oscillation.

Objective: To Design, simulation of Wien bridge oscillator using BJT and determination of frequency of oscillation.

Components required:

Component	Specification
Bread board	
CRO	
Power supply	DC 0-20V
Signal generator	0-2Mhz
Transistor	BC107
Resistors	2.4KΩ, 9.4KΩ, 50.5KΩ, 600Ω, 1.2KΩ, 4.7KΩ pot
Capacitors	44uF, 34nF,

Design Wein-bridge Oscillator using BJT to generate 1KHz Sinewave

Output requirements

Fo = 1 KHz

Vo(p-p) =12V

DC Bias Conditions

V_{CC} =12V

Ic = 2mA

V_{CE} = 50% of V_{CC} = 6V

V_{RC} = 40% of VCC = 0.4*12 = 4.8V

V_{RE} =10% of V_{CC} = 0.1*12 = 1.2V

Design Collector Resistor Rc

$$R_C = \frac{VRC}{Ic} = \frac{4.8}{2*10^{-3}} = 2.4\ K\Omega$$

Ic ≈ I_E

Design Emitter Resistor R_E

$$R_E = = \frac{VRE}{Ic} = \frac{1.2}{2*10^{-3}} = 600\ \Omega$$

Design of Voltage divider resistance R_5 and R_6

$I_C = \beta I_B$

$I_C = h_{Fe} * I_B$

Let h_{Fe}=100

$$I_B = \frac{I_C}{h_{Fe}}$$

$$I_B = \frac{I_C}{h_{Fe}} = \frac{2*10^{-3}}{100} = 20\ \mu A$$

Assume current through $R_5 = 10I_B$, and that through $R_6 = 9I_B$ to avoid loading

$V_{R6} = V_{BE} + V_{RE}$ = 0.7+1.2V = 1.9V

$V_{R6} = 9I_B * R_6$

$1.9 = 9*(20*10^{-6}) * R_6$

$R_6 = \frac{1.9}{9*20*10^{-3}} = 9.4\ k\ \Omega$

$VR_5 = Vcc - V_{R6}$

$VR_5 = 12 - 1.9V = 10.1V$

$VR_5 = 10 I_B * R_5$

$R_5 = \frac{VR_5}{10 I_B} = \frac{10.1}{10*20*10^{-6}} = 50.5\ K\ \Omega$

$R_5 = 50.5\ K\Omega$

Design of coupling capacitor Cc,

$F = \frac{1}{2\pi\ (R_1 II\ R_2 II\ h_{Fe} Re)\ Cc}$

$Cc = 44\ \mu F$

Design of Feedback Network

The frequency of oscillations is determined by the series element R_1C_1 and parallel element R_2C_2 of the bridge

$$f = \frac{1}{2\pi\sqrt{R1R2C1C2}}$$

If $R_1 = R_2 = R$ and $C_1 = C_2 = C$ then $f = \frac{1}{2\pi RC}$

Frequency of Oscillation, $Fo = \frac{1}{2\pi RC} = 1KHz$

Let $R = 4.7K\Omega$

$C = 33.87\ nF$

$\frac{R_3}{R_4} = 2$, $K_{min} = 2$

$R_3 = 2R_4$

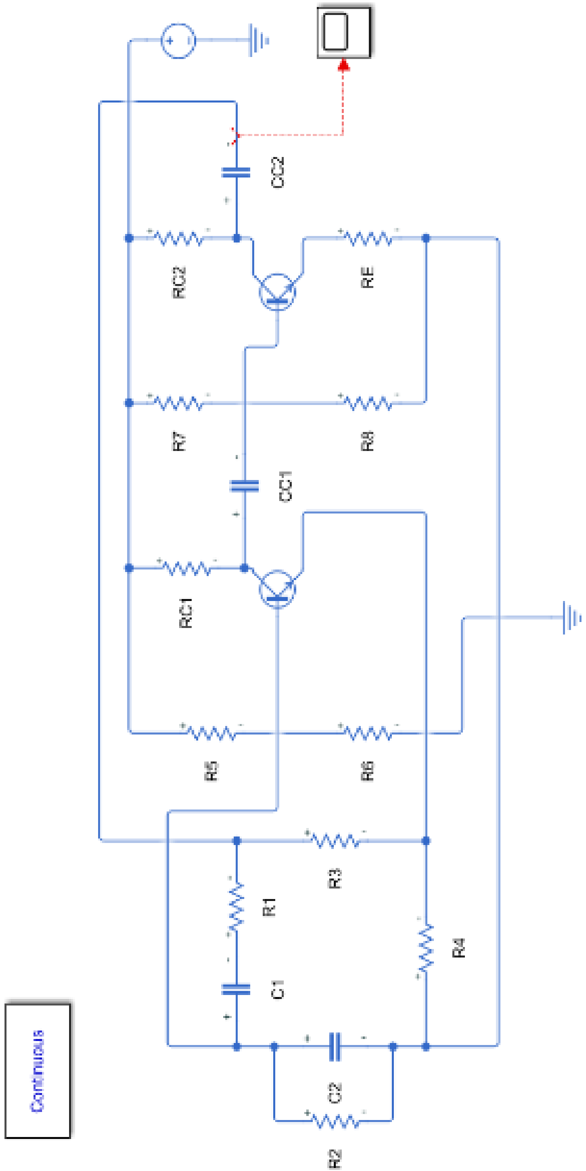
Let $R_4 = 600\ \Omega$

R3 = 1.2 KΩ, Use Pot 4.7 K Ω

Design Parameters

Fo=1KHz, Vo(p-p) =12V
Vcc = 12V, Ic=2mA
Rc = 2.4 KΩ (R_{C1}, R_{C2})
$R_E = 600\Omega$
Let $h_{Fe}=100$
$R_6 = R_8 = 9.4K\ \Omega$
$R_5 = R_7 = 50.5K\Omega$
Cc = 44 μF (C_{C1}, C_{C2})
$R_1 = R_2 = R = 4.7\ K\ \Omega$, $C_1 = C_2 = C = 33.87nF$
$R_4 = 600\Omega$, $R_3 = 1.2\ K\Omega$ (Use 4.7KΩ Pot)

Circuit Diagram



Procedure:

1. Make the Connections as shown in circuit diagram.
2. Set Vcc as 12V, and check the DC biasing conditions such that V_{CE} should be approximately equal to ($V_{CC}/2$) i,e 6V and V_{BE}=0.7V.
3. Vary 4.7KΩ potentiometer so as to get an undistorted sine wave at the output.
4. Note down the frequency of the output wave and compare it with the theoretical frequency of oscillation.

Open MATLAB and then open Simulink using the 'Simulink' icon on MATLAB, under Simulink library browser click on 'File' for New Simulink model. Under Simulink library browser click on 'simPowersystems', Select required component, right click on the component to add(Place) it to editor and build/complete the circuit and Start simulation.

Observation:

	Frequency of oscillation F_o	Amplitude of sine wave
Theoretical value		
Practical value		
Simulation value		

Result:

The Design Wein-bridge Oscillator using BJT oscillator was designed simulated (MATLAB) and Tested. The theoretical, practical & Simulated frequency of oscillations was found to be almost matching

Outcome: at the end of the experiment,

- On completion of the experiment the student understands design, working, Simulation of Wein-bridge oscillators used to generate high frequency Sine wave.

Experiment-10

Design and simulation of Full wave – centre tapped transformer type and Bridge type rectifier circuits with and without Capacitor filter using MATLAB. Determination of ripple factor, regulation and efficiency.

Objective: Design and simulation of Full wave – centre tapped transformer type and Bridge type rectifier circuits with and without Capacitor filter using MATLAB and determination of ripple factor, regulation and efficiency.

Software: Matlab 2010 and above

Theory:

- Rectifiers are used to convert an AC power to a DC power. Among the rectifiers, the bridge rectifier is the most efficient rectifier circuit.
- Many electronic circuits require a rectified DC power supply to power various electronic basic components from the available AC mains supply.
- We can define bridge rectifiers as a type of full-wave rectifier that uses four or more diodes in a bridge circuit configuration to efficiently convert alternating (AC) current to a direct (DC) current.

Rectifier is a circuit which converts AC to pulsating DC. Rectifiers are used in construction of DC power supplies. There are three types of rectifiers namely Half wave rectifier, Centre tap full wave rectifier and bridge rectifier.

In half wave rectification, either the positive or negative half of the AC wave is passed, while the other half is blocked. Because only one half of the input waveform reaches the output, it is very inefficient if used for power transfer.

A full-wave rectifier converts the whole of the input waveform to one of constant polarity (positive or negative) at its output. Full-wave rectification converts both polarities of the input waveform to DC (direct current), and is more efficient. Fullwave rectification can be obtained either by using center tap transformer or by using bridge rectifier.

The output of a rectifier is not a smooth DC it consists of ac ripples therefore to convert this pulsating DC in to smooth DC we use a circuit called filter. There are many types of filters like C filter, L filter, LC filter, multiple LC filter, πfilter etc..of all these C filter is the most fundamental filter.

Circuit Diagram:

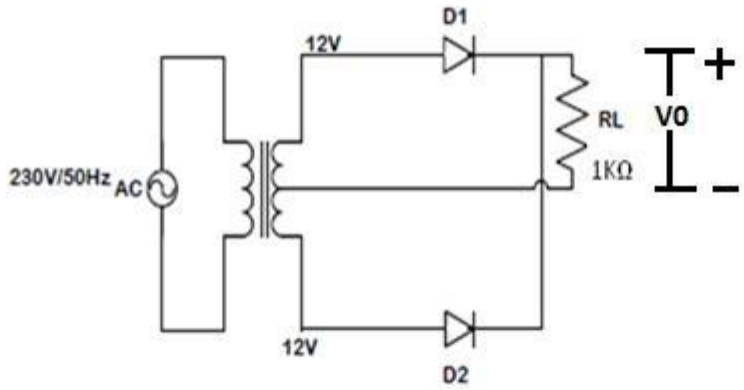


Fig. 1.1 Circuit of full wave rectifier without filter

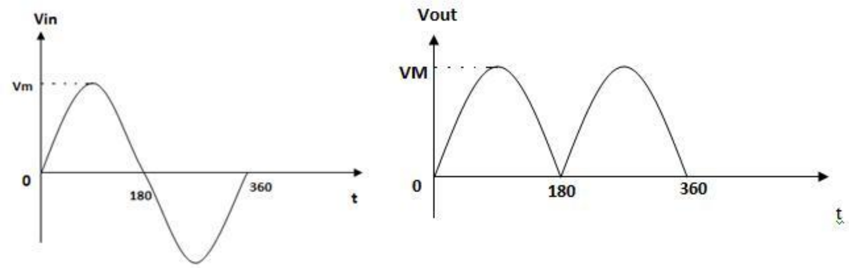


Fig. 1.2 Waveform for full wave rectifier without filter

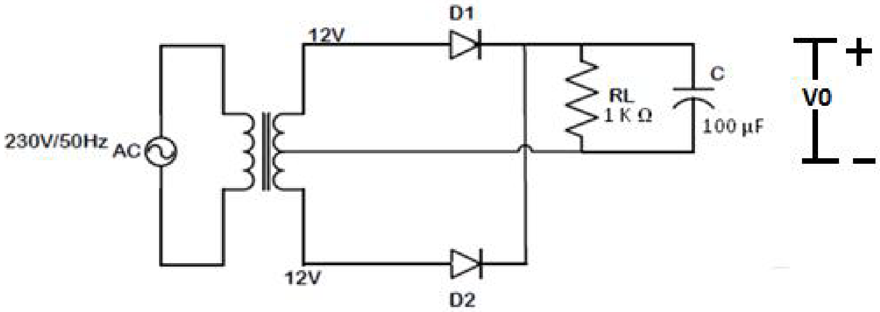


Fig. 1.3 Circuit of full wave rectifier with capacitor filter

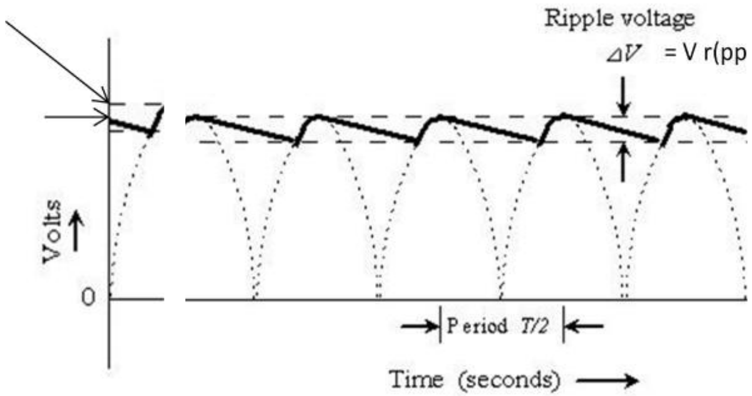


Fig. 1.4 Waveform for full wave rectifier with filter

Theoretical Calculations:

Full wave rectifier without Capacitor filter

Under No Load

$V_{M\,(NL)}$ = ___________V (Peak value of voltage from CRO)

V_{DC} is dc (average) value, $V_{DC\,(NL)} = \left(\frac{2V_{M(NL)}}{\pi}\right)$ = ____________ V

Full-Load readings:

Peak Output Voltage, V_M = _________V

Average value $V_{DC} = \frac{2V_M}{\pi} = V_{DC(FL)}$ = -------------------- V

$V_{RMS} = \frac{V_M}{\sqrt{2}}$

$V_{AC} = \sqrt{V_{RMS}^2 - V_{DC}^2}$

Ripple Factor $\gamma = V_{AC}/ V_{DC}$ =

$P_{DC} = V_{DC}^2 / R_L$ =

$P_{AC} = V_{RMS}^2 / R_L$ =

% $\eta = (P_{DC}/ P_{AC})*100$

% Regulation $= \frac{V_{DC\,(NL)} - V_{DC(FL)}}{V_{DC(FL)}} * 100 =$

The peak inverse voltage for each diode is PIV = $2V_{p(out)} + 0.7$ V =

Theoretical Calculations:

Full wave rectifier with Capacitor filter

$V_{(NL)}$ = ___________V

Full-Load readings:

Peak Output Voltage, V_M = _________V

Ripple Factor $\gamma = V_{AC}/ V_{DC}$

$V_{DC} = \frac{2V_M}{\pi} = V_{DC(FL)} =$

$R = R_L$

$V_{AC} = \frac{Vr(p-p)}{2\sqrt{3}}$

$V_{RMS} = \sqrt{V_{AC}^2 + V_{DC}^2}$

$P_{DC} = V_{DC}^2 / R_L =$

$P_{AC} = V_{RMS}^2 / R_L =$

$\% \eta = (P_{DC}/ P_{AC}) * 100$

$\% \text{ Regulation} = \frac{V_{DC(NL)} - V_{DC(FL)}}{V_{DC(FL)}} * 100 =$

Bridge Rectifier

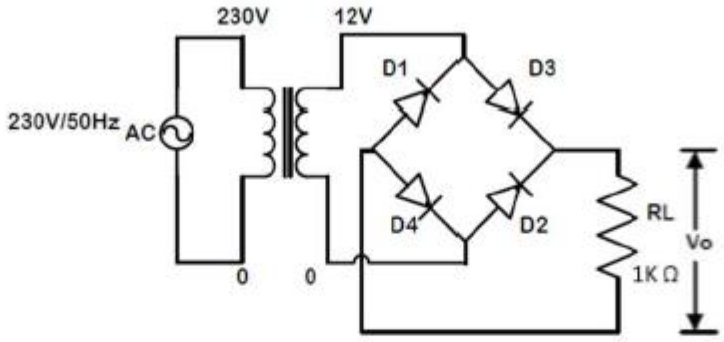


Fig. 1.5 Circuit of bridge rectifier without capacitor filter

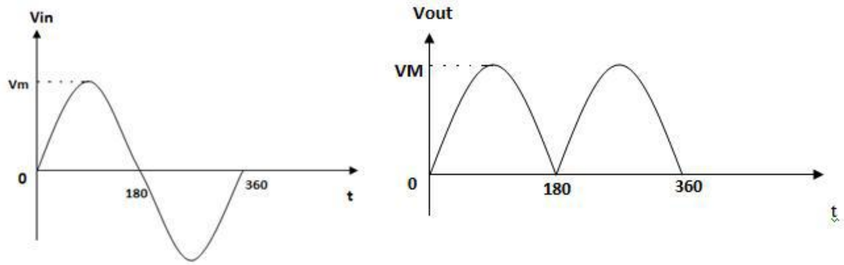


Fig. 1.6 Waveform for bridge rectifier with without filter

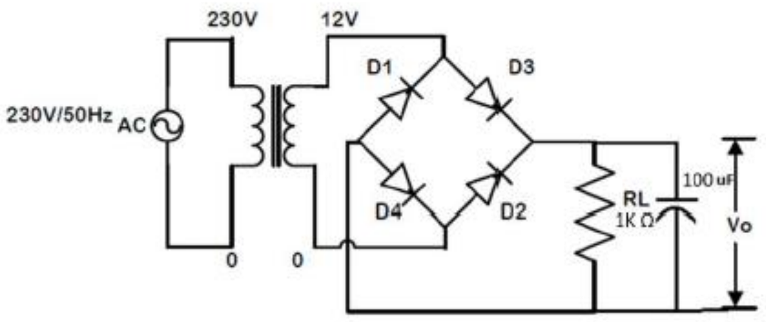
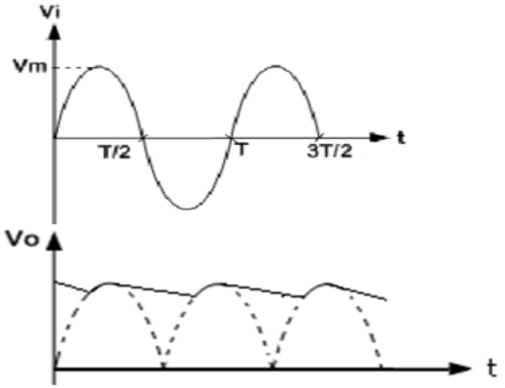


Fig. 1.7 Circuit of bridge rectifier with capacitor filter



- **Calculation and formula are same as full wave bridge rectifier**.

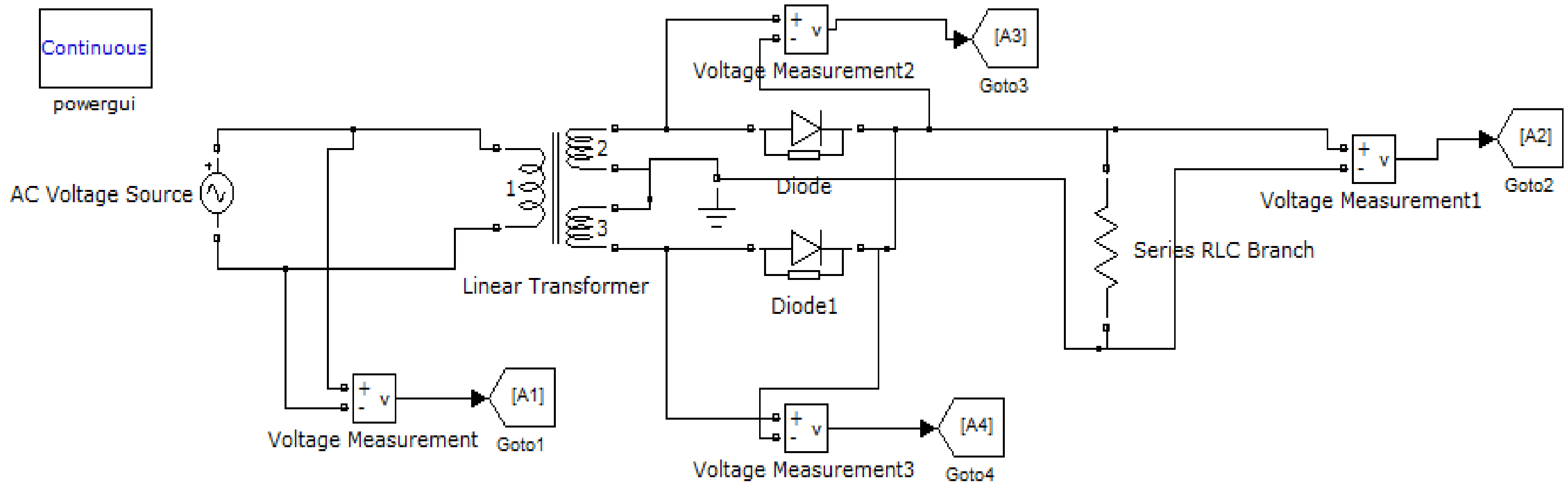
MATLAB CODE

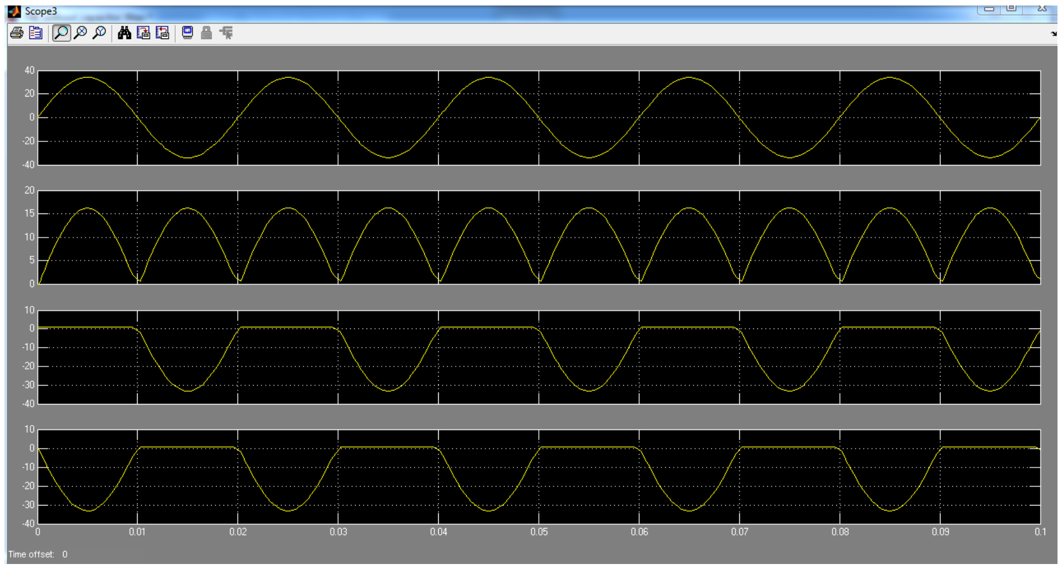
```
% Rectifier Circuit Design and Analysis

% Rectifier parameters
Vin = 230; % Input voltage (V)
f = 50; % Frequency (Hz)
RL = 100; % Load resistance (ohms)
Vdc = 0; % DC voltage (initialization)
ripple_factor = 0; % Ripple factor (initialization)
regulation = 0; % Regulation (initialization)
efficiency = 0; % Efficiency (initialization)

% Full wave center tapped transformer rectifier
Vout_center_tapped = (2/sqrt(2)) * (Vin/2); % Peak voltage
Vdc_center_tapped = Vout_center_tapped - 2*0.7; % Subtracting diode voltage drops
ripple_factor_center_tapped = (Vout_center_tapped / (2*f*RL)) * 100; % Ripple factor calculation
regulation_center_tapped = ((Vout_center_tapped - Vdc_center_tapped) / Vdc_center_tapped) * 100; % Regulation calculation
efficiency_center_tapped = (Vdc_center_tapped / Vin) * 100; % Efficiency calculation

% Full wave bridge rectifier
Vout_bridge = (2/sqrt(2)) * Vin; % Peak voltage
Vdc_bridge = Vout_bridge - 2*0.7; % Subtracting diode voltage drops
ripple_factor_bridge = (Vout_bridge / (2*f*RL)) * 100; % Ripple factor calculation
regulation_bridge = ((Vout_bridge - Vdc_bridge) / Vdc_bridge) * 100; % Regulation calculation
efficiency_bridge = (Vdc_bridge / Vin) * 100; % Efficiency calculation

% Rectifier with Capacitor Filter
C = 100e-6; % Capacitance (F)
Vdc_capacitor = Vdc_bridge; % DC voltage with capacitor filter
ripple_factor_capacitor = (Vdc_capacitor / (2*f*RL*C)) * 100; % Ripple factor calculation
regulation_capacitor = ((Vout_bridge - Vdc_capacitor) / Vdc_capacitor) * 100; % Regulation calculation
```

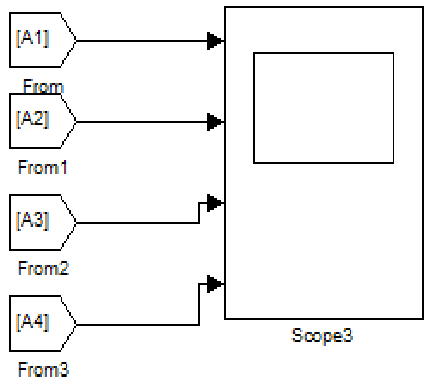
```
efficiency_capacitor = (Vdc_capacitor / Vin) * 100; % Efficiency calculation

% Displaying results
disp('Full Wave Center Tapped Transformer Rectifier:')
disp(['DC Voltage: ', num2str(Vdc_center_tapped), ' V'])
disp(['Ripple Factor: ', num2str(ripple_factor_center_tapped), '%'])
disp(['Regulation: ', num2str(regulation_center_tapped), '%'])
disp(['Efficiency: ', num2str(efficiency_center_tapped), '%'])

disp('Full Wave Bridge Rectifier:')
disp(['DC Voltage: ', num2str(Vdc_bridge), ' V'])
disp(['Ripple Factor: ', num2str(ripple_factor_bridge), '%'])
disp(['Regulation: ', num2str(regulation_bridge), '%'])
disp(['Efficiency: ', num2str(efficiency_bridge), '%'])

disp('Rectifier with Capacitor Filter:')
disp(['DC Voltage: ', num2str(Vdc_capacitor), ' V'])
disp(['Ripple Factor: ', num2str(ripple_factor_capacitor), '%'])
disp(['Regulation: ', num2str(regulation_capacitor), '%'])
disp(['Efficiency: ', num2str(efficiency_capacitor), '%'])
```

Open MATLAB and then open Simulink using the ‘Simulink’ icon on MATLAB, under Simulink library browser click on ‘File’ for New Simulink model. Under Simulink library browser click on ‘simPowersystems’, Select required component, right click on the component to add(Place) it to editor and build/complete the circuit and Start simulation.

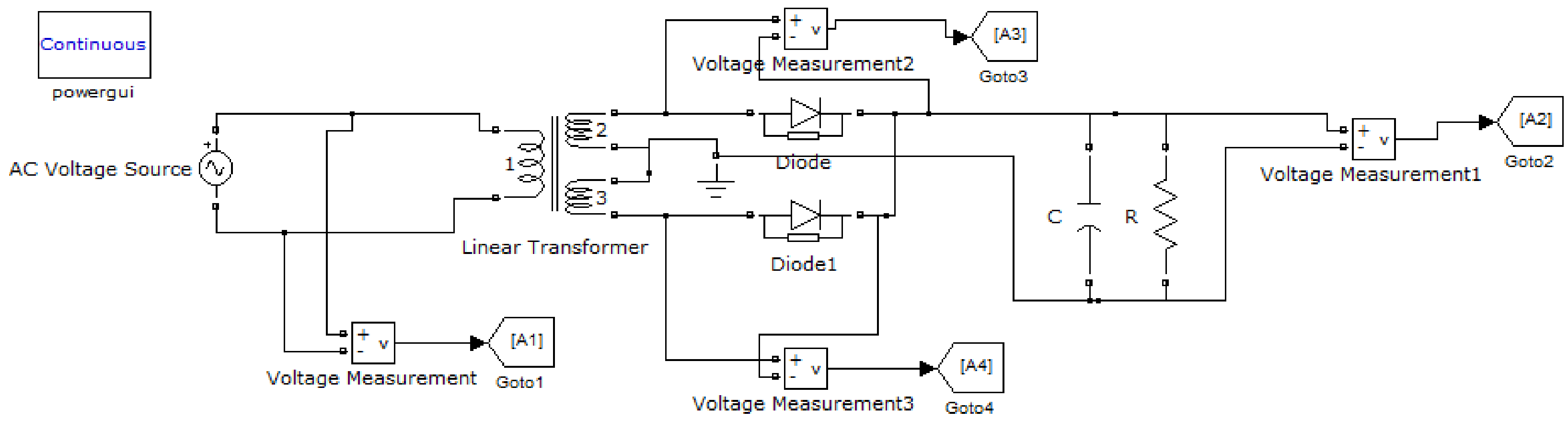
MATLAB_Simulink Full wave centre tapped transformer without capacitor filter

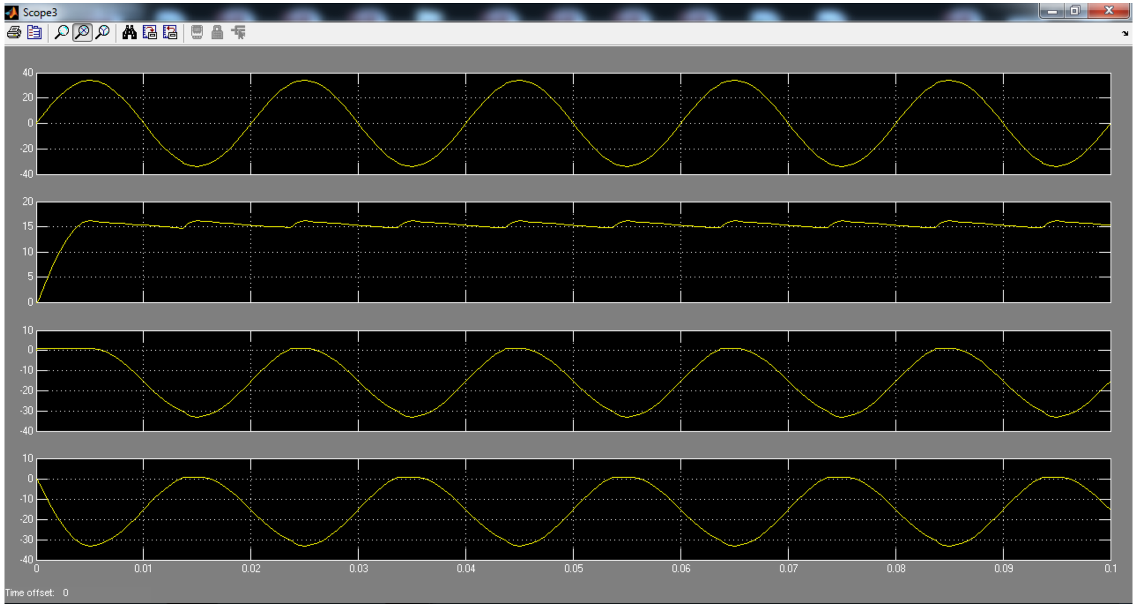


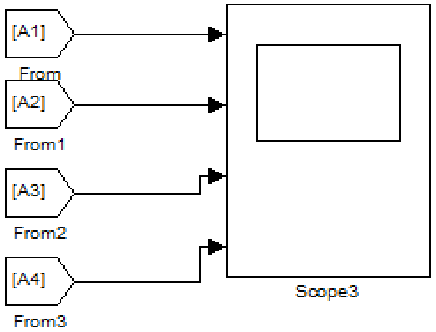




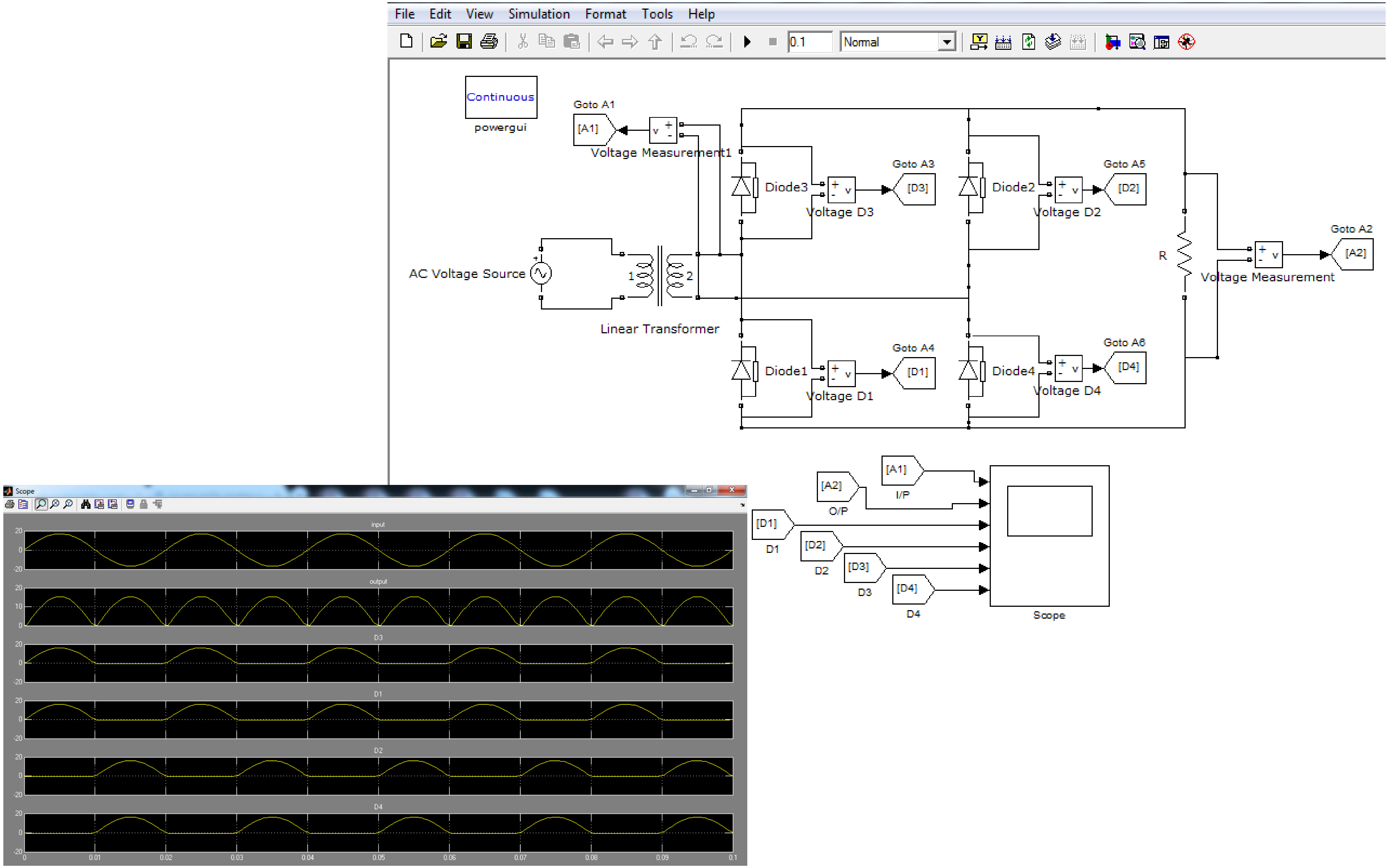
MATLAB_Simulink Full wave centre tapped transformer with capacitor filter



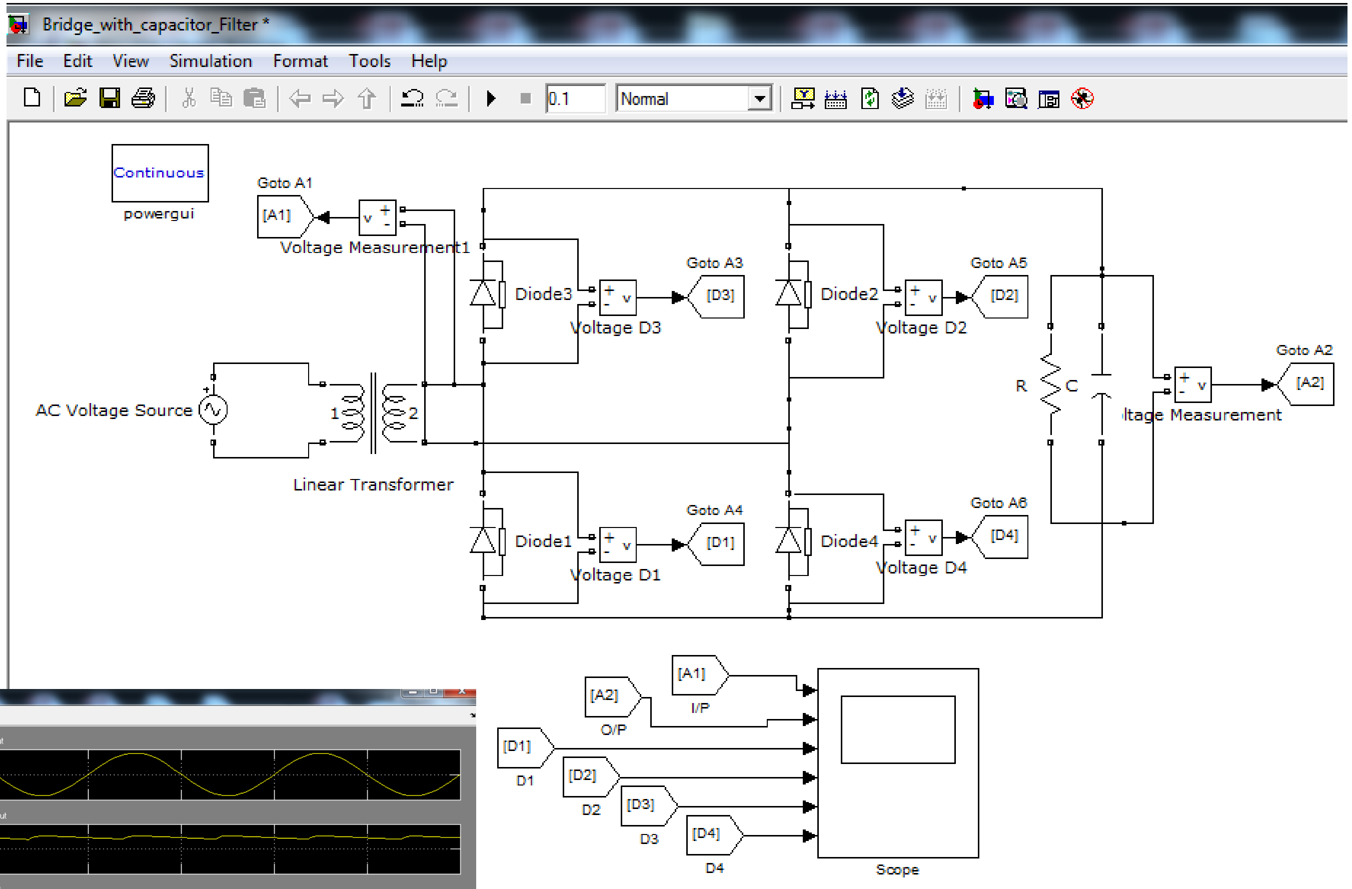


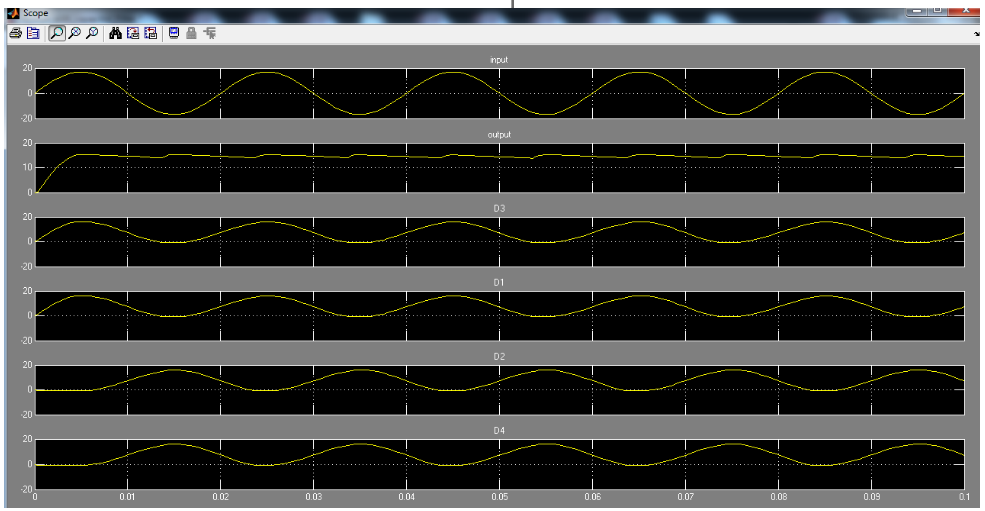


MATLAB_Simulink Full Wave Bridge type rectifier circuits without Capacitor filter



MATLAB_Simulink Full Wave Bridge type rectifier circuits with Capacitor filter





Result:

Table 1.1 Comparison of Rectifier

Rectifier Type	Without Filter			Without Filter		
	Ripple factor	Efficiency	Regulation	Ripple factor	Efficiency	Regulation
FWR						
BR						
FWR Simulation						
BR Simulation						

Preparation(4)	Conduction(4)	Result/Conclusion(5)	Total(13)

Signature with date

Conclusions:

Vive Voce

1. What is the function of a bridge rectifier?
2. Why do we need ripple factor?
3. Why capacitor is used in bridge rectifier?