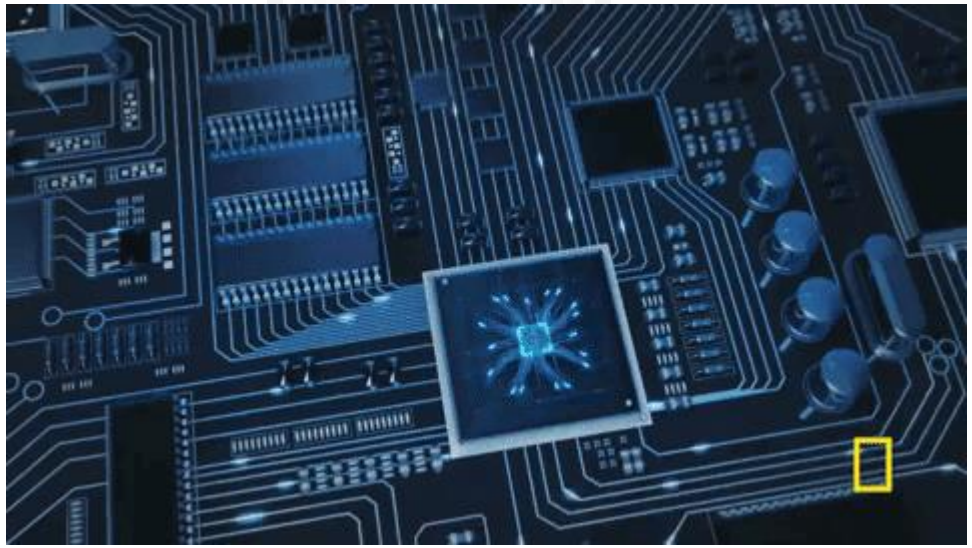
ATME College of Engineering

Department of EEE
Emitting Elite Energy

BEE613B
Embedded Systems Design
Module-3: Hardware Software Co design and Program Modelling



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Contents

Learning Objectives

1.Understand Hardware-Software Co-Design: Analyze key issues and architectural trade-offs.

2.Explore Computational Models: Familiarize with models such as FSM, DFG, and CDFG.

3.Understand Embedded Hardware Design: Study the role of analog and digital components.

4.Learn VLSI Design Concepts: Understand IC types, design steps, and methodologies.

5.Introduction to EDA Tools: Study modern tools like OrCAD, Eagle, and Prote

3.1 Hardware Software Co-Design and Program Modelling

Fundamental Issues in Hardware-Software Co-Design:

1.Selecting the Model:

1. Specification Stage: Focus on functionality.
2. Implementation Stage: Focus on system structure.

2.Selecting the Architecture:

1. **Controller Architecture:** Finite State Machine (FSM).
2. **Datapath Architecture:** Data Flow Graph (DFG).
3. **FSMD:** Combination of controller + datapath.
4. **Other Architectures:** CISC, RISC, VLIW, SIMD, MIMD.

3. Selecting the Language:

- **Software Languages:** C, C++, Java.
- **Hardware Languages:** VHDL, Verilog.

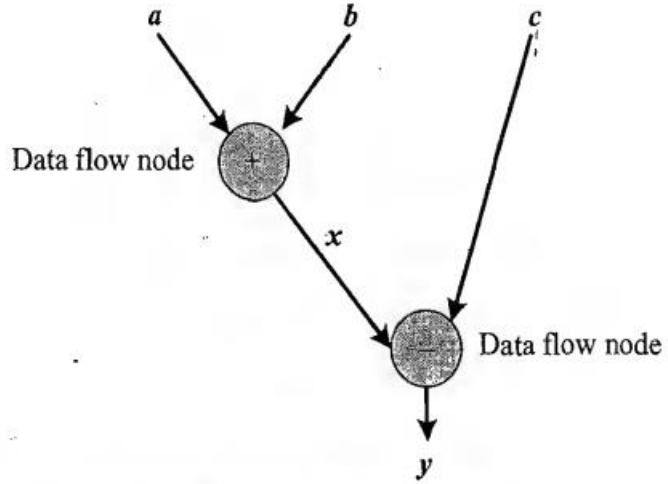
4. Partitioning System Requirements:

- Hardware vs Software trade-offs.

3.2 Computational Models in Embedded System Design

1.Data Flow Graph (DFG) Model:

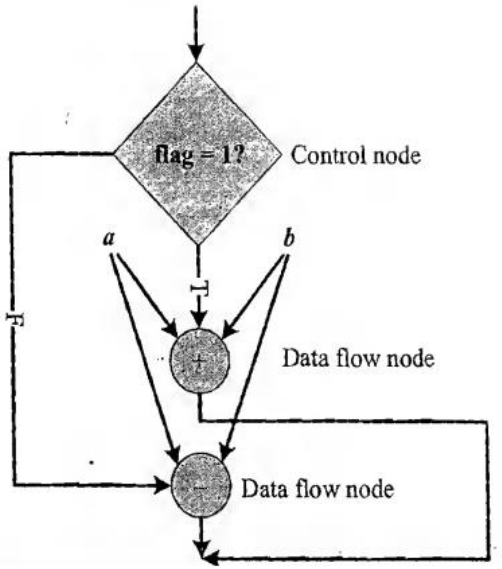
1. Data-driven model where operations transform input to output.
2. **Applications:** DSP and computational tasks.
3. **Example:** Acyclic DFG for mathematical operations.



2. Control Data Flow Graph (CDFG) Model

1. Extends **DFG model** by incorporating **control operations (conditionals)**.
2. Uses **decision nodes (diamonds)** to represent conditional execution.
3. Example: **Image processing in a digital camera**, where the user selects **JPEG, TIFF, BMP** format.

If flag = 1, $x = a + b$; else $y = a - b$;



3. State Machine Model (FSM):

1. Represents reactive systems through states, events, and actions.
2. **Example:** Seat Belt Warning System.

4. Sequential Program Model:

1. Executes tasks in a defined sequence.
2. Tools: FSMs, Flow Charts.

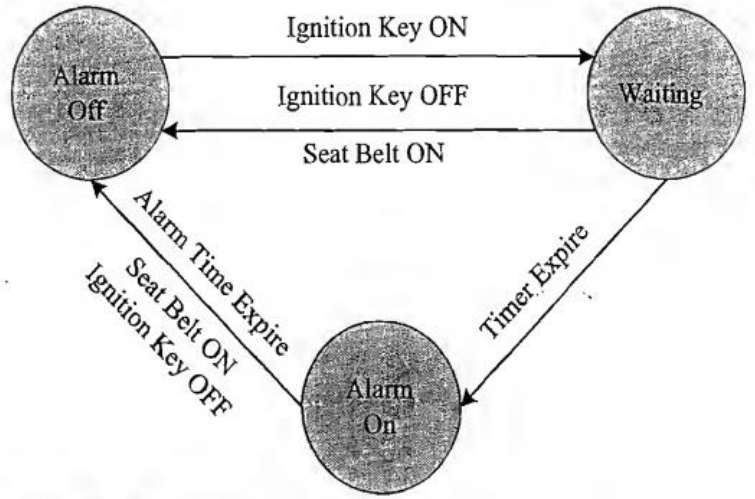


Fig. 7.3 FSM Model for Automatic seat belt warning system

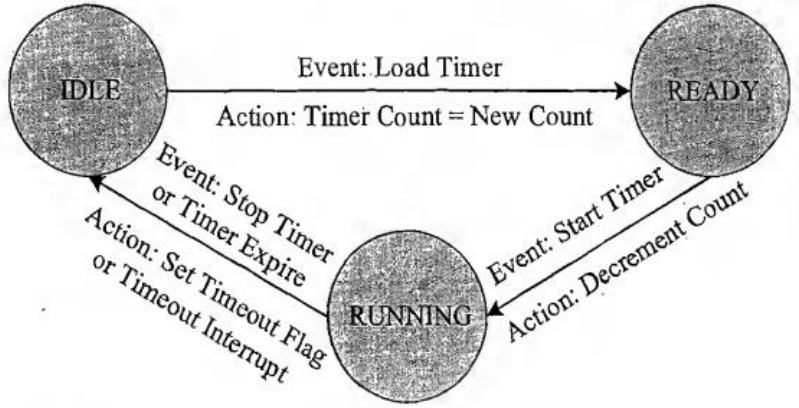


Fig. 7.4 FSM Model for timer

Example-1

Question

Design an Automatic Tea/Coffee Vending Machine using FSM Model

A **tea/coffee vending machine** operates based on a **Finite State Machine (FSM) model** with the following requirements:

1. The machine starts in **'Wait for Coin'** state.
2. The user **inserts a ₹5 coin** to initiate the vending process.
3. After inserting the coin, the system transitions to **'Wait for User Input'** state.
4. The user can select:
   - **'Tea'** → Transitions to **'Dispense Tea'** state.
   - **'Coffee'** → Transitions to **'Dispense Coffee'** state.

- **Cancel’** → Coin is returned, and state transitions back to **‘Wait for Coin’**.

1. Once the drink is dispensed, the system resets back to **‘Wait for Coin’**.
2. Additional conditions may include:
   - **Timeout in ‘Wait for User Input’ state** (if no input, coin is returned).
   - **Error Handling** for **‘Water Not Available’** or **‘Mix Not Available’**.

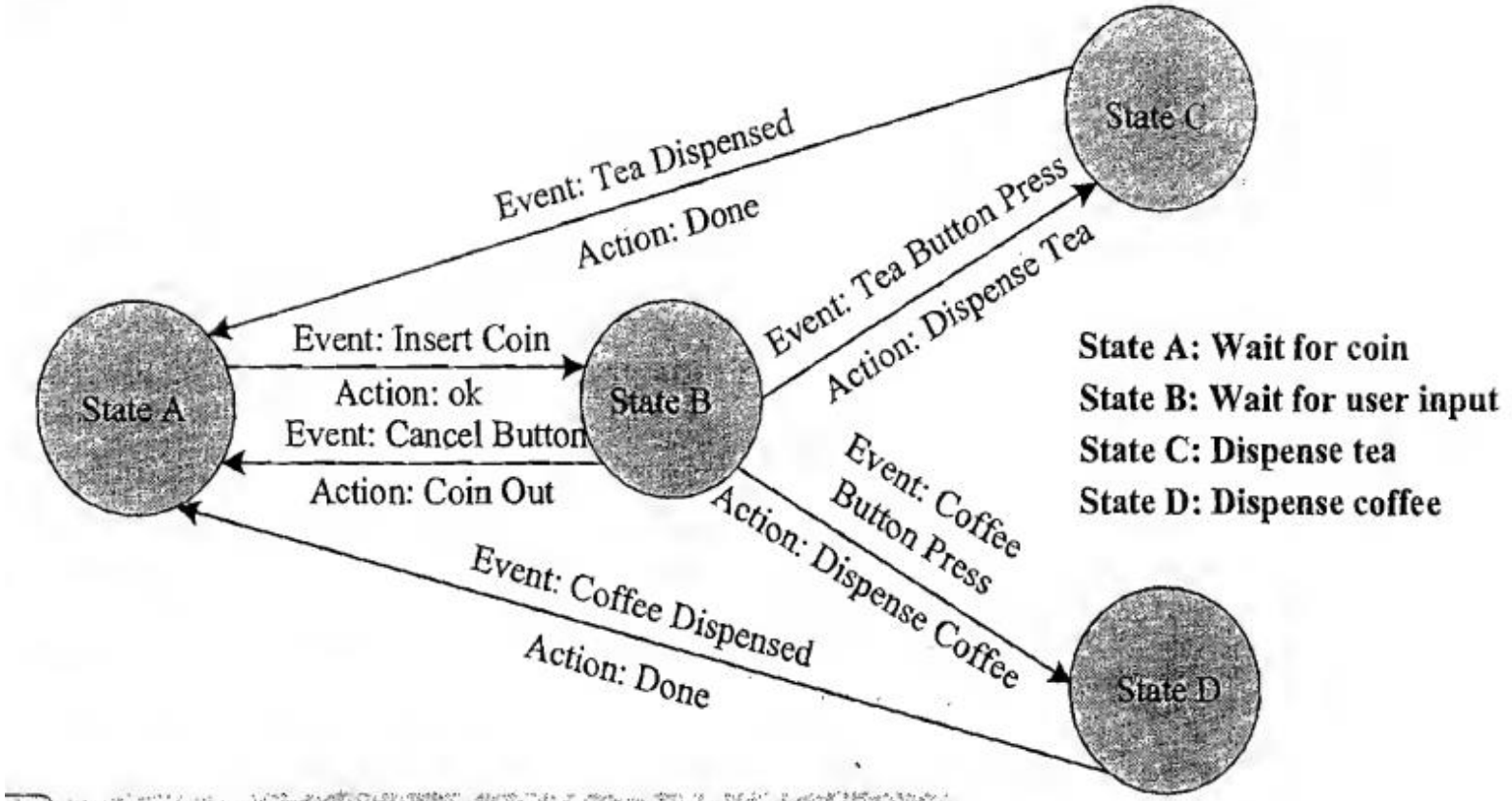
Solution – FSM Representation

States of the FSM Model:

1. **Wait for Coin** → Initial state, waiting for a ₹5 coin.
2. **Wait for User Input** → Waiting for selection of **Tea, Coffee, or Cancel**.
3. **Dispense Tea** → Vends tea, then returns to **Wait for Coin**.
4. **Dispense Coffee** → Vends coffee, then returns to **Wait for Coin**.
5. **Error State (Optional)** → Handles **no water/mix availability** issues.

FSM State Transitions:

Current State	Event (Input)	Next State	Action
Wait for Coin	Insert ₹5 coin	Wait for User Input	Accept Coin
Wait for User Input	Press ‘Tea’	Dispense Tea	Start Tea Dispensing
Wait for User Input	Press ‘Coffee’	Dispense Coffee	Start Coffee Dispensing
Wait for User Input	Press ‘Cancel’	Wait for Coin	Return Coin
Dispense Tea	Tea Dispensed	Wait for Coin	Reset System
Dispense Coffee	Coffee Dispensed	Wait for Coin	Reset System
Wait for User Input	Timeout (No Selection)	Wait for Coin	Return Coin
Any State	Error (No Water/Mix)	Error State	Display Error
Error State	Problem Resolved	Wait for Coin	Reset System



7.5 **FSM Model for Automatic Tea\Coffee Vending Machine**

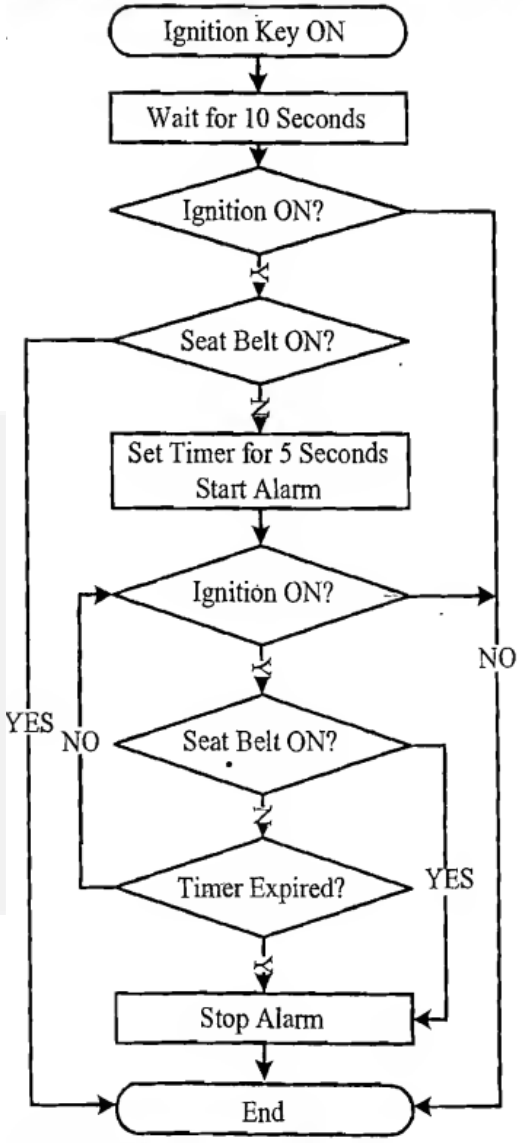


Fig. 7.7 **Sequential Program Model for seat belt warning system**

3.3 Embedded Hardware Design and Development: Analog Components

1.Resistors: Current limiting.
2.Capacitors: Filtering, decoupling, RF matching.
3.Inductors: Ripple and noise filtering.
4.Diodes: Voltage clamping, rectification.
5.Transistors: Switching and amplification.

3.4 Embedded Hardware Design and Development: Digital Components

1.Logic Gates: AND, OR, XOR, etc.

2.Buffers: Amplifies current or power.

3.Latches: Data storage.

4.Decoders/Encoders: Address decoding and encoding.

5.Multiplexers/Demultiplexers: Signal selection and distribution.

3.5 VLSI & Integrated Circuit Design

1.IC Types: SSI, MSI, LSI, VLSI.

2.Design Steps:

1. Specification, Design Entry, Simulation, Logic Synthesis.
2. Physical Layout, Timing Simulation.

3.VHDL: Describes behavior and structure of digital circuits.

3.6 Electronic Design Automation Tools

1.Capabilities: PCB design, routing, layout automation.

2.Popular Tools: OrCAD, Eagle, Protel.

3.Applications: Accurate and faster PCB and hardware design.

Thank You