Digital Logic Circuits– EE306A

Module-3

Prepared By,

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Course Outline

Course Code	Course Title	Core/Elective	Prerequisite	Contact Hours			Total Hrs/ Sessions
				L	T	P	
EE306A	Digital Logic Circuits	Elective	Basic Electronics	3	-	-	40

Module – 1: Principles of Combinational Logic: Definition of combinational logic, canonical forms, Generation of switching equations from truth tables, Karnaugh maps-3,4,5 variables, Incompletely specified functions (Don‘t care terms) Simplifying Max term equations, Quine-McCluskey minimization technique, Quine-McCluskey using don‘t care terms, Reduced prime implicants Tables.	
Bloom’s Taxonomy Level	L1 – Remembering, L2 – Understanding, L3 – Applying, L4 – Analyzing,
Module – 2: Analysis and Design of Combinational logic: General approach to combinational logic design, Decoders, BCD decoders, Encoders, digital multiplexers, Using multiplexers as Boolean function generators, Adders and subtractors, Cascading full adders, Look ahead carry, Binary comparators	
Bloom’s Taxonomy Level	L1 – Remembering, L2 – Understanding, L3 – Applying, L4 – Analysing,
Module – 3: Flip-Flops: Basic Bistable elements, Latches, Timing considerations, The master-slave flip-flops (pulsetriggered flip-flops): SR flip-flops, JK flip-flops, Edge triggered flip- flops, Characteristic equations .	
Bloom’s Taxonomy Level	L1 – Remembering, L2 – Understanding
Module – 4: Flip-Flops Applications: Registers, binary ripple counters, synchronous binary counters, Counters based on shift registers, Design of a synchronous counter, Design of a synchronous mod-n counter using clocked T, JK, D and SR flip-flops.	
Bloom’s Taxonomy Level	L1 – Remembering, L2 – Understanding, L3 – Applying, L – 4 Analysing,
Module – 5: Sequential Circuit Design: Mealy and Moore models, State machine notation, Synchronous Sequential circuit analysis, Construction of state diagrams, counter design. Memories: Read only and Read/Write Memories, Programmable ROM, EPROM, Flash memory.	

Course Outcomes

1. Develop simplified switching equation using Karnaugh Maps and Quine McClusky techniques.[L3]
2. Apply the design procedures for Multiplexer, Encoder, Decoder, Adder, Subtractors and Comparator as digital combinational control circuits.[L3]
3. Illustrate the design of flip flops and development of its characteristic equation.[L2]
4. Apply the design procedures for counters and shift registers as sequential control circuits.[L3]
5. Develop Mealy/Moore Models and state diagrams for the given clocked sequential circuits and Interpret the functioning of Read only and Read/Write Memories, Programmable ROM, EPROM and Flash memory.[L3]

List of Reference Books

1. Digital Logic Applications and Design, John M Yarbrough, Thomson Learning 2001 ISBN 981- 240-062-1.
2. Digital Principles and Design Donald D. Givone McGraw Hill 2002 ISBN 978-0- 07-052906-9.

Module – 3: Introduction

1. Sequential Circuit:

Combinational circuit produces an output based on input variable only, but Sequential circuit produces an output based on current input and previous input variables.

→sequential circuits include memory elements which are capable of storing binary information.

→That binary information defines the state of the sequential circuit at that time.

Sequential Circuits

Combinational Circuit:

Figure: Combinational Circuits

Sequential Circuit:

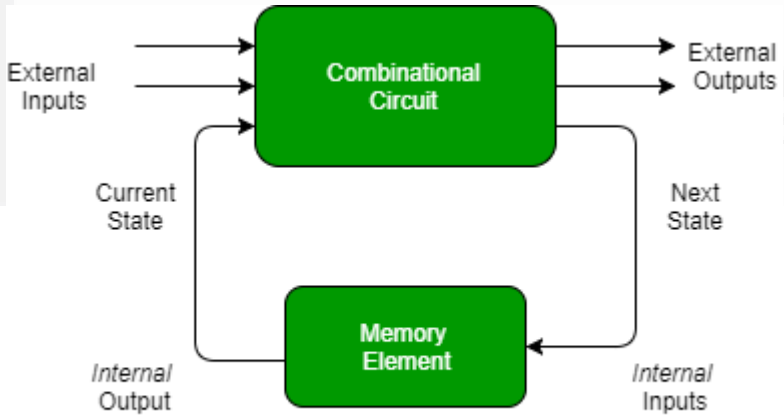


Figure: Sequential Circuit

Sequential Circuits

1. Sequential Circuit:

- External inputs which is not controlled by the circuit.
- Internal inputs which are a function of a previous output states.

**Sequential circuits are used to design Counters, Registers, RAM and other state retaining machines.

Types of Sequential Circuits

1. Asynchronous sequential circuit
2. Synchronous sequential circuit

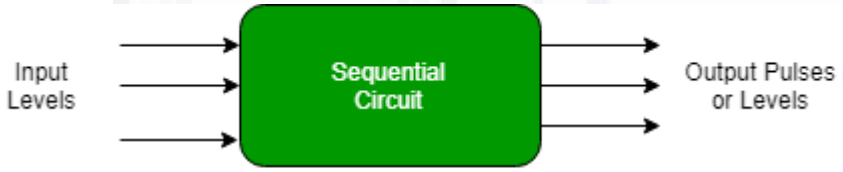


Figure: Asynchronous Sequential Circuit

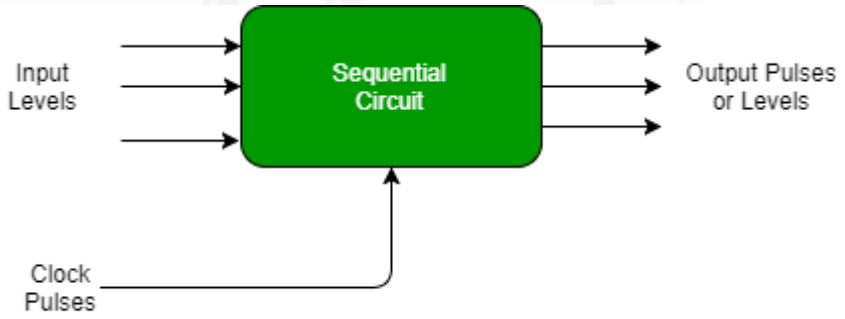


Figure: Synchronous Sequential Circuit

Types of Sequential Circuits

1. Asynchronous sequential circuit

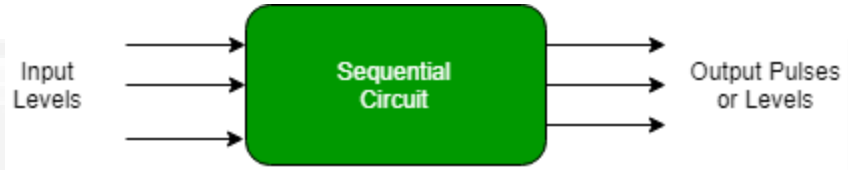


Figure: Asynchronous Sequential Circuit

2. These circuit do not use a clock signal
3. These circuits are faster Since there is no clock pulse, changes their state immediately when there is a change in the input signal.

** Asynchronous sequential circuits are used when speed of operation is important and independent of internal clock pulse.

Synchronous sequential circuit

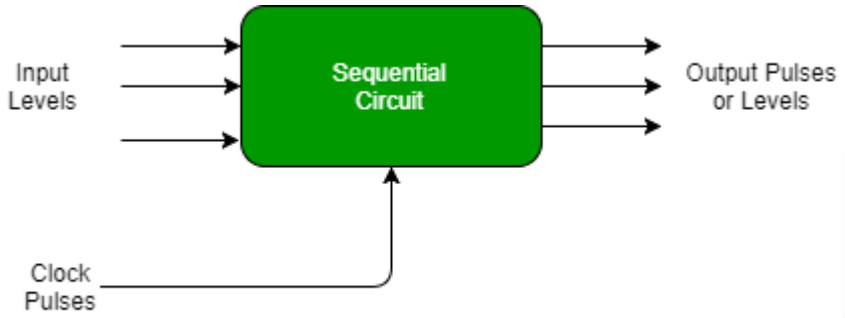


Figure: Synchronous Sequential Circuit

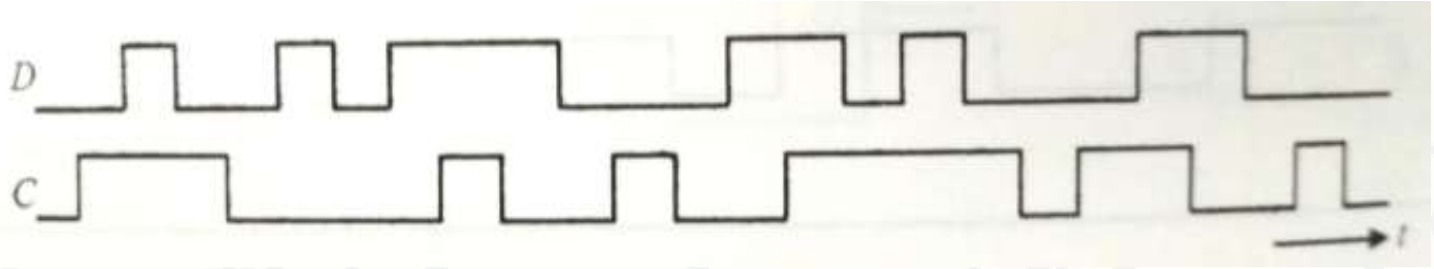
1. These circuit uses clock signal (pulsed) and level inputs
2. Output pulse has same duration as that of clock pulse
3. Circuits are bit slower compared to Asynchronous.
4. Level output changes state at the start of an input pulse and remains in that state until the next input or clock pulse arrives

** Synchronous sequential circuit are used in synchronous counters, flip flops, and in the design of MEALY-MOORE state management machines.

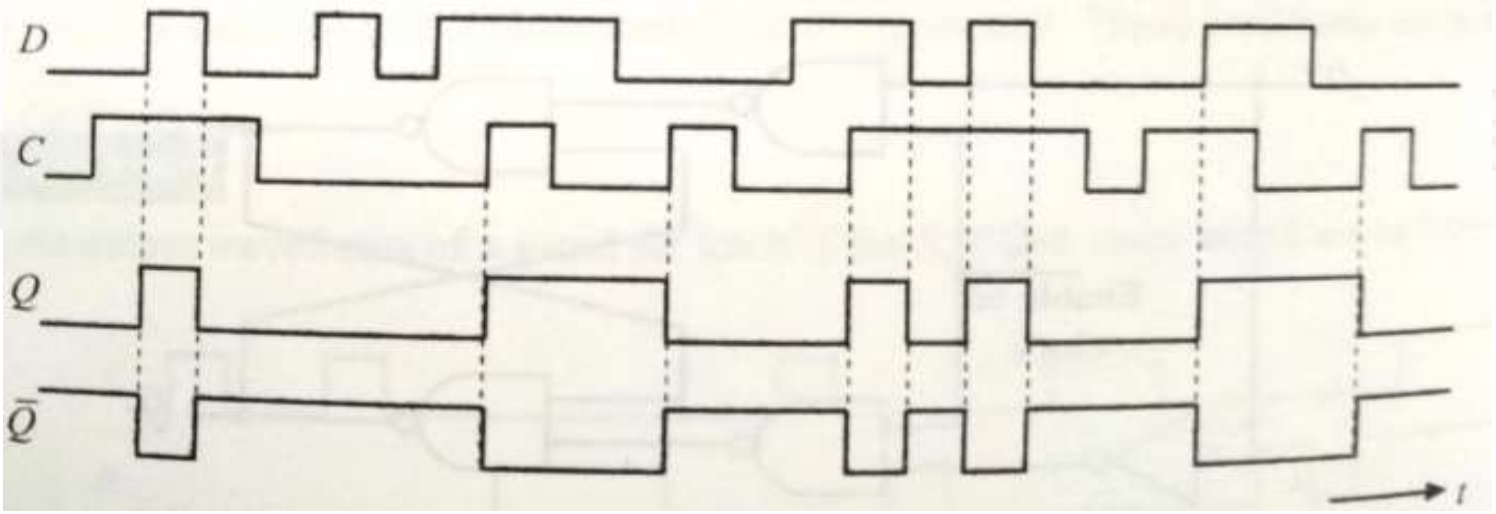
S.NO.	COMBINATIONAL CIRCUITS	SEQUENTIAL CIRCUITS
(1)	The output depends only upon the present input and there is no need for feedback for input and output, so memory element is not required.	The output depends upon both present input and present state (previous output), so memory element is required to save the feedback state.
(2)	It is easier to design, use and handle.	It is not easier to design, use and handle than combinational circuits.
(3)	Clock signals are not required and it is not dependent on time.	Clock signals are required and it is dependent on time and clock so need triggering.
(4)	Elementary building blocks are only logic gates.	Elementary building blocks are Flip-Flops.
(5)	These are faster logic circuits.	These circuits are slower than combinational circuits.

Numericals

Sketch the Output of the Gated D Latch



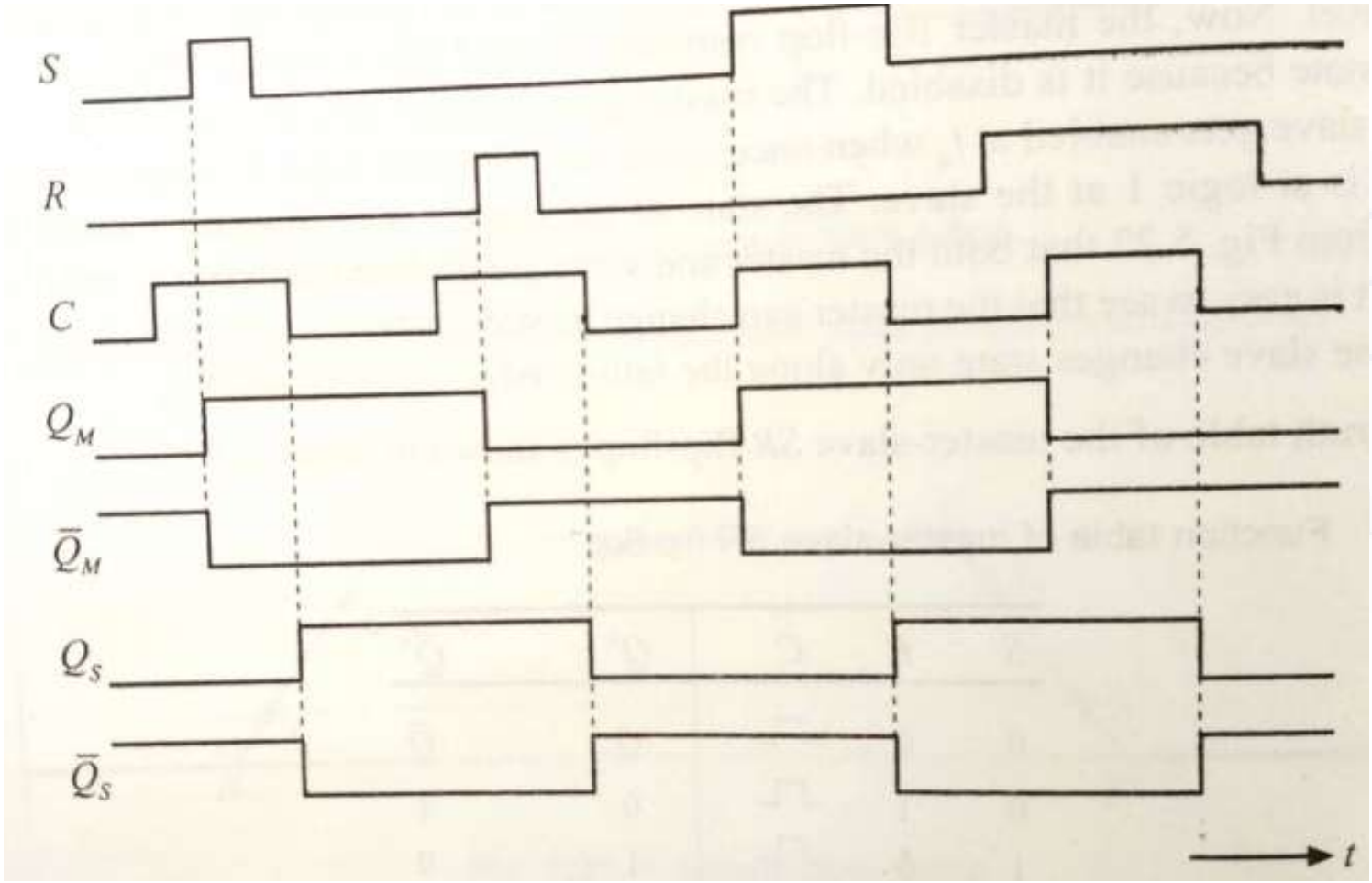
Solution:



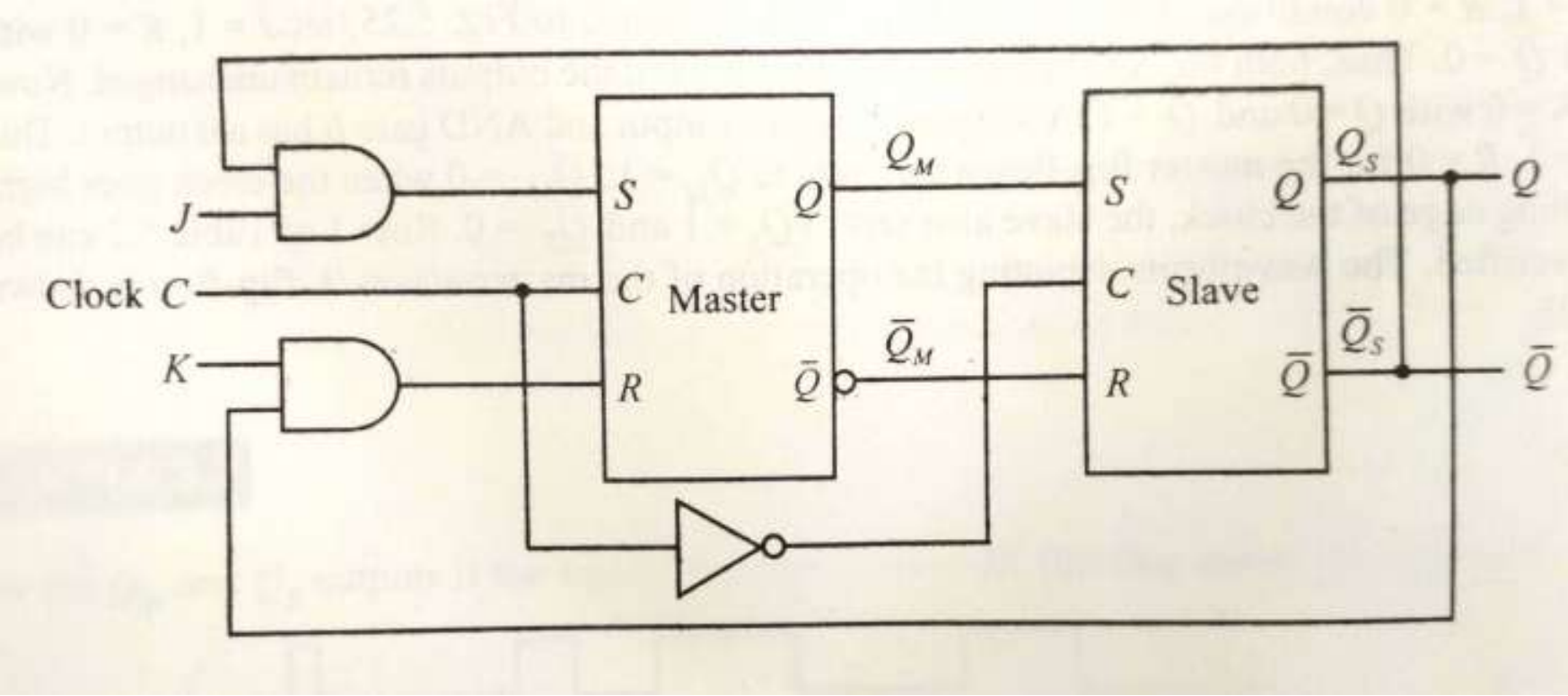
Pulse Triggered Flip Flop

- Master Slave S-R Flip Flop
- Master Slave J-K Flip Flop

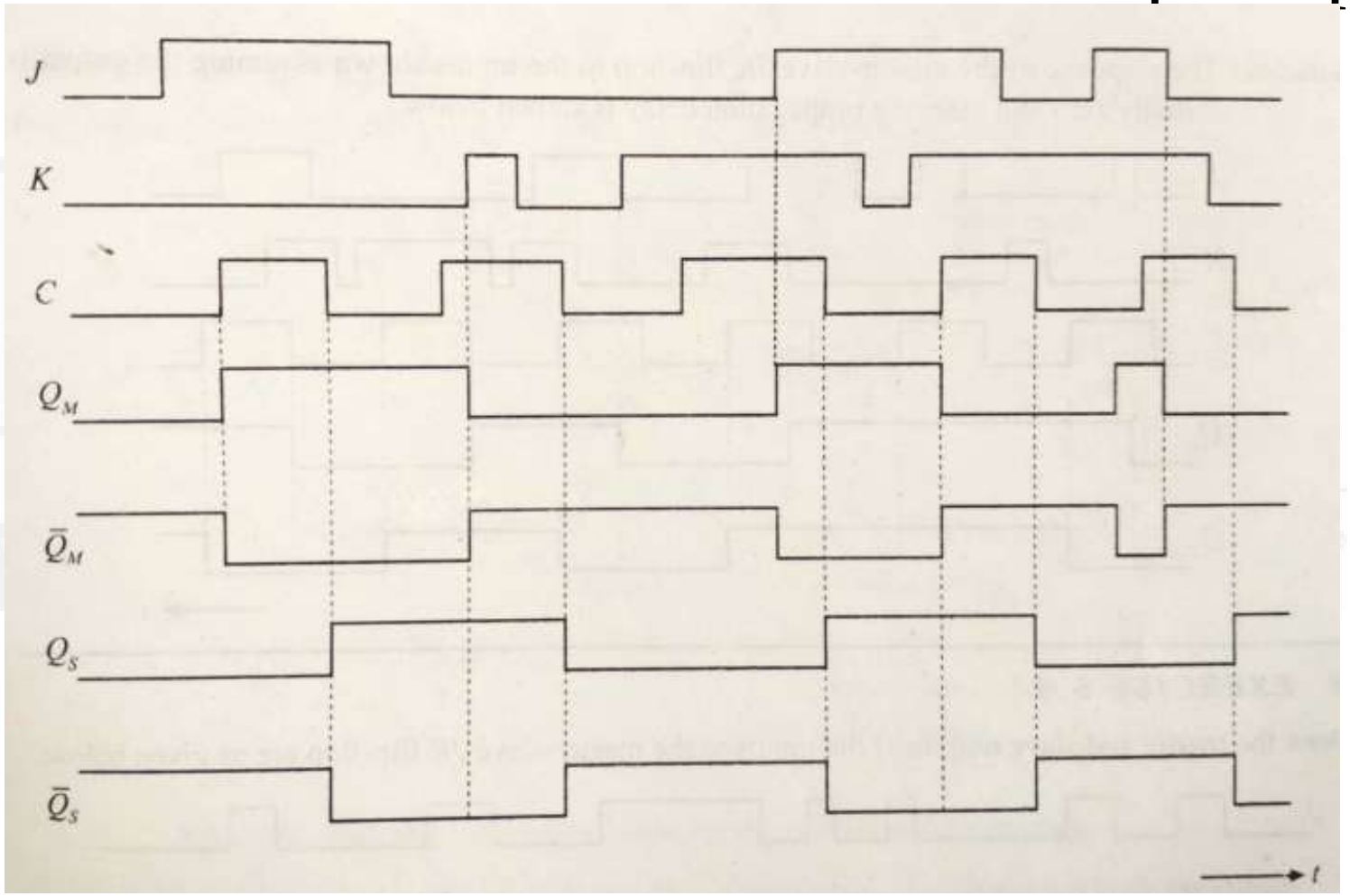
Waveforms of Master Slave SR Flip Flop



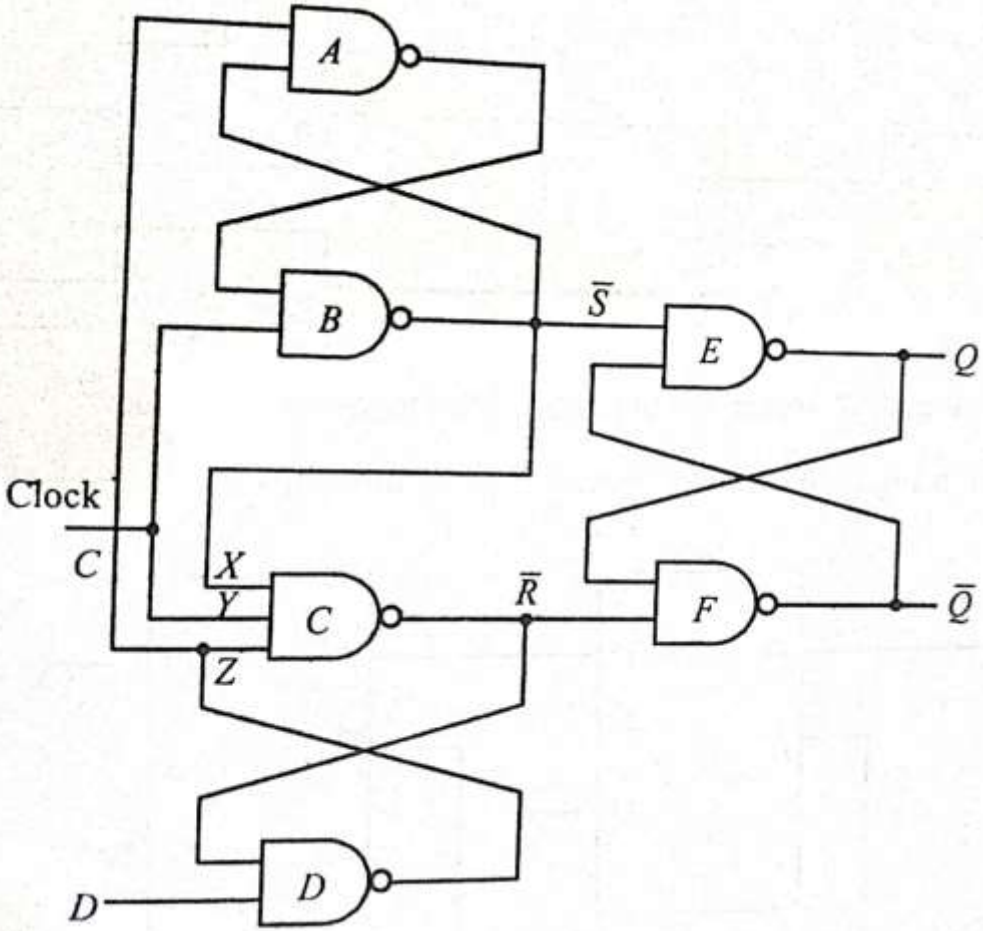
Master Slave J-K Flip Flop



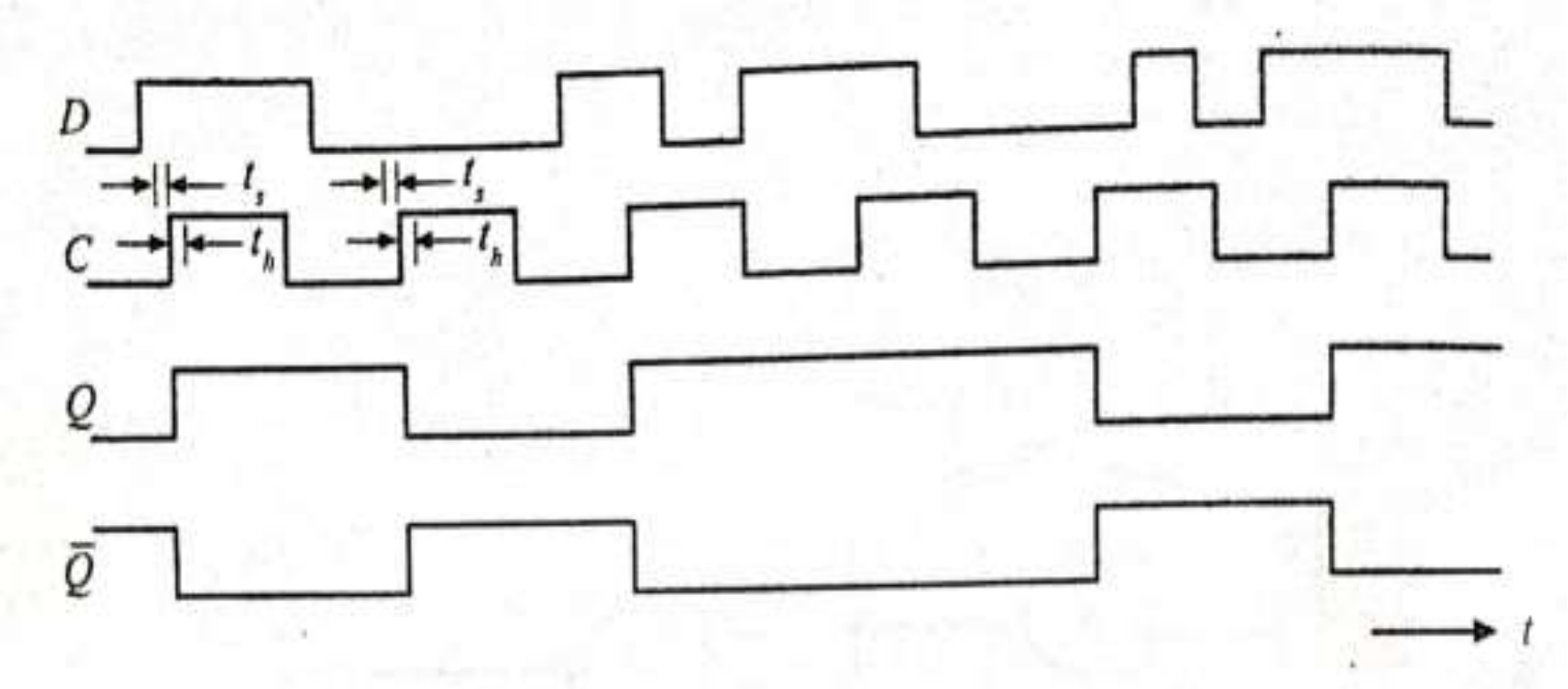
Waveforms of Master Slave J-K Flip Flop



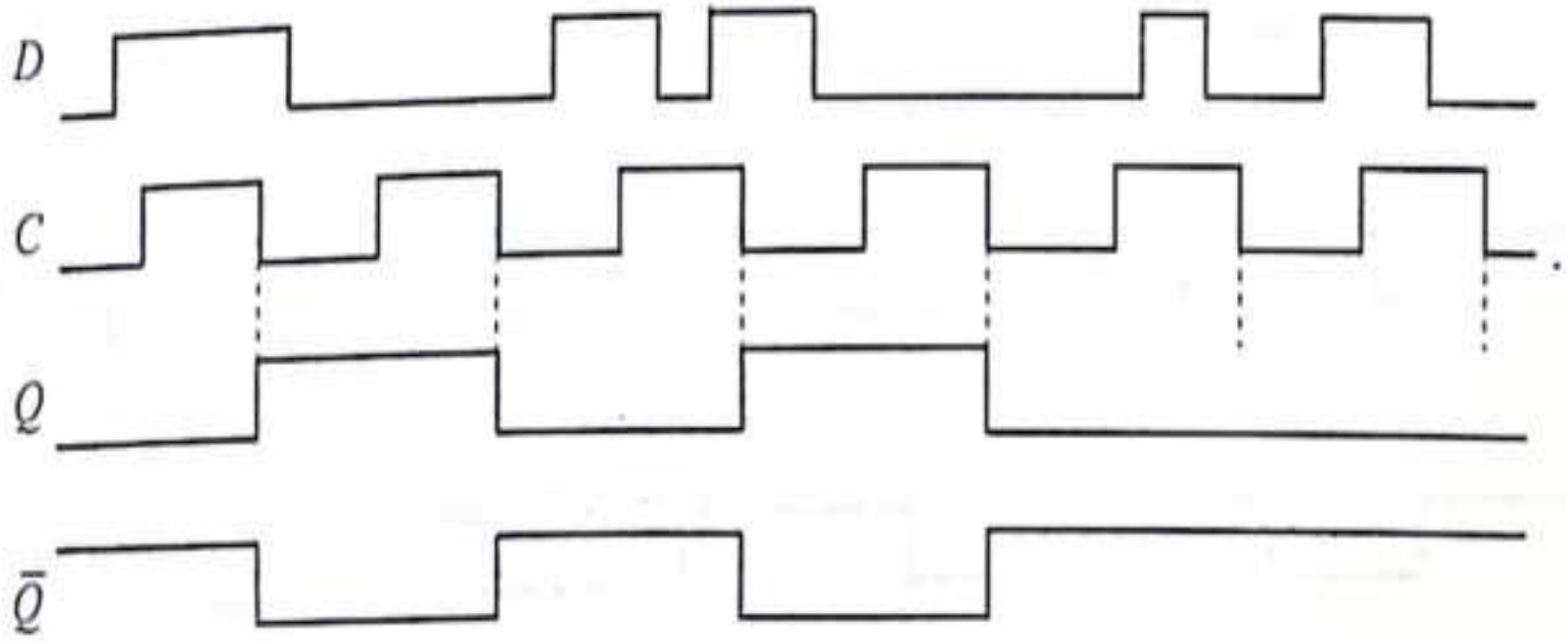
Positive Edge Triggered D Flip Flop



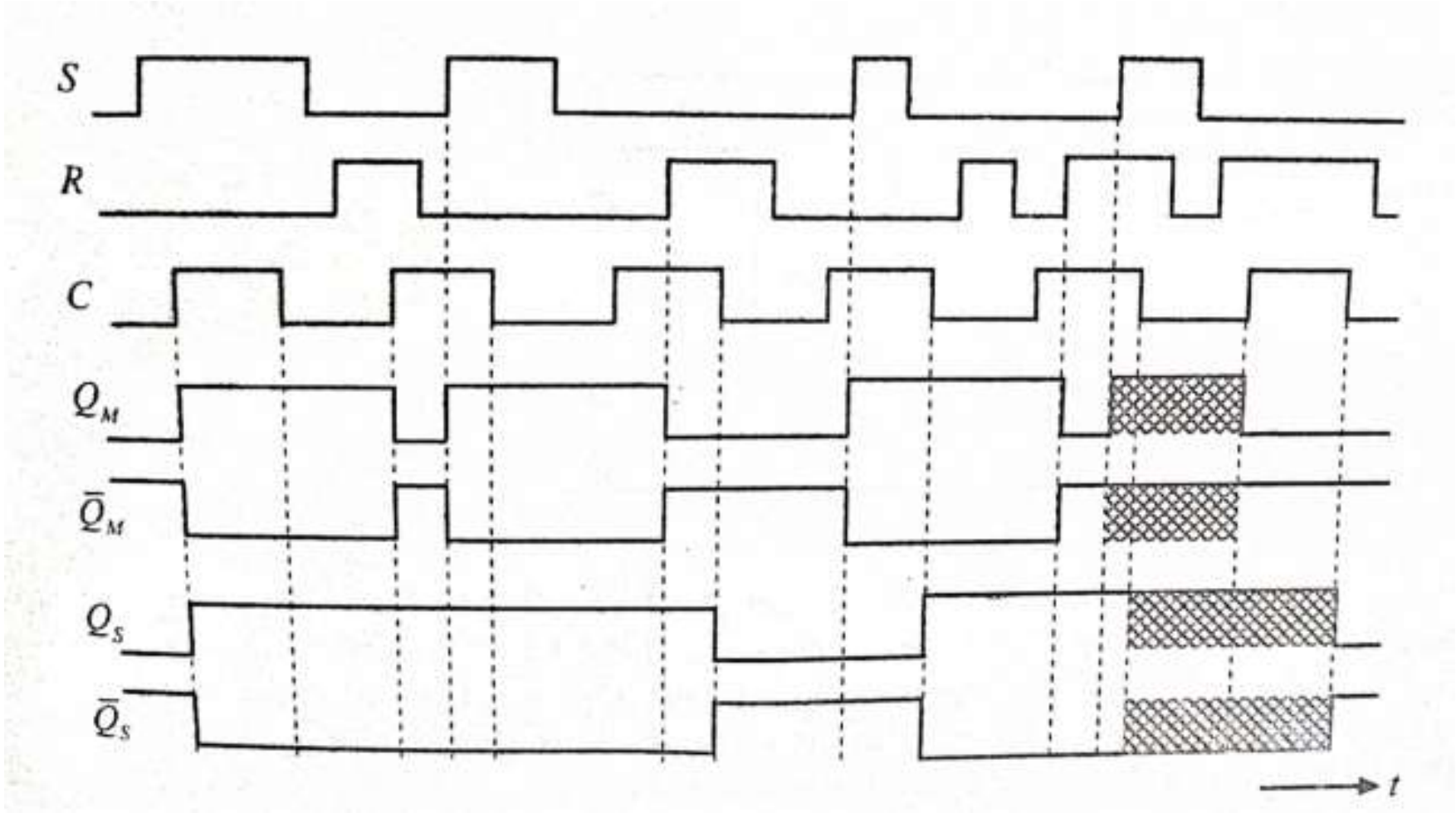
Response of Positive Edge Triggered D Flip Flop



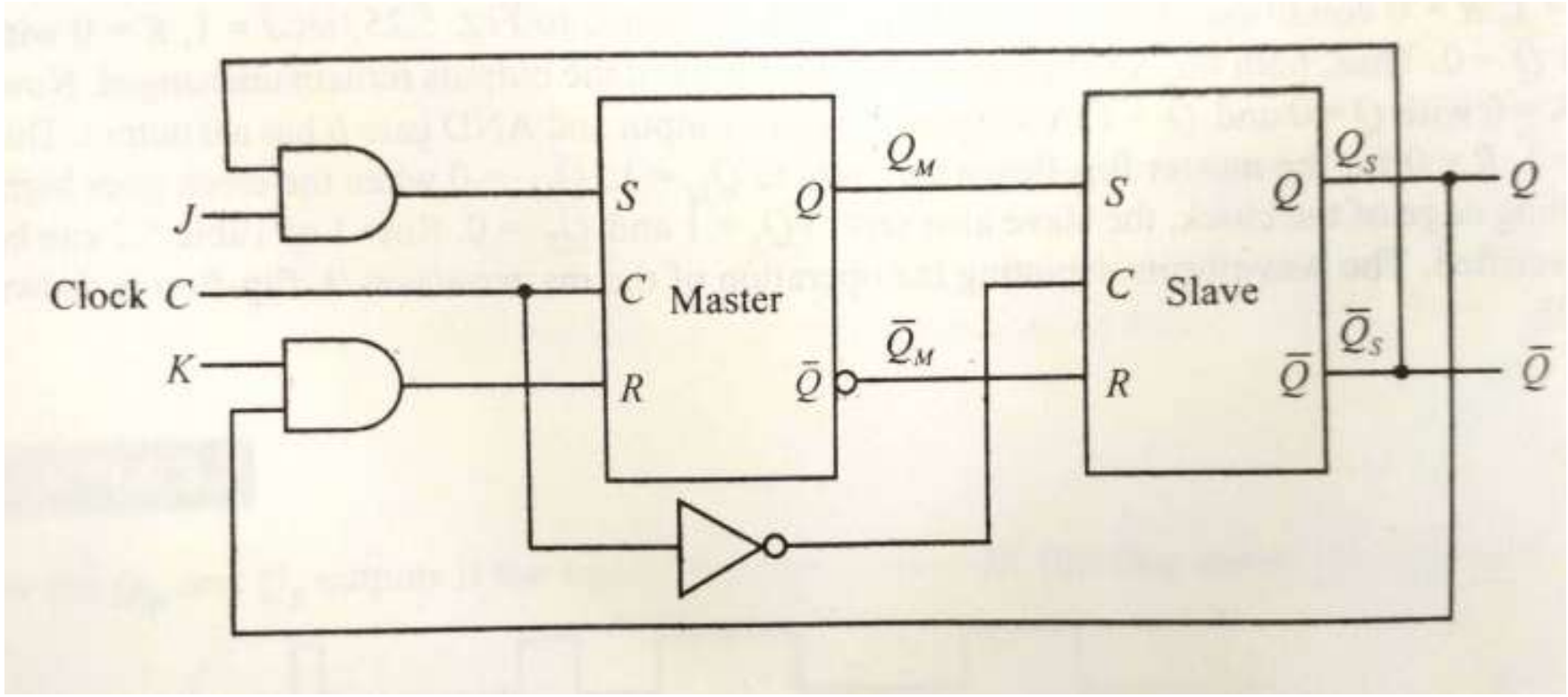
Response of Negative Edge Triggered D Flip Flop



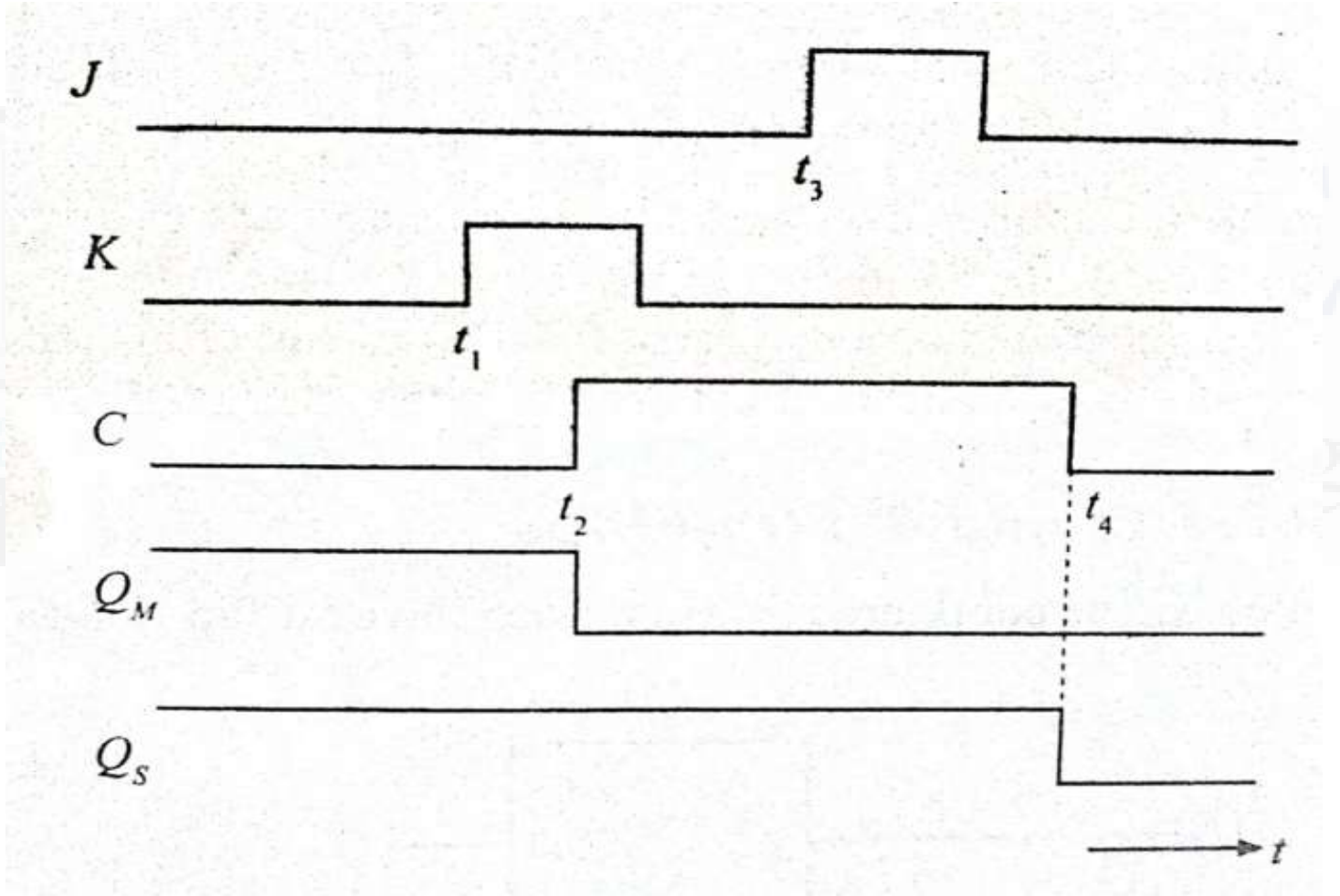
Response of Assignment Solution



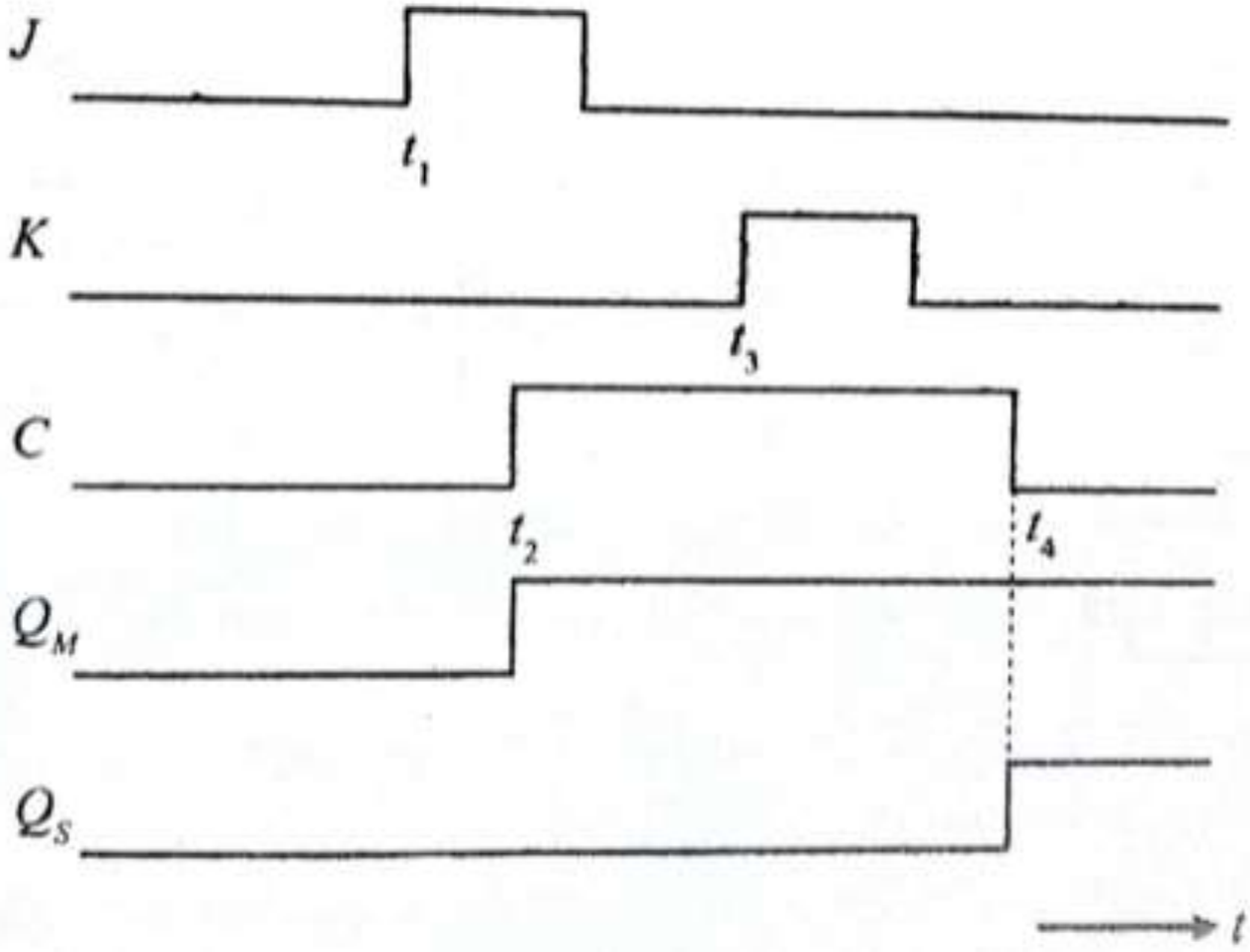
Master Slave J-K Flip Flop



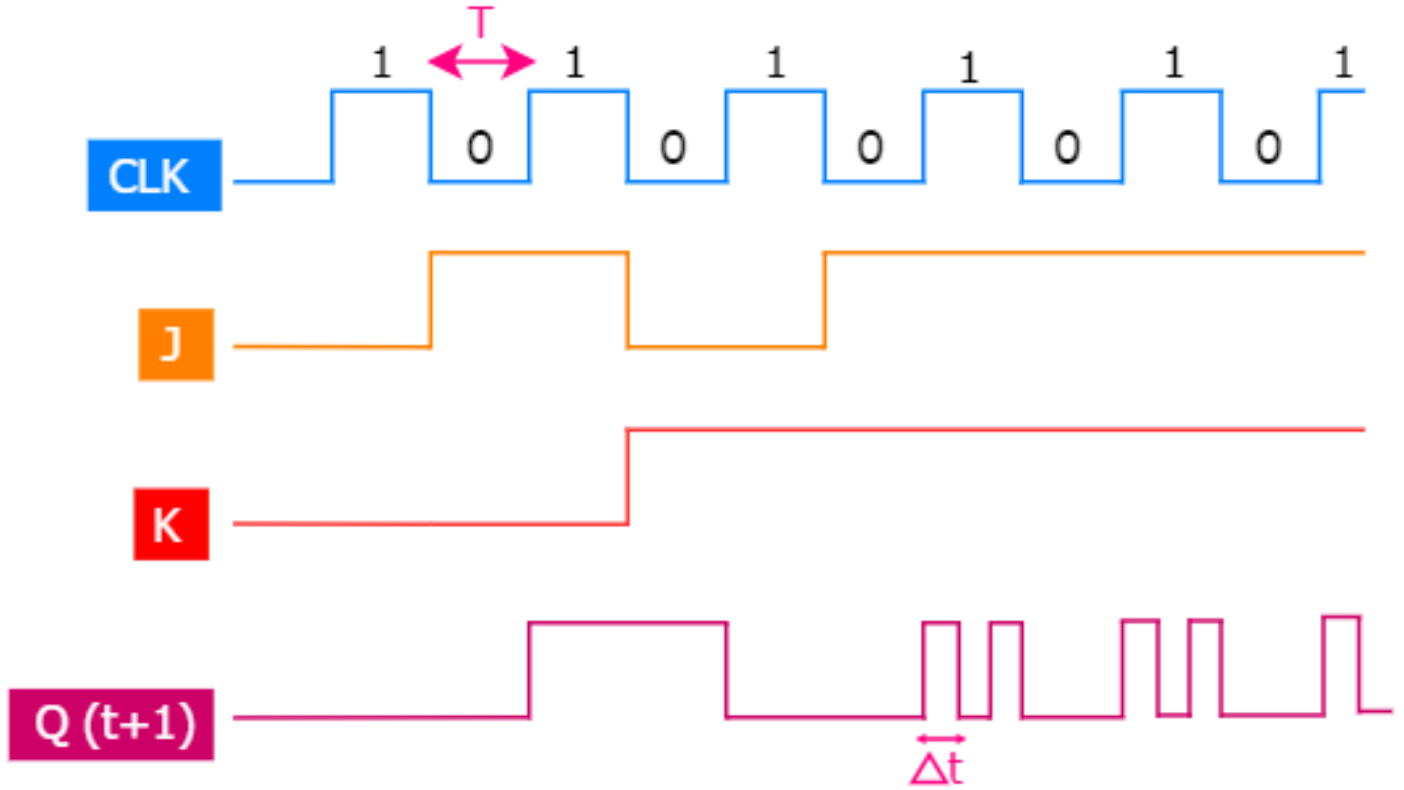
Response of Master Slave J-K Flip Flop to 0's catching



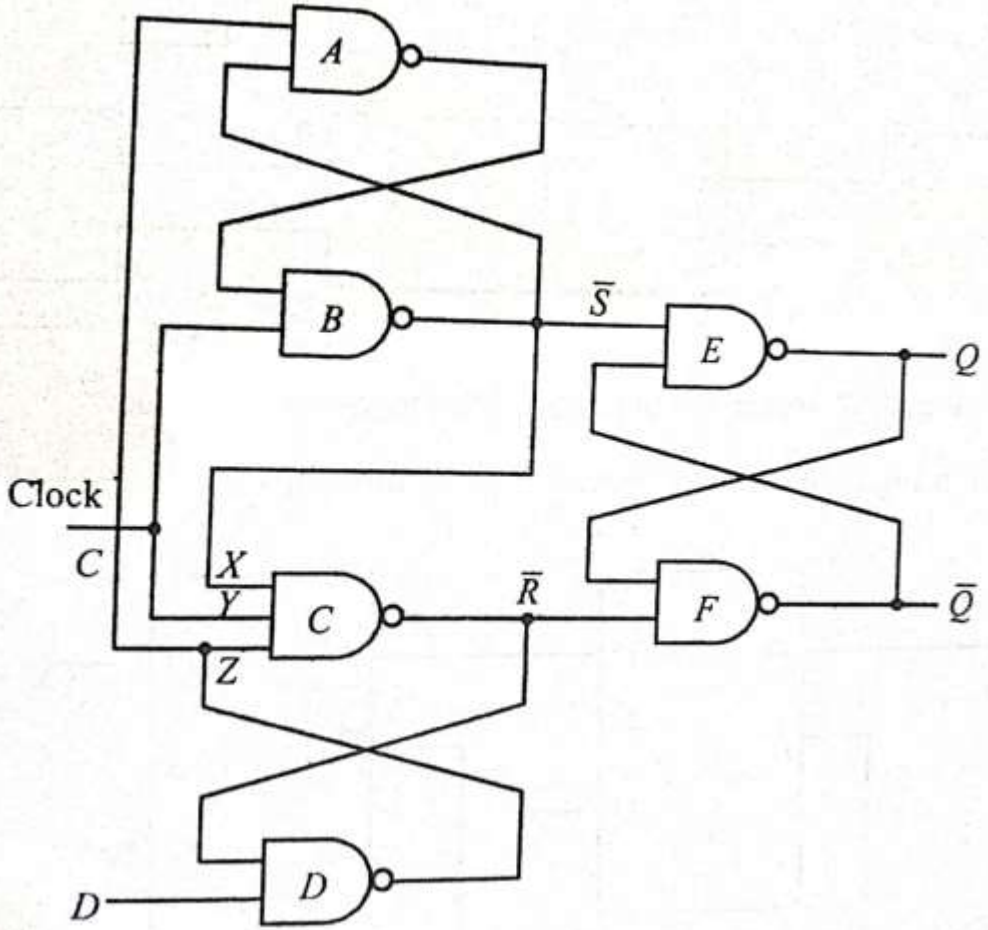
Response of Master Slave J-K Flip Flop to 1's catching



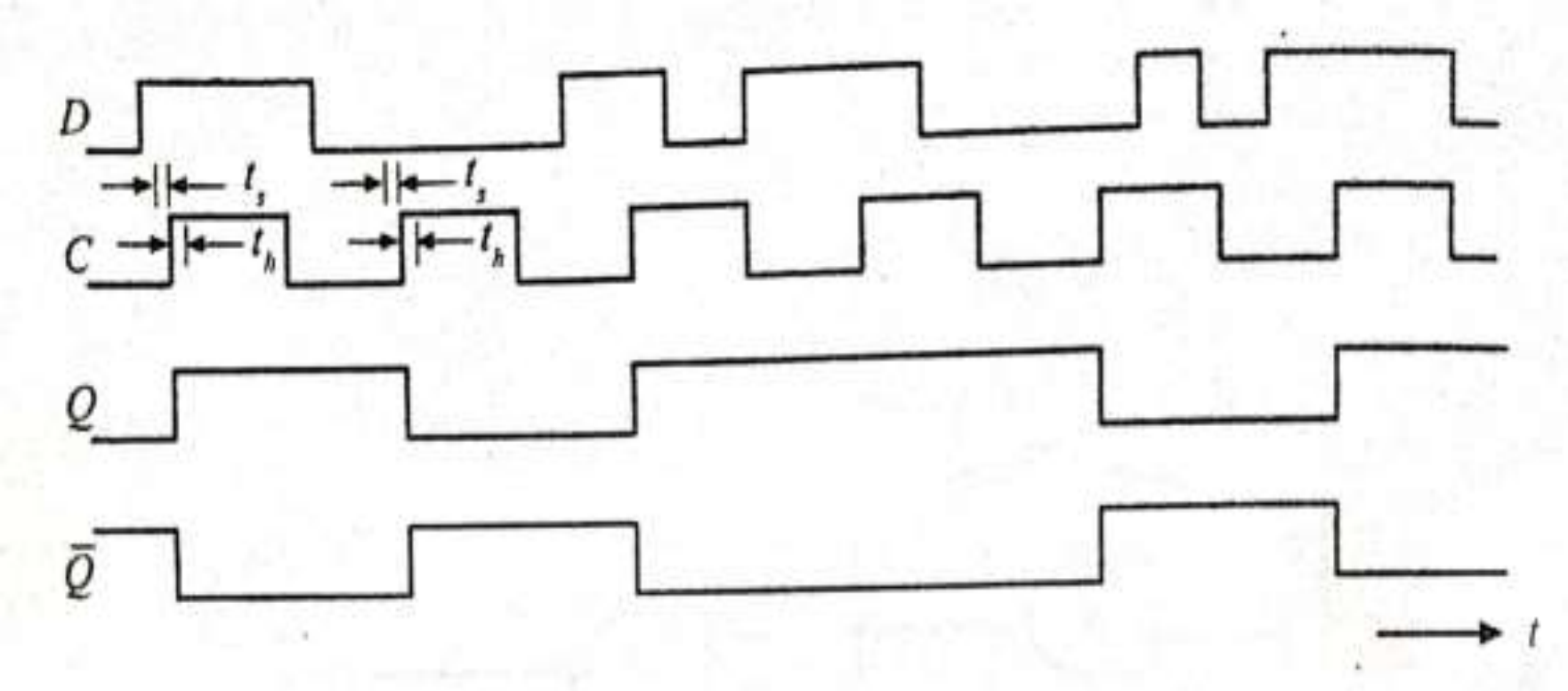
Race Around Condition in Master Slave J-K Flip Flop



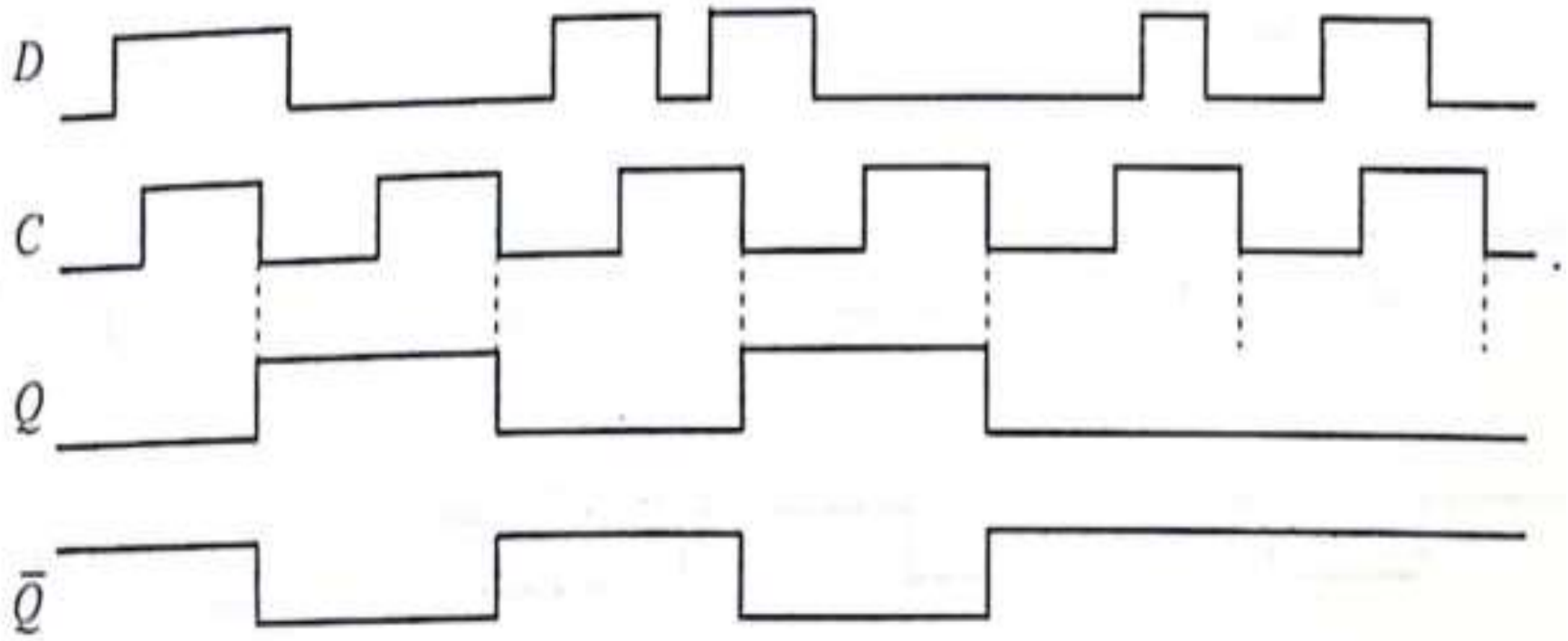
Positive Edge Triggered D Flip Flop



Response of Positive Edge Triggered D Flip Flop



Response of Negative Edge Triggered D Flip Flop



THANK YOU