Digital Logic Circuits – BEE306A

Module-2

Prepared By,

Mrs. Swathi C A

Asst Professor

Dept of EEE

ATMECE, Mysuru

Course Outline

Course Code	Course Title	Core/Elective	Prerequisite	Contact Hours			Total Hrs/ Sessions
				L	T	P	
EE306A	Digital Logic Circuits	Elective	Basic Electronics	3	-	-	40

Module – 1: Principles of Combinational Logic: Definition of combinational logic, canonical forms, Generation of switching equations from truth tables, Karnaugh maps-3,4,5 variables, Incompletely specified functions (Don‘t care terms) Simplifying Max term equations, Quine-McCluskey minimization technique, Quine-McCluskey using don‘t care terms, Reduced prime implicants Tables.	
Bloom’s Taxonomy Level	L1 – Remembering, L2 – Understanding, L3 – Applying, L4 – Analyzing,
Module – 2: Analysis and Design of Combinational logic: General approach to combinational logic design, Decoders, BCD decoders, Encoders, digital multiplexers, Using multiplexers as Boolean function generators, Adders and subtractors, Cascading full adders, Look ahead carry, Binary comparators	
Bloom’s Taxonomy Level	L1 – Remembering, L2 – Understanding, L3 – Applying, L4 – Analysing,
Module – 3: Flip-Flops: Basic Bistable elements, Latches, Timing considerations, The master-slave flip-flops (pulsetriggered flip-flops): SR flip-flops, JK flip-flops, Edge triggered flip- flops, Characteristic equations .	
Bloom’s Taxonomy Level	L1 – Remembering, L2 – Understanding
Module – 4: Flip-Flops Applications: Registers, binary ripple counters, synchronous binary counters, Counters based on shift registers, Design of a synchronous counter, Design of a synchronous mod-n counter using clocked T, JK, D and SR flip-flops.	
Bloom’s Taxonomy Level	L1 – Remembering, L2 – Understanding, L3 – Applying, L – 4 Analysing,
Module – 5: Sequential Circuit Design: Mealy and Moore models, State machine notation, Synchronous Sequential circuit analysis, Construction of state diagrams, counter design. Memories: Read only and Read/Write Memories, Programmable ROM, EPROM, Flash memory.	

Course Outcomes

1. Develop simplified switching equation using Karnaugh Maps and Quine McClusky techniques.[L3]
2. Apply the design procedures for Multiplexer, Encoder, Decoder, Adder, Subtractors and Comparator as digital combinational control circuits.[L3]
3. Illustrate the design of flip flops and development of its characteristic equation.[L2]
4. Apply the design procedures for counters and shift registers as sequential control circuits.[L3]
5. Develop Mealy/Moore Models and state diagrams for the given clocked sequential circuits and Interpret the functioning of Read only and Read/Write Memories, Programmable ROM, EPROM and Flash memory.[L3]

List of Reference Books

1. Digital Logic Applications and Design, John M Yarbrough, Thomson Learning 2001 ISBN 981- 240-062-1.
2. Digital Principles and Design Donald D. Givone McGraw Hill 2002 ISBN 978-0- 07-052906-9.

General Approach

1. Problem Statement
2. Generate Truth Table that give relation between input and output
3. The functions are simplified using K-Map or QM Technique to obtain expression in SOP or POS form
4. Simplified equations are implemented using basic logic gates

General Approach

1.Design a combinational circuit to find 9’s complement of a BCD number

2. Design a combinational circuit to convert BCD to Exess-3

3. Design a combinational circuit to find 2’s complement of a 4-bit number

Note: To get 2's complement of binary number is 1's complement of given number plus 1 to the least significant bit (LSB).

For example 2's complement of binary number 10010 is (01101) + 1 = 01110.

Half Adders

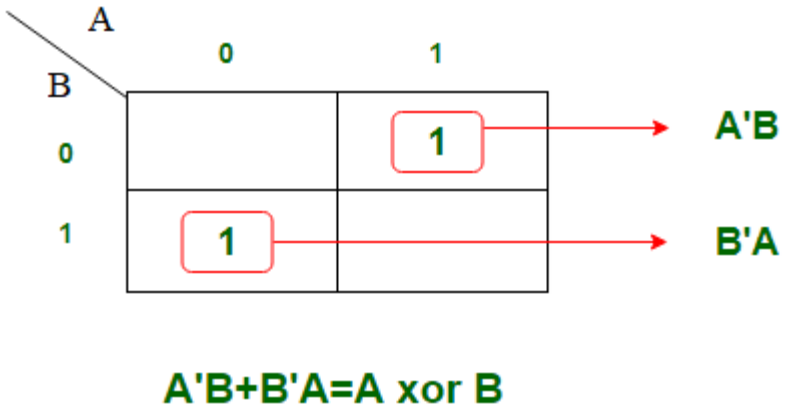
- A combinational logic circuit that performs the addition of two single bits is called Half Adder.

Design of Half-Adder

Boolean function is obtained as

$$S = A \oplus B \qquad C = AB$$

K-Map of Sum:

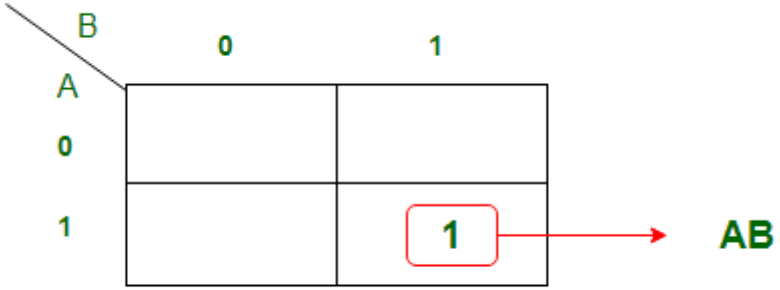


A'B+B'A=A xor B

Truth Table

Inputs		Outputs	
A	B	Sum	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

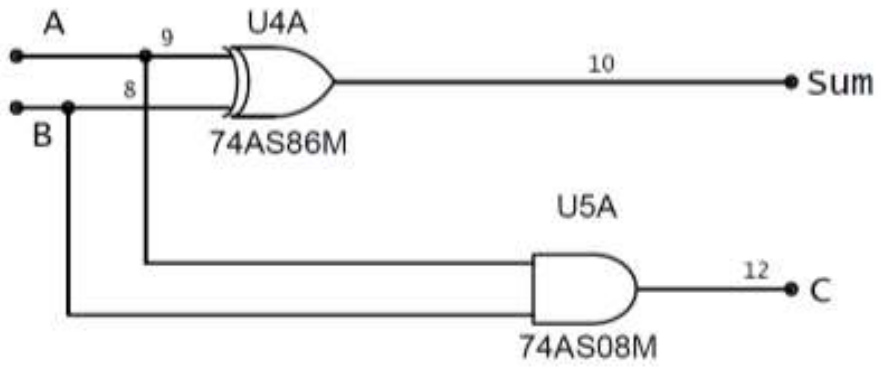
K-Map of Carry:



Design of Half-Adder

Boolean function is obtained as

$S = A \oplus B$ $C = AB$

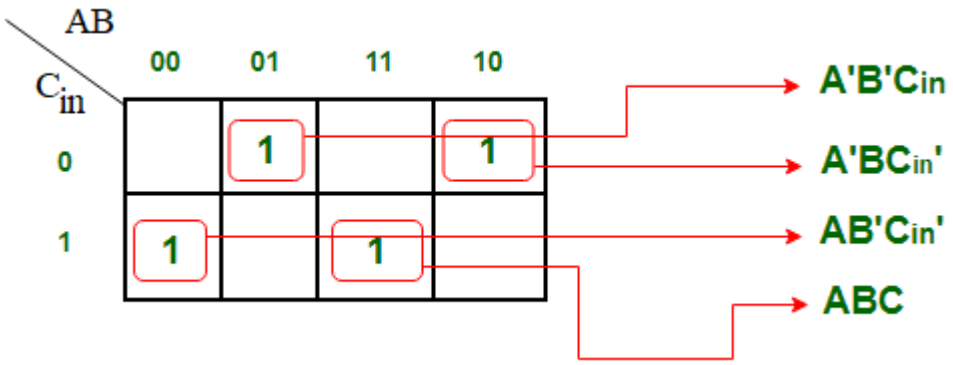


Design of Full Adders:

- A combinational logic circuit that performs the addition of three single bits is called Full Adder.

Design of Full-Adder

K-Map of Sum:



$S = B'(A'C_{in}+AC_{in}') + B(AC + A'C_{in}')$

$S = B'(A \text{ xor } C_{in}) + B\,(A \text{ xor } C_{in})'$

$S = A \text{ xor } B \text{ xor } C_{in}$

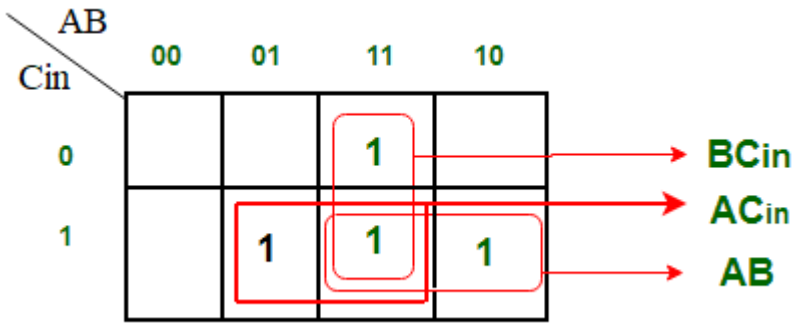
$S = A \oplus B \oplus C$

Truth Table

Inputs			Outputs	
A	B	C in	Sum	C out
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Design of Full-Adder

K-Map of Carry:



$C_{out} = BC_{in} + AB + AC_{in}$

$$Cout = AB + Cin(A \oplus B)$$

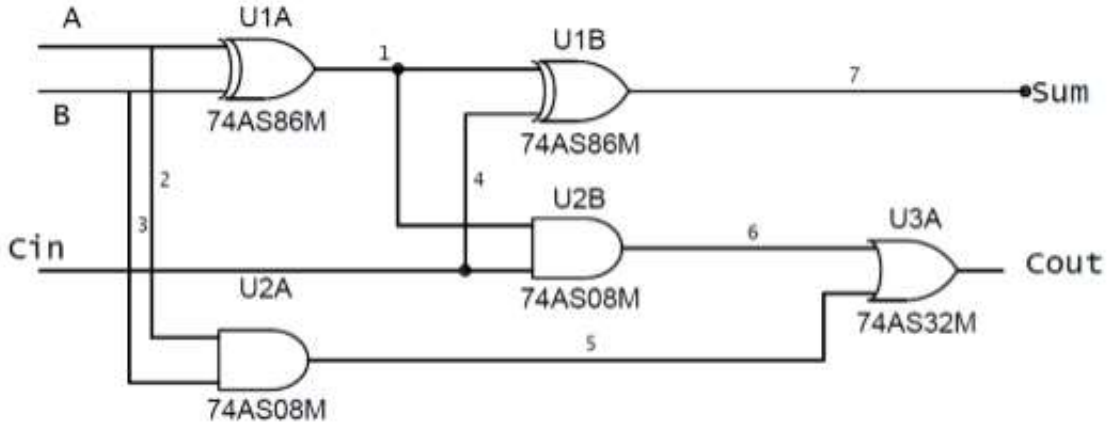
Truth Table

Inputs			Outputs	
A	B	C in	Sum	C out
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Design of Full-Adder

Boolean function is obtained as

$$S = A \oplus B \oplus C \qquad Cout = AB + Cin(A \oplus B)$$



Design of Half Subtractor

Boolean function is obtained as

$$Dif = A \oplus B \qquad Bor = \overline{A}B$$

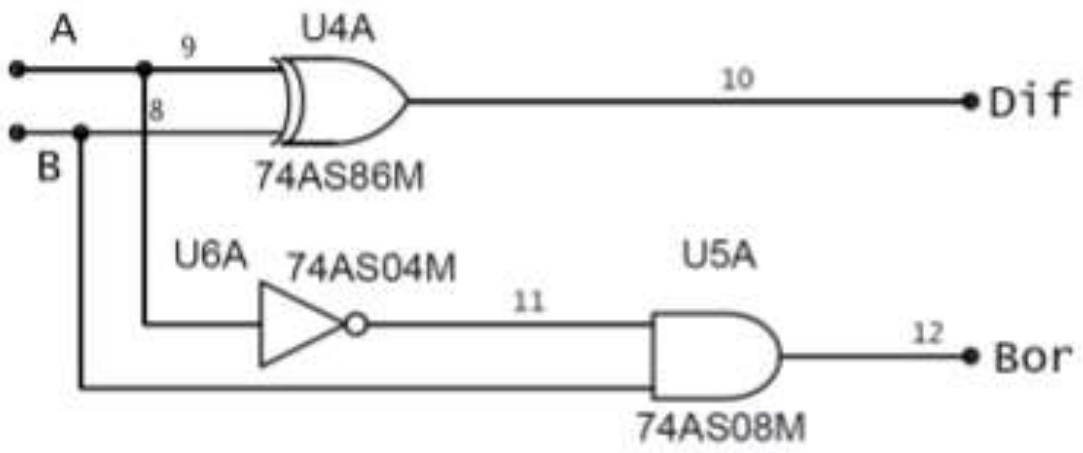


Fig: Circuit for Half Sbtractor

Truth Table

Inputs		Outputs	
A	**B**	**Bor**	**Dif**
0	0	0	0
0	1	1	1
1	0	0	1
1	1	0	0

Design of Full Subtractor

Boolean function is obtained as

$$Dif = A \oplus B \oplus Cin$$

$$Bor\_out = \bar{A}B + (\bar{A} + B)Bor\_in$$

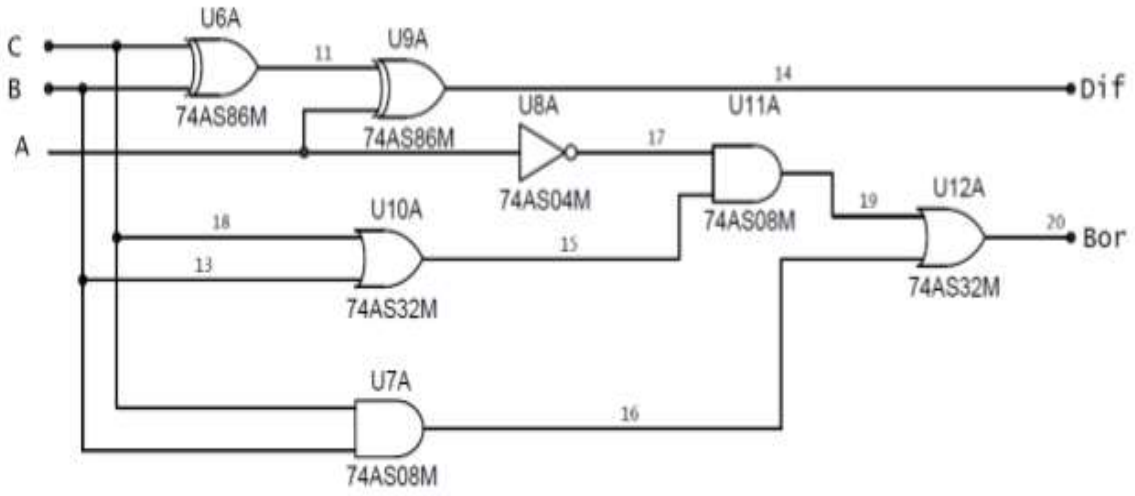


Fig: Circuit for full Sbtractor

Truth Table

Inputs			Outputs	
A	B	C in	Bor	Dif
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	1	0
1	0	0	0	1
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

Decoders

A Decoder is a combinational circuit that converts binary information from n input lines to 2^n unique output lines.

Apart from the Input lines, a decoder may also have an Enable input line.

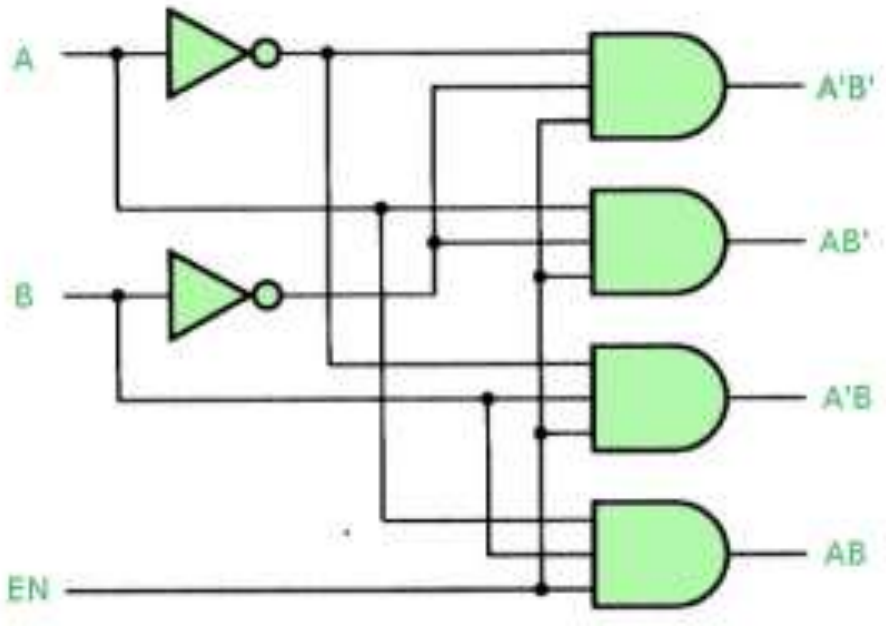
Types of Decoc

- 2 to 4 line decoder
- 3 to 8 line decoder
- 4 to 16 line decoder
- 5 to 32 line decoder

In general, n: 2^n Decoder → n input lines to 2^n unique output lines

2 to 4 line Decoder

2:4 Decoder

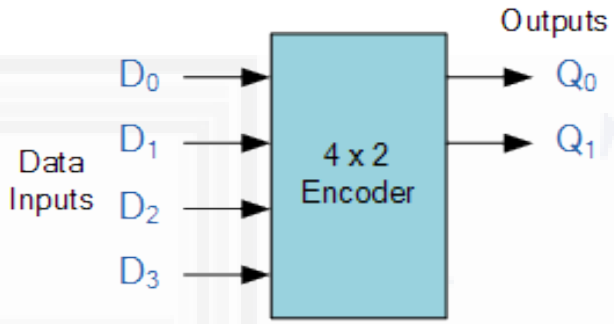


Encoders

1. An “n-bit” binary encoder has 2n input lines and n-bit output lines with common types that include 4-to-2, 8-to-3 and 16-to-4 line configurations.
2. Various Types of Encoder
3. 4 to 2 line Encoder
4. 8 – 3 Line Encoder

Encoders

1. 4 to 2 line Encoder



Inputs				Outputs	
D_3	D_2	D_1	D_0	Q_1	Q_0
0	0	0	1	0	0
0	0	1	0	0	1
0	1	0	0	1	0
1	0	0	0	1	1
0	0	0	0	x	x

Disadvantage:

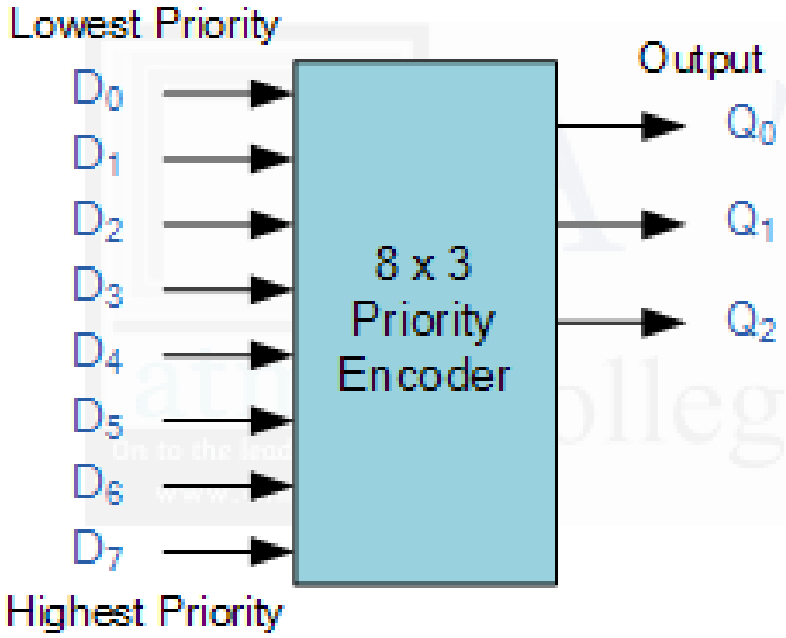
- if we make inputs D1 and D2 HIGH at logic “1” both at the same time, the resulting output is neither at “01” or at “10” but will be at “11” which is an output binary number that is different to the actual input present

Encoders

- One simple way to overcome this problem is to “Prioritise” the level of each input pin
- So if there is more than one input at logic level “1” at the same time, the actual output code would only correspond to the input with the highest designated priority.
- Then this type of digital encoder is known commonly as a Priority Encoder

Encoders

1. 8 to 3 Line Encoder



Inputs								Outputs		
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Q_2	Q_1	Q_0
0	0	0	0	0	0	0	1	0	0	0
0	0	0	0	0	0	1	x	0	0	1
0	0	0	0	0	1	x	x	0	1	0
0	0	0	0	1	x	x	x	0	1	1
0	0	0	1	x	x	x	x	1	0	0
0	0	1	x	x	x	x	x	1	0	1
0	1	x	x	x	x	x	x	1	1	0
1	x	x	x	x	x	x	x	1	1	1

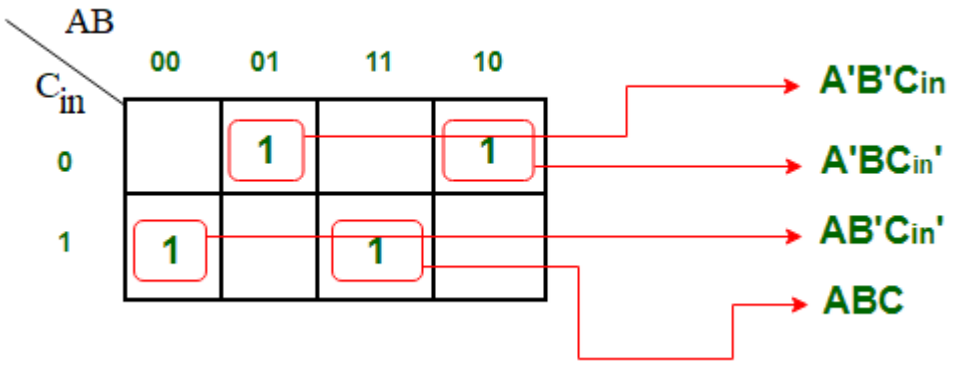
X = dont care

Truth Table

Digital Inputs								Binary Output		
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Q_2	Q_1	Q_0
0	0	0	0	0	0	0	**1**	0	0	0
0	0	0	0	0	0	**1**	X	0	0	1
0	0	0	0	0	**1**	X	X	0	1	0
0	0	0	0	**1**	X	X	X	0	1	1
0	0	0	**1**	X	X	X	X	1	0	0
0	0	**1**	X	X	X	X	X	1	0	1
0	**1**	X	X	X	X	X	X	1	1	0
1	X	X	X	X	X	X	X	1	1	1

Design of Full-Adder

K-Map of Sum:



$S = B'(A'C_{in}+AC_{in}') + B(AC + A'C_{in}')$

$S = B'(A \text{ xor } C_{in}) + B\,(A \text{ xor } C_{in})'$

$S = A \text{ xor } B \text{ xor } C_{in}$

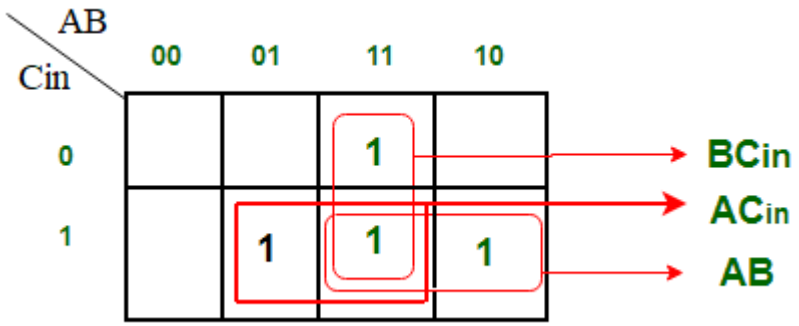
$$S = A \oplus B \oplus C$$

Truth Table

Inputs			Outputs	
A	B	C in	Sum	C out
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Design of Full-Adder

K-Map of Carry:



$C_{out} = BC_{in} + AB + AC_{in}$

$$Cout = AB + Cin(A \oplus B)$$

Truth Table

Inputs			Outputs	
A	B	C in	Sum	C out
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

THANK YOU