A T M E
College of Engineering

Digital Logic Circuits– BEE306A

Module - 4

Prepared By,

Ms. Swathi C A

Asst Professor

Dept of EEE

ATMECE, Mysuru

Course Outline

Course Code	Course Title	Core/Elective	Prerequisite	Contact Hours			Total Hrs/ Sessions
				L	T	P	
BEE306A	Digital Logic Circuits	Elective	Basic Electronics	3	-	-	40

Module – 1: Principles of Combinational Logic: Definition of combinational logic, canonical forms, Generation of switching equations from truth tables, Karnaugh maps-3,4,5 variables, Incompletely specified functions (Don‘t care terms) Simplifying Max term equations, Quine-McCluskey minimization technique, Quine-McCluskey using don‘t care terms, Reduced prime implicants Tables.	
Bloom’s Taxonomy Level	L1 – Remembering, L2 – Understanding, L3 – Applying, L4 – Analyzing,
Module – 2: Analysis and Design of Combinational logic: General approach to combinational logic design, Decoders, BCD decoders, Encoders, digital multiplexers, Using multiplexers as Boolean function generators, Adders and subtractors, Cascading full adders, Look ahead carry, Binary comparators	
Bloom’s Taxonomy Level	L1 – Remembering, L2 – Understanding, L3 – Applying, L4 – Analysing,
Module – 3: Flip-Flops: Basic Bistable elements, Latches, Timing considerations, The master-slave flip-flops (pulsetriggered flip-flops): SR flip-flops, JK flip-flops, Edge triggered flip- flops, Characteristic equations .	
Bloom’s Taxonomy Level	L1 – Remembering, L2 – Understanding
Module – 4: Flip-Flops Applications: Registers, binary ripple counters, synchronous binary counters, Counters based on shift registers, Design of a synchronous counter, Design of a synchronous mod-n counter using clocked T, JK, D and SR flip-flops.	
Bloom’s Taxonomy Level	L1 – Remembering, L2 – Understanding, L3 – Applying, L – 4 Analysing,
Module – 5: Sequential Circuit Design: Mealy and Moore models, State machine notation, Synchronous Sequential circuit analysis, Construction of state diagrams, counter design. Memories: Read only and Read/Write Memories, Programmable ROM, EPROM, Flash memory.	

Course Outcomes

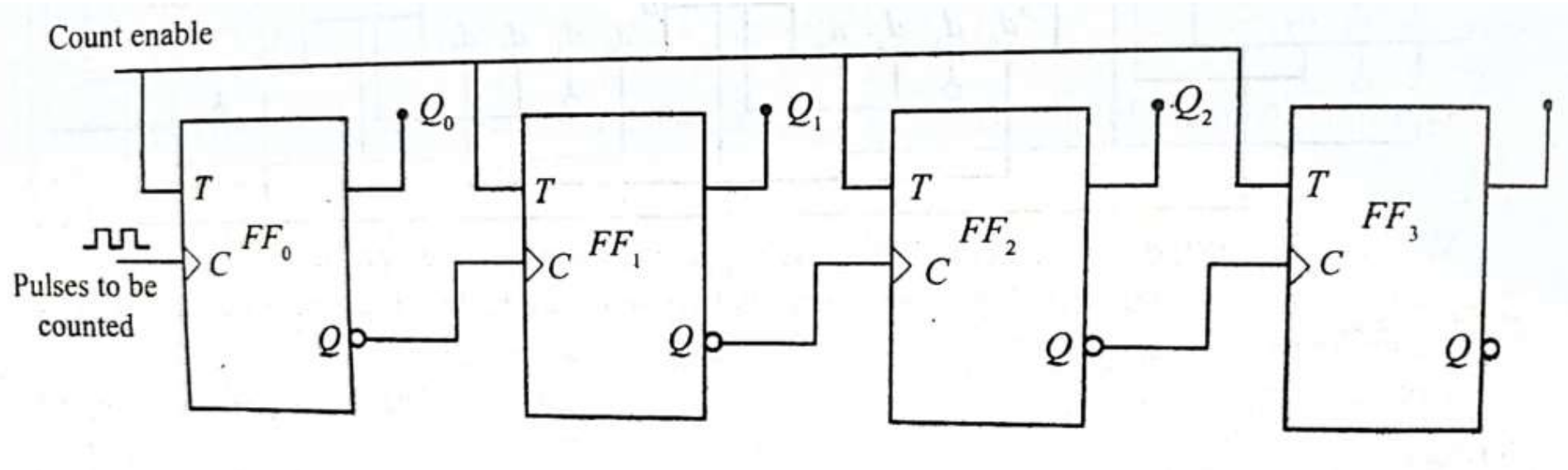
1. Develop simplified switching equation using Karnaugh Maps and Quine McClusky techniques.[L3]
2. Apply the design procedures for Multiplexer, Encoder, Decoder, Adder, Subtractors and Comparator as digital combinational control circuits.[L3]
3. Illustrate the design of flip flops and development of its characteristic equation.[L2]
4. Apply the design procedures for counters and shift registers as sequential control circuits.[L3]
5. Develop Mealy/Moore Models and state diagrams for the given clocked sequential circuits and Interpret the functioning of Read only and Read/Write Memories, Programmable ROM, EPROM and Flash memory.[L3]

List of Reference Books

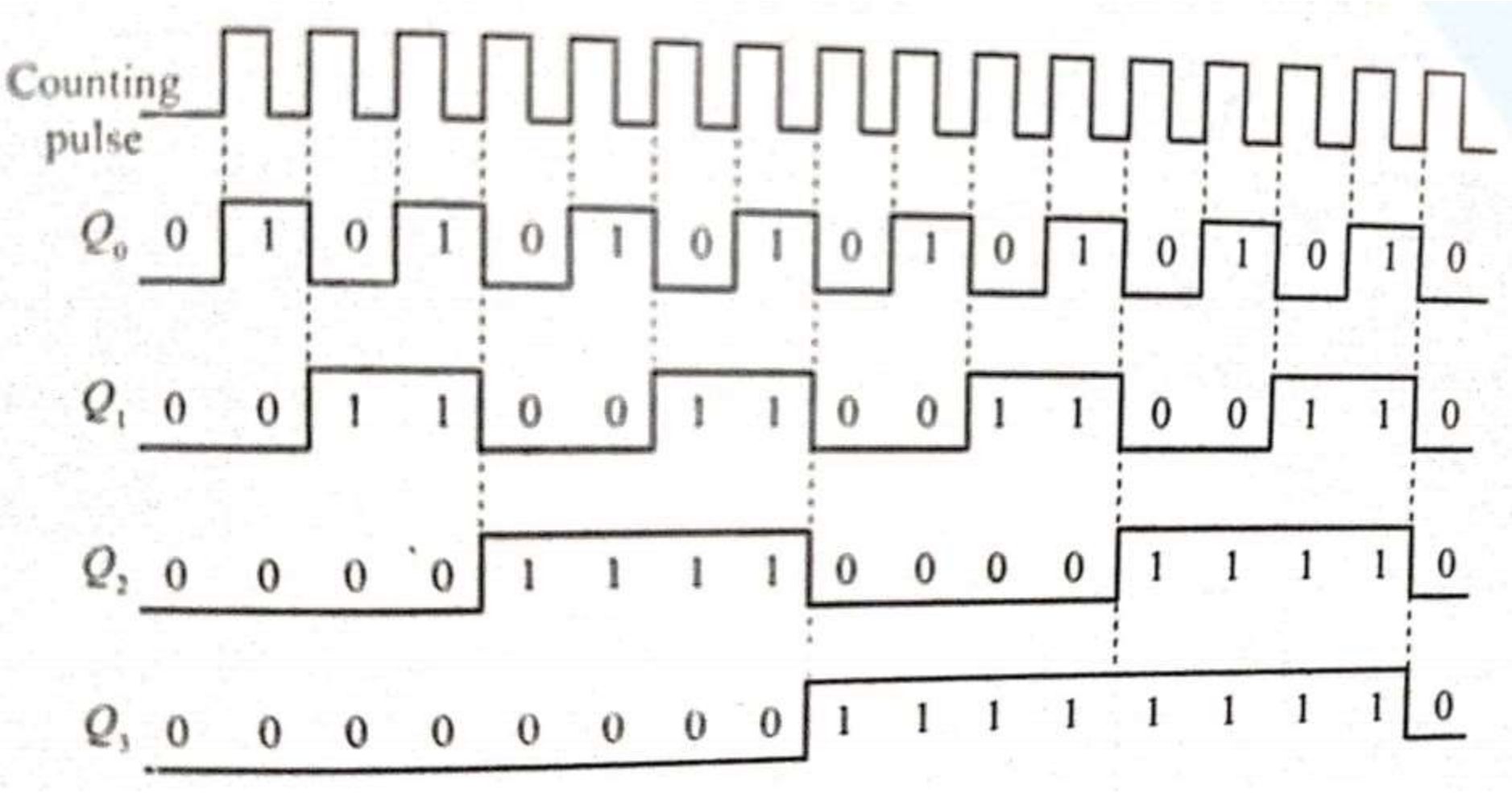
1. Digital Logic Applications and Design, John M Yarbrough, Thomson Learning 2001 ISBN 981- 240-062-1.
2. Digital Principles and Design Donald D. Givone McGraw Hill 2002 ISBN 978-0- 07-052906-9.

Counters

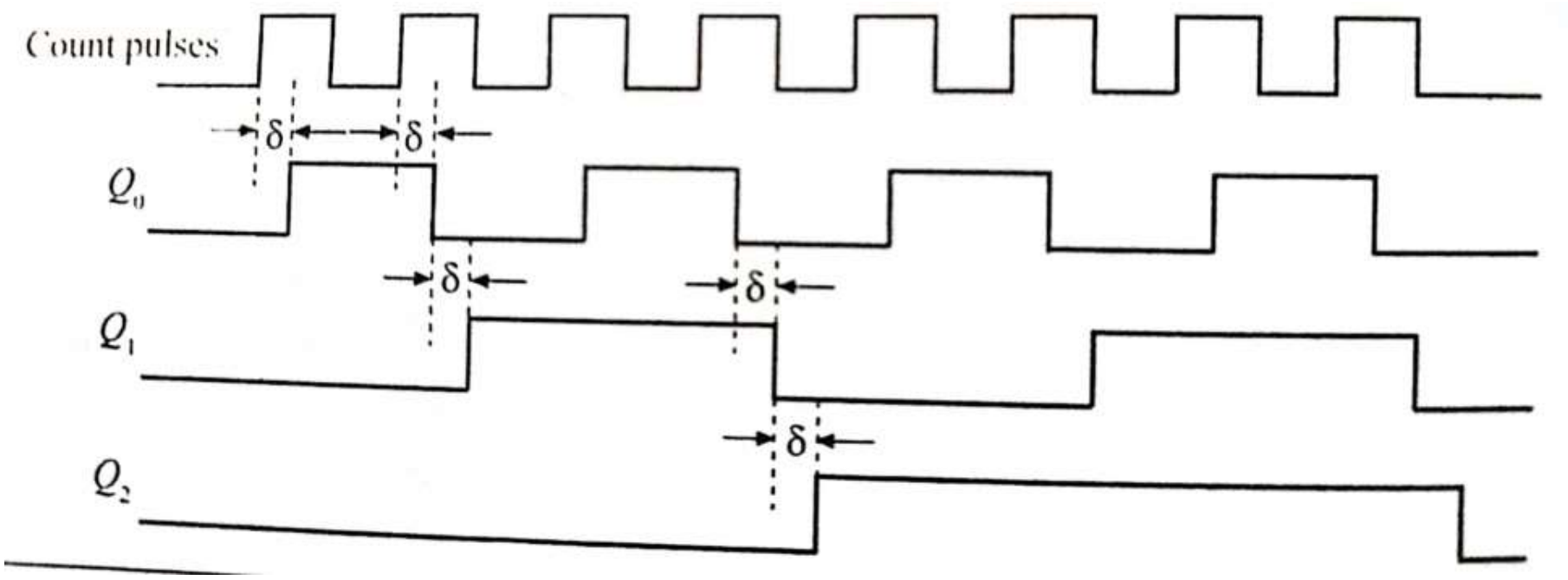
- Binary Ripple Counter using T Flip Flop



Timing Diagram Binary Ripple Counter using T Flip Flop

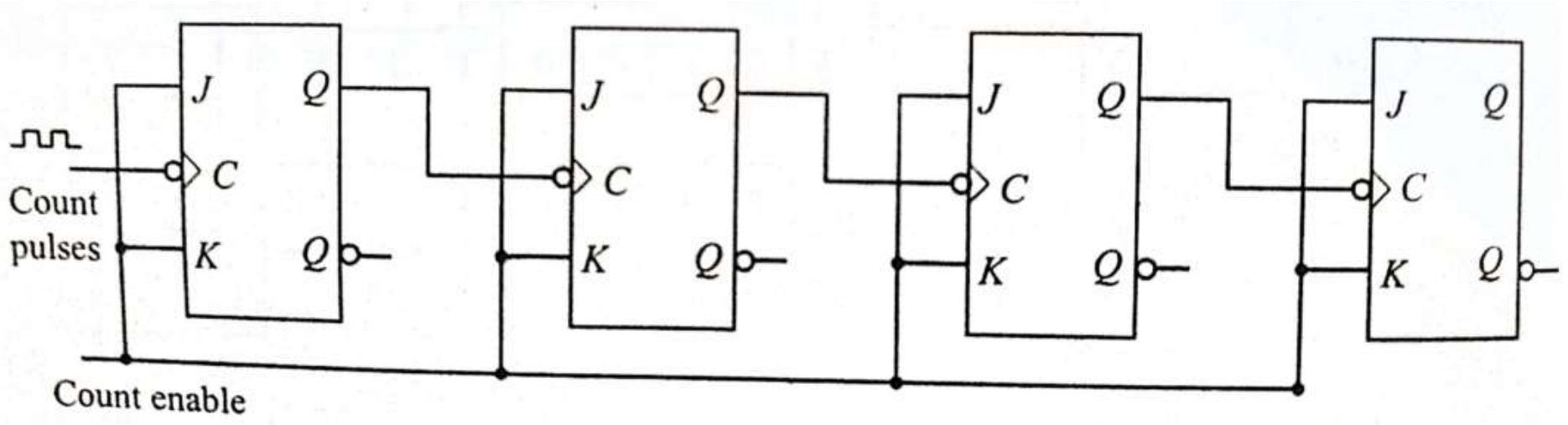


Timing Diagram Binary Ripple Counter using Delay

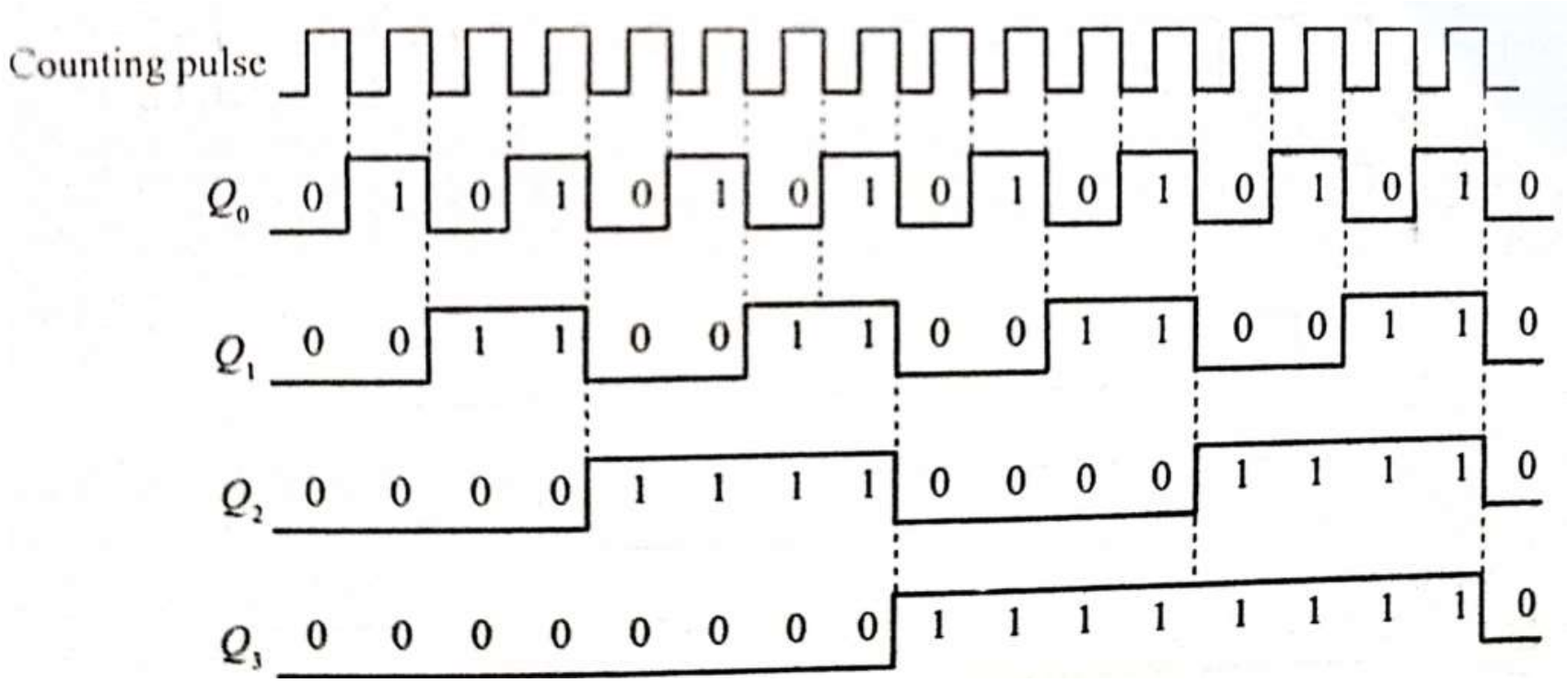


Design of a Binary Ripple Counter using J K Flip Flop

- At J = K=1 , Output Q -- Toggles

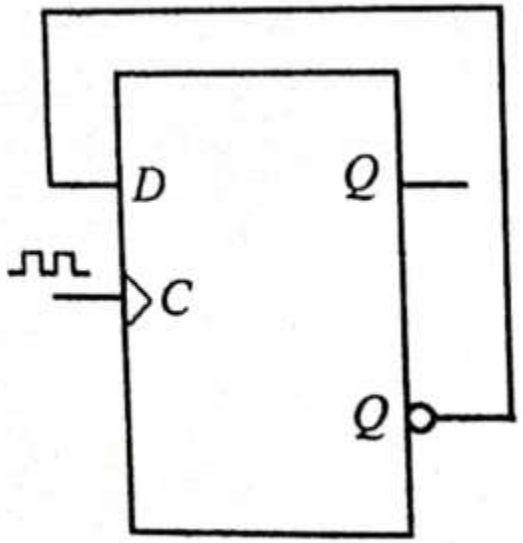


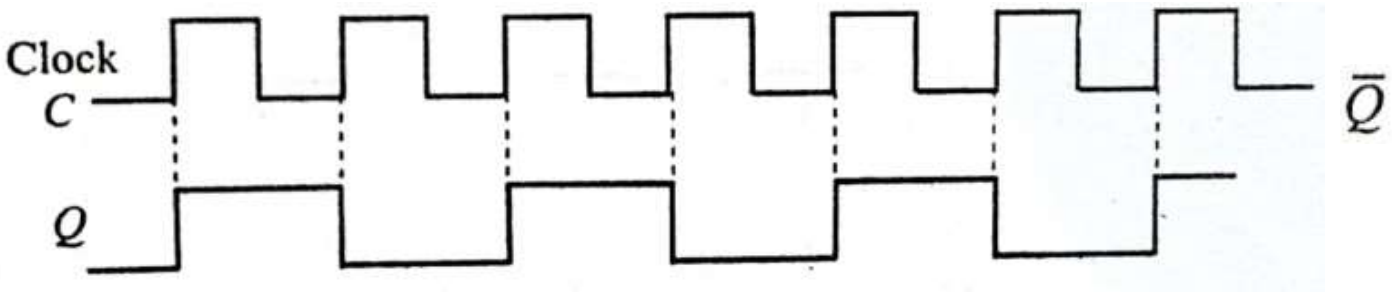
Timing Diagram of Binary Ripple Counter using J K Flip Flop



Binary Ripple Counter using D Flip Flop

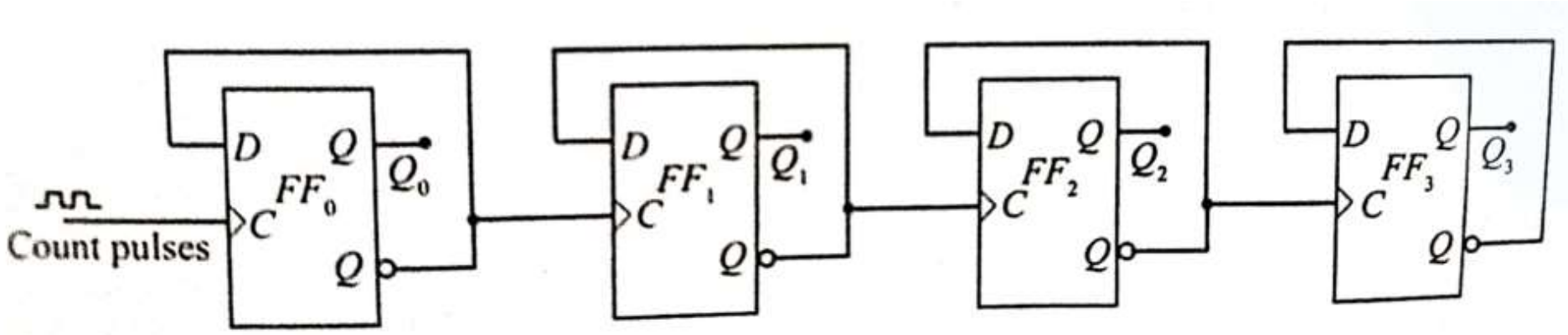
Output Toggles When D is connected to



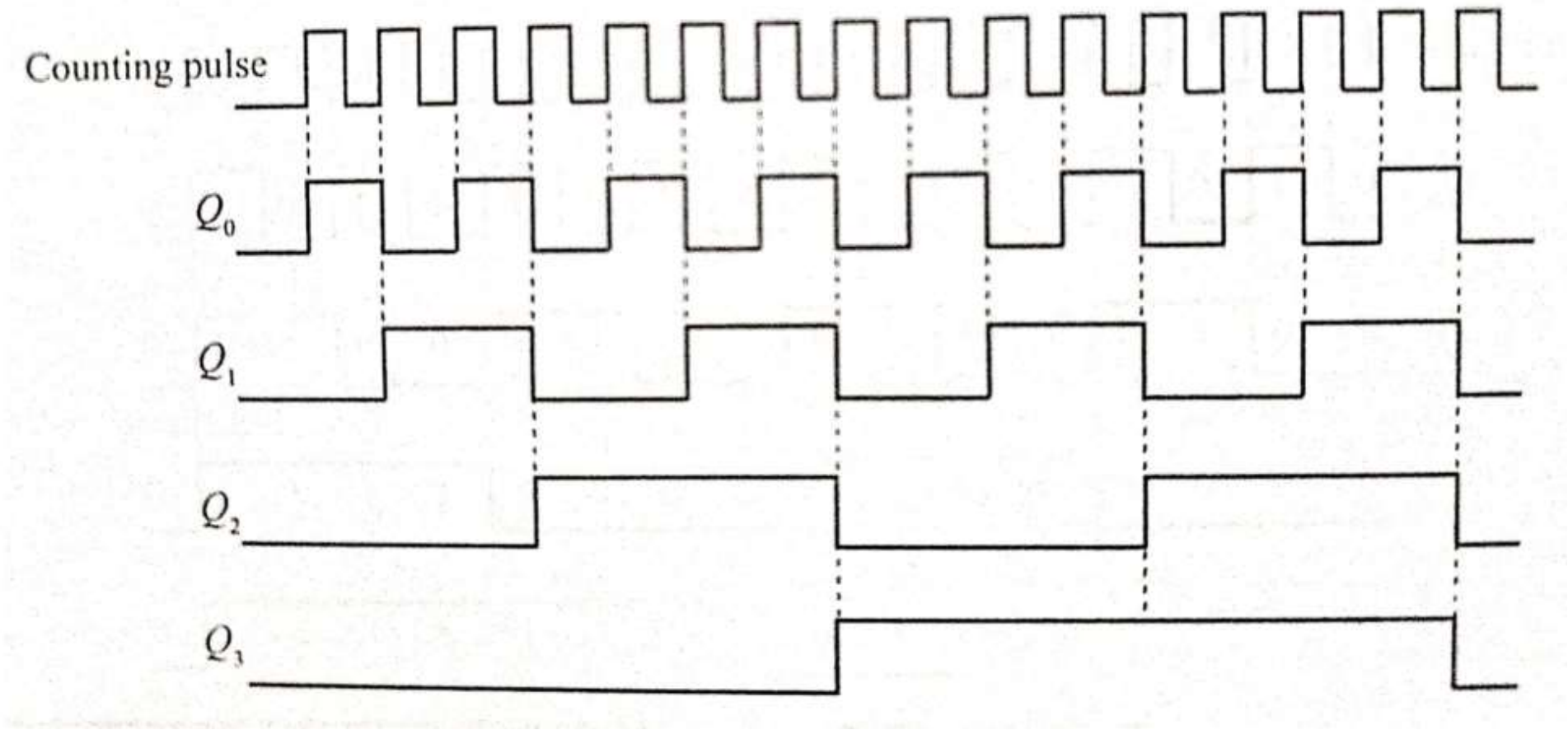


Binary Ripple Counter using D Flip Flop

4-Bit Counter



Timing Diagram of Binary Ripple Counter using D Flip Flop



THANK YOU