Analog Electronic Circuits-BEE303

Course Credit Description

Sl. No.	Course Code	Course Type	Course	Teaching Hours /Week	Exam Duration in Hours	SEE Marks	CIE Marks	Total Marks	Credits
1	BEE303	IPCC	Analog Electronic Circuits	(3Theory + 2 Tutorial)	3	50	50	100	4

Course Objectives:

1. Provide the knowledge for the analysis of diode and transistor circuits.
2. Develop skills to design the electronic circuits using transistors and Op-amps.
3. To understand the concept and various types of converters.

Course Contents

Module – 1
Module-1: Diode Circuits: Diode clipping and clamping circuits. **Transistor Biasing and Stabilization**: The operating point, load line analysis, DC analysis and design of fixed bias circuit, emitter stabilized bias circuit, collector to base bias circuit, voltage divider bias circuit, modified DC bias with voltage feedback. **Bias stabilization and stability factors** for fixed bias circuit, collector to base bias circuit and voltage divider bias circuit, bias compensation, Transistor switching circuits
Bloom's Taxonomy Level **L1 – Remembering, L2 – Understanding, L3 – Applying. L4 – Analysing**
Module - 2
Module-2: Transistor at Low Frequencies: Hybrid model, h-parameters for CE, CC and CB modes, mid-band analysis of single stage amplifier, simplified hybrid model, analysis for CE, CB and CC(emitter voltage follower circuit) modes, Millers Theorem and its dual, analysis for collector to base bias circuit and CE with un bypassed emitter resistance. **Transistor frequency response:** General frequency considerations, effect of various capacitors on frequency response, Miller effect capacitance, high frequency response, hybrid
Bloom's Taxonomy Level **L1 – Remembering, L2 – Understanding, L3 – Applying. L4 – Analysing.**

Course Contents

Module - 3
Module-3: Multistage amplifiers: Cascade connection, analysis for CE-CC mode, CE-CE mode, CASCODE stage-unbypassed and bypassed emitter resistance modes, Darlington connection using h-parameter model. **Feedback Amplifiers:** Classification of feedback amplifiers, concept of feedback, general characteristics of negative feedback amplifiers, Input and output resistance with feedback of various feedback amplifiers, analysis of different practical feedback amplifier circuits
Bloom's Taxonomy Level **L1 – Remembering, L2 – Understanding, L3 – Applying, L4 – Analysing.**
Module - 4
Module-4: Power Amplifiers: Classification of power amplifiers, Analysis of class A, Class B, class C and Class AB amplifiers, Distortion in power amplifiers, second harmonic distortion, harmonic distortion in Class B amplifiers, cross over distortion and elimination of cross over distortion. **Oscillators:** Concept of positive feedback, frequency of oscillation for RC phase oscillator, Wien Bridge oscillator, Tuned oscillator circuits, Hartley oscillator, Colpitt's oscillator , crystal oscillator and its types
Bloom's Taxonomy Level **L1 – Remembering, L2 – Understanding, L3 – Applying, L4 – Analysing**
Module - 5
Module-5: Construction, working and characteristics of JFET and MOSFET(enhance and Depletion type) Biasing of JFET and MOSFET. Fixed bias configuration, self bias configuration, voltage divider biasing. Analysis and design of JFET (only common source configuration with fixed bias) and MOSFET amplifiers.
Bloom's Taxonomy Level **L1 – Remembering, L2 – Understanding, L3 – Applying, L4 – Analysing**

Course Outcomes

At the end of the course the students will be able to:

1. Produce the preliminary design of the transistor biasing circuits, switching circuits and also to predict the output response of clipper and clamper circuits.
2. Develop the model of transistor amplifiers for their h-parameters at low frequencies.
3. Analyse and produce the preliminary design of the multistage and feedback amplifiers.
4. Analyse and produce the preliminary design of the power amplifier circuits and oscillators for different frequencies.
5. Analyse and produce the preliminary design of the FET and MOSFET amplifiers.

Text Books and Reference Books

1. **"Electronic devices and circuit theory"**, Robert L Boylestad and Louis Nashelsky, Pearson, 11th Eidition 2015.
2. **"Electronic devices and circuits",** Millman and Halkias, McGraw Hill, 4th Edition 2015.
3. **"Electronic devices and circuits",** David A Bell, Oxford University Press, 5th edition 2008.
4. **"Microelectronics circuits analysis and design",** Muhammad Rashid, 2nd Edition 2014.
5. **"A Textbook of Electrical technology, Electronic devices and circuits"** by B.L.Theraja and A.K.Theraja, 2013.
6. **"Fundamentals of analog circuits",** Thomas L Floyd, 2nd Edition 2012.
7. **"Analog Electronic Circuits",** U B Mahadevaswamy.

Basic Concepts

Conductors

It is an object or a type of material that allows flow of charge (electrical current) in one or more directions.

Examples: Copper wire, Aluminium Wire

Insulators:

It is a material in which the electron does not flow freely. Insulators does not conduct.

Examples: Glass, Porcelain, Paper, Rubber etc.

Semiconductors:

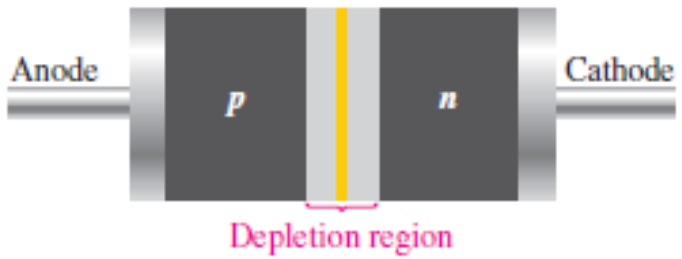
A semiconductor material has an electrical conductivity value falling between that of a conductor and an insulator.

Examples: Silicon, Germanium, Gallium Arsenide

Semiconductor Devices

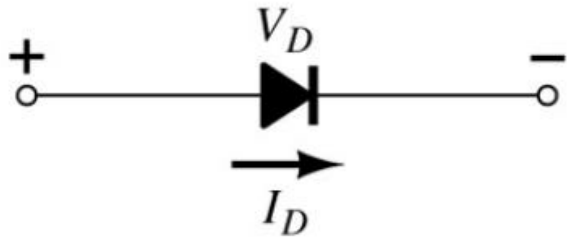
- Diode
- Bipolar Junction Transistor (BJT)
- Field Effect Transistor (FET)
- Metal Oxide Semiconductor Field Effect Transistor (MOSFET)
- Thyristors
- Insulated Gate Bipolar Junction Transistor (IGBT)

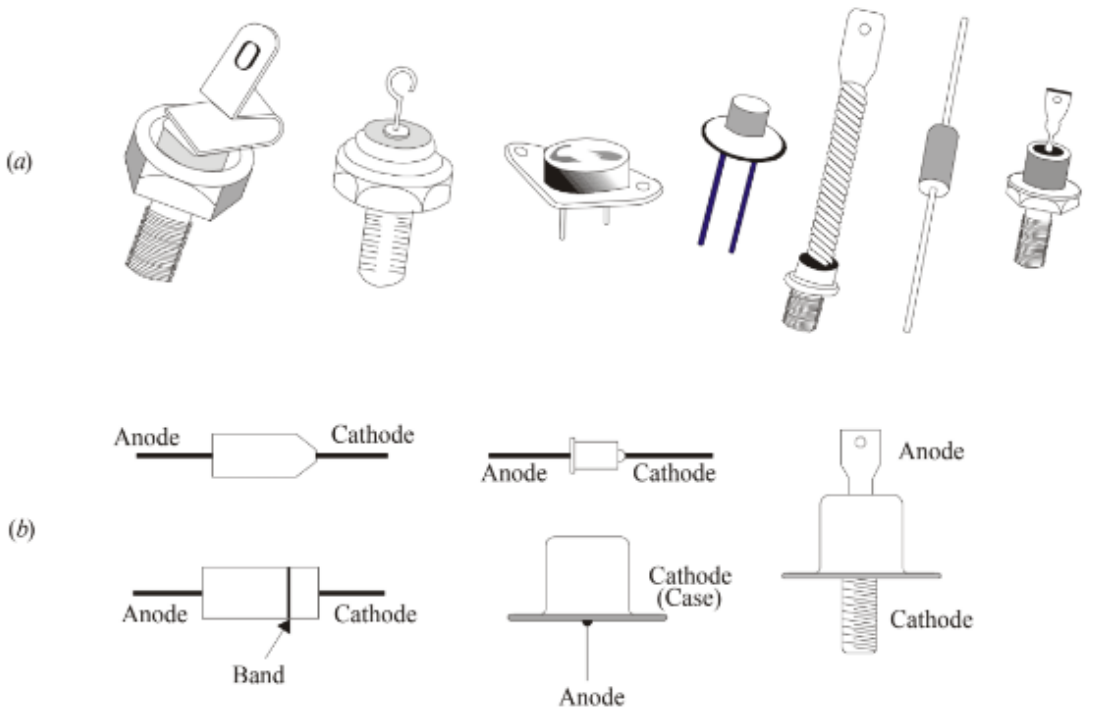
The Diode



(a) Basic structure

(b) Symbol





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SEMICONDUCTOR®

1N4001 - 1N4007

Features

- Low forward voltage drop.
- High surge current capability.

DO-41
COLOR BAND DENOTES CATHODE

General Purpose Rectifiers

Absolute Maximum Ratings*

T_A = 25°C unless otherwise noted

Symbol	Parameter	Value							Units
		4001	4002	4003	4004	4005	4006	4007	
V_{RRM}	Peak Repetitive Reverse Voltage	50	100	200	400	600	800	1000	V
$I_{F(AV)}$	Average Rectified Forward Current, .375 " lead length @ T_A = 75°C	1.0							A
I_{FSM}	Non-repetitive Peak Forward Surge Current 8.3 ms Single Half-Sine-Wave	30							A
T_{stg}	Storage Temperature Range	-55 to +175							°C
T_J	Operating Junction Temperature	-55 to +175							°C

*These ratings are limiting values above which the serviceability of any semiconductor device may be impaired.

Thermal Characteristics

Symbol	Parameter	Value	Units
P_D	Power Dissipation	3.0	W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	50	°C/W

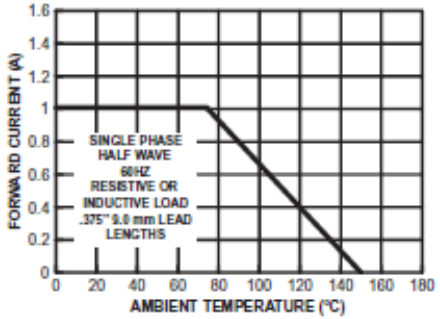
Electrical Characteristics

T_A = 25°C unless otherwise noted

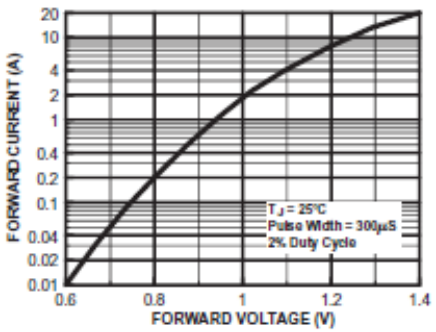
Symbol	Parameter	Device							Units
		4001	4002	4003	4004	4005	4006	4007	
V_F	Forward Voltage @ 1.0 A	1.1							V
I_{rr}	Maximum Full Load Reverse Current, Full Cycle T_A = 75°C	30							µA
I_R	Reverse Current @ rated V_R T_A = 25°C	5.0							µA
	T_A = 100°C	500							µA
C_T	Total Capacitance V_R = 4.0 V, f = 1.0 MHz	15							pF

Typical Characteristics

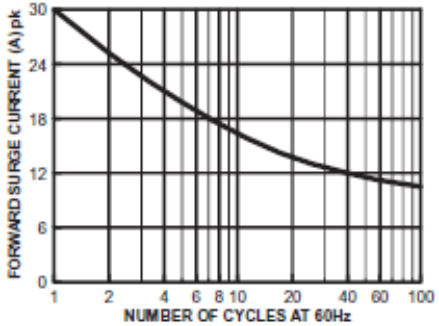
Forward Current Derating Curve



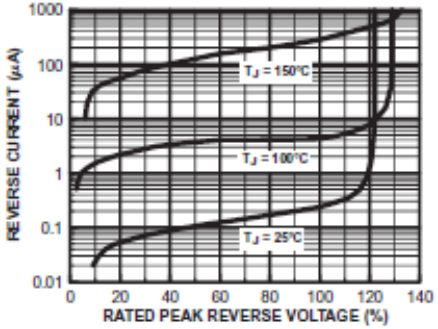
Forward Characteristics



Non-Repetitive Surge Current

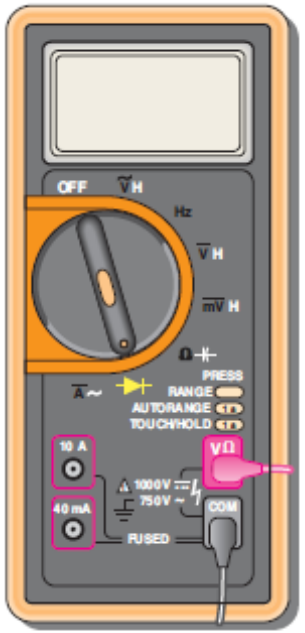


Reverse Characteristics



Testing a Diode

- When function switch set to diode test position, the meter provides an internal voltage sufficient to forward-bias and reverse-bias a diode. This internal voltage may vary among different makes of DMM, but 2.5 V to 3.5 V is a typical range of values.

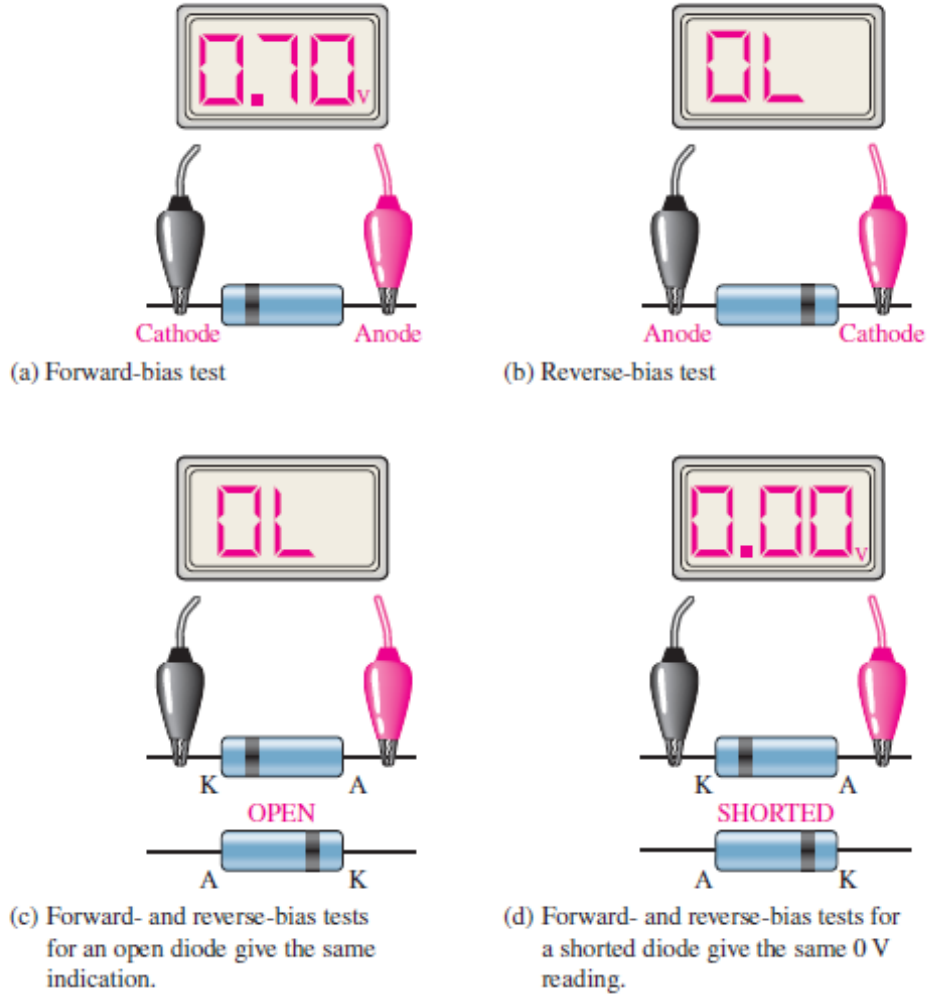


When the Diode Is Working

- The red (positive) lead of the meter is connected to the anode and the black (negative) lead is connected to the cathode to forward bias the diode.

- If the diode is good, you will get a reading of between approximately 0.5 V and 0.9 V, with 0.7 V being typical for forward bias.

- The diode is turned around for reverse bias as shown.
- If the diode is working properly, you will typically get a reading of "OL." out-of-range indication
- Some DMMs may display the internal voltage for a reverse-bias condition.



▲ FIGURE 2–76

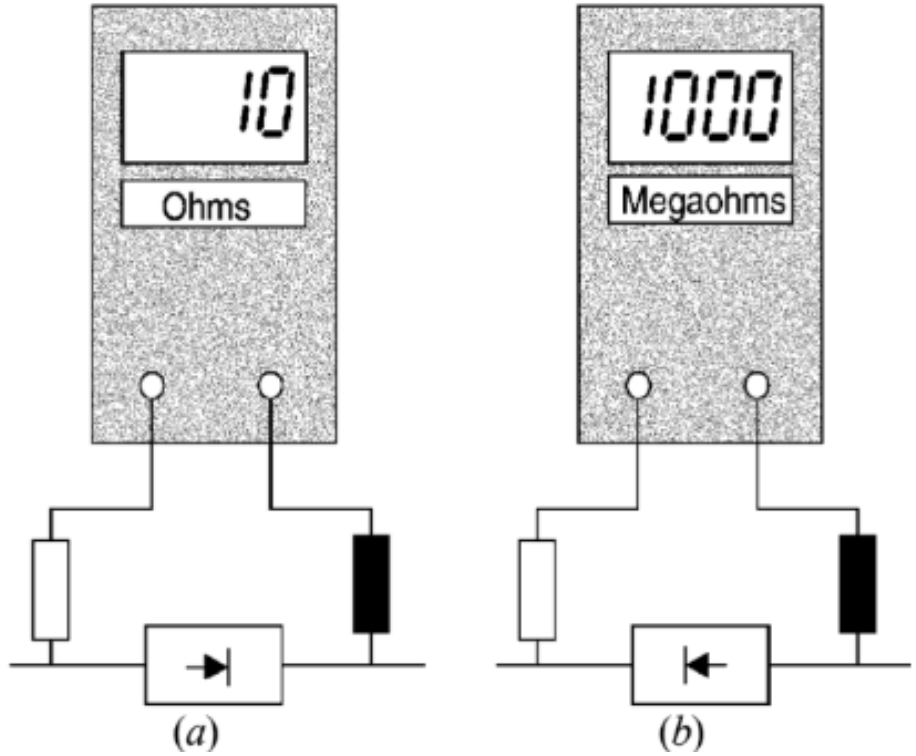
Testing a diode out-of-circuit with a DMM.

When the Diode Is Defective

When a diode has failed open, you get an out-of-range "OL" indication for both the forward-bias and the reverse-bias conditions, as illustrated in Figure (c). If a diode is shorted, the meter reads 0 V in both forward- and reverse-bias tests, as indicated in part (d).

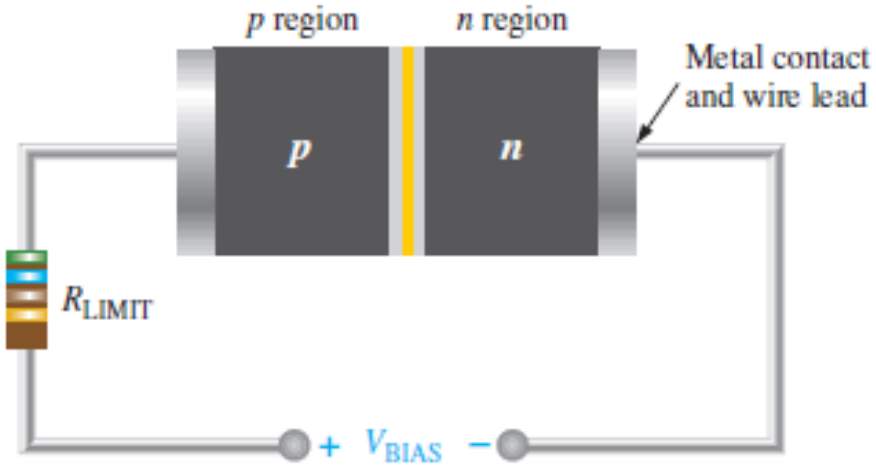
Checking a Diode with the OHMs Function

- Set the function switch on an OHMs range



- For a forward-bias check of a good diode, you will get a resistance reading that can vary depending on the meter's internal battery. Many meters do not have sufficient voltage on the OHMs setting to fully forward-bias a diode and you may get a reading of from several hundred to several thousand ohms
- For the reverse-bias check of a good diode, you will get an out-of-range indication such as "OL" on most DMMs because the reverse resistance is too high for the meter to measure.
- Even though you may not get accurate forward and reverse-resistance readings on a DMM, the relative readings indicate that a diode is functioning properly, and that is usually all you need to know. The out-of-range indication shows that the reverse resistance is extremely high, as you expect
- The reading of a few hundred to a few thousand ohms for forward bias is relatively small compared to the reverse resistance, indicating that the diode is working properly. The actual resistance of a forward-biased diode is typically much less than 100 V.

Forward bias

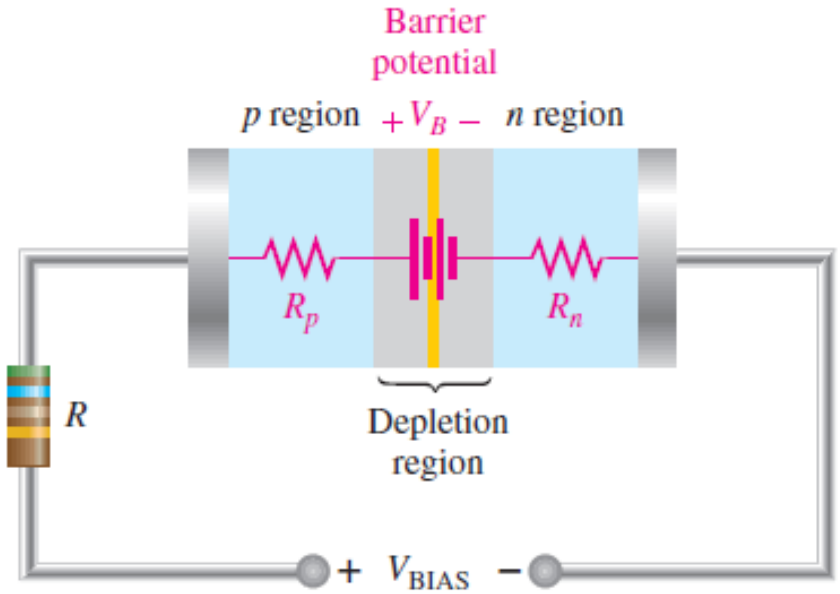


A diode connected for forward bias

Forward bias is the condition that permits current through a diode.

Figure shows a dc voltage connected in a direction to forward-bias the *pn* junction.

Notice that the negative terminal of the source is connected to the *n* region, and the positive terminal is connected to the *p* region

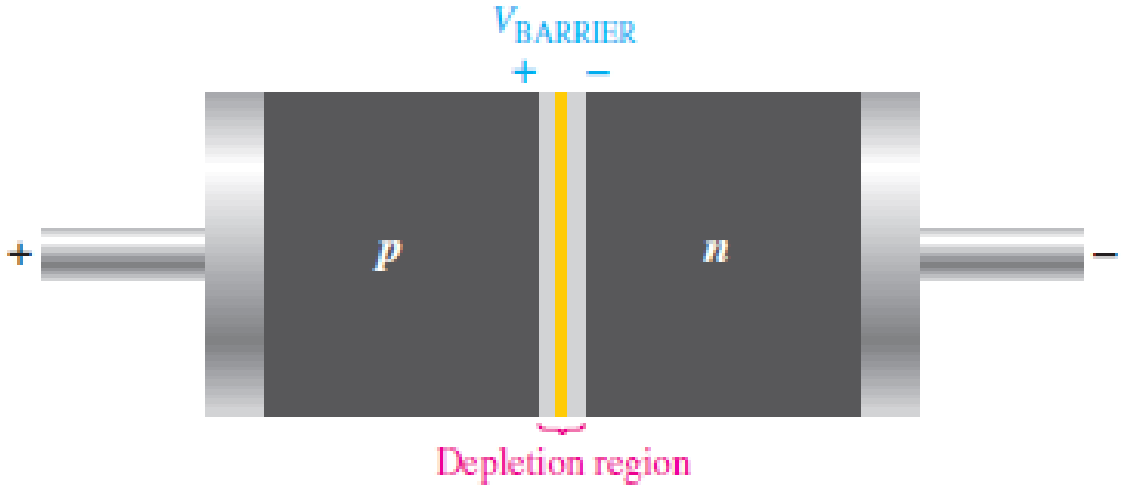


The resistances Rp and Rn represent the dynamic resistances of the p and n materials

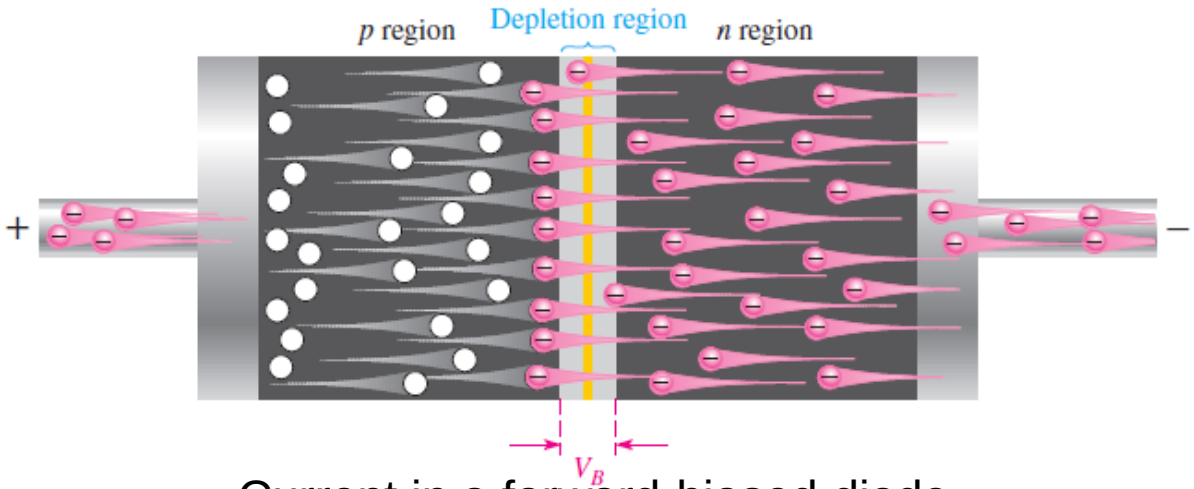
The external bias voltage must overcome the effect of the barrier potential before the diode conducts, as illustrated in Figure.

Conduction occurs at approximately 0.7 V for silicon.

Once the diode is conducting in the forward direction, the voltage drop across it remains at approximately the barrier potential and changes very little with changes in forward current as illustrated in Figure

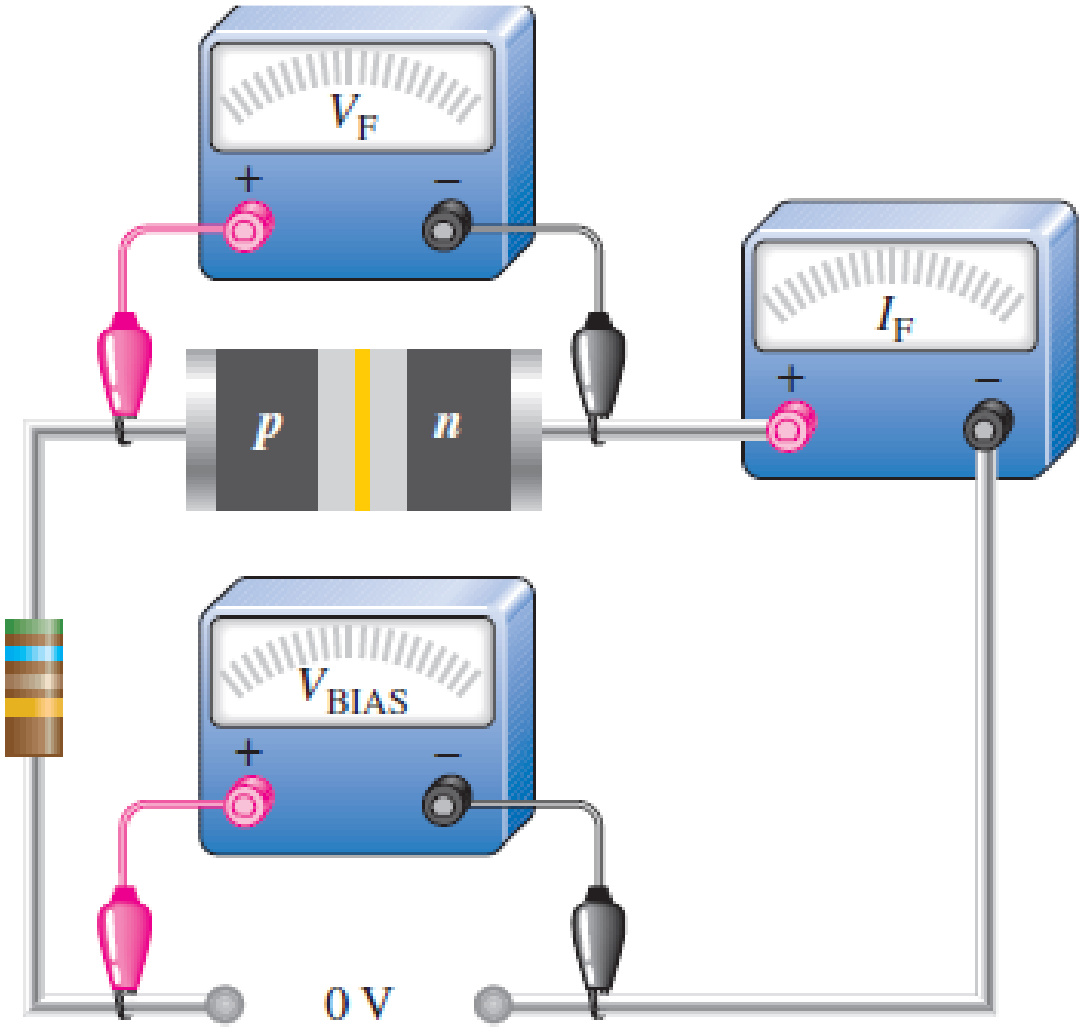


(b) Forward bias narrows the depletion region and produces a voltage drop across the *pn* junction equal to the barrier potential.

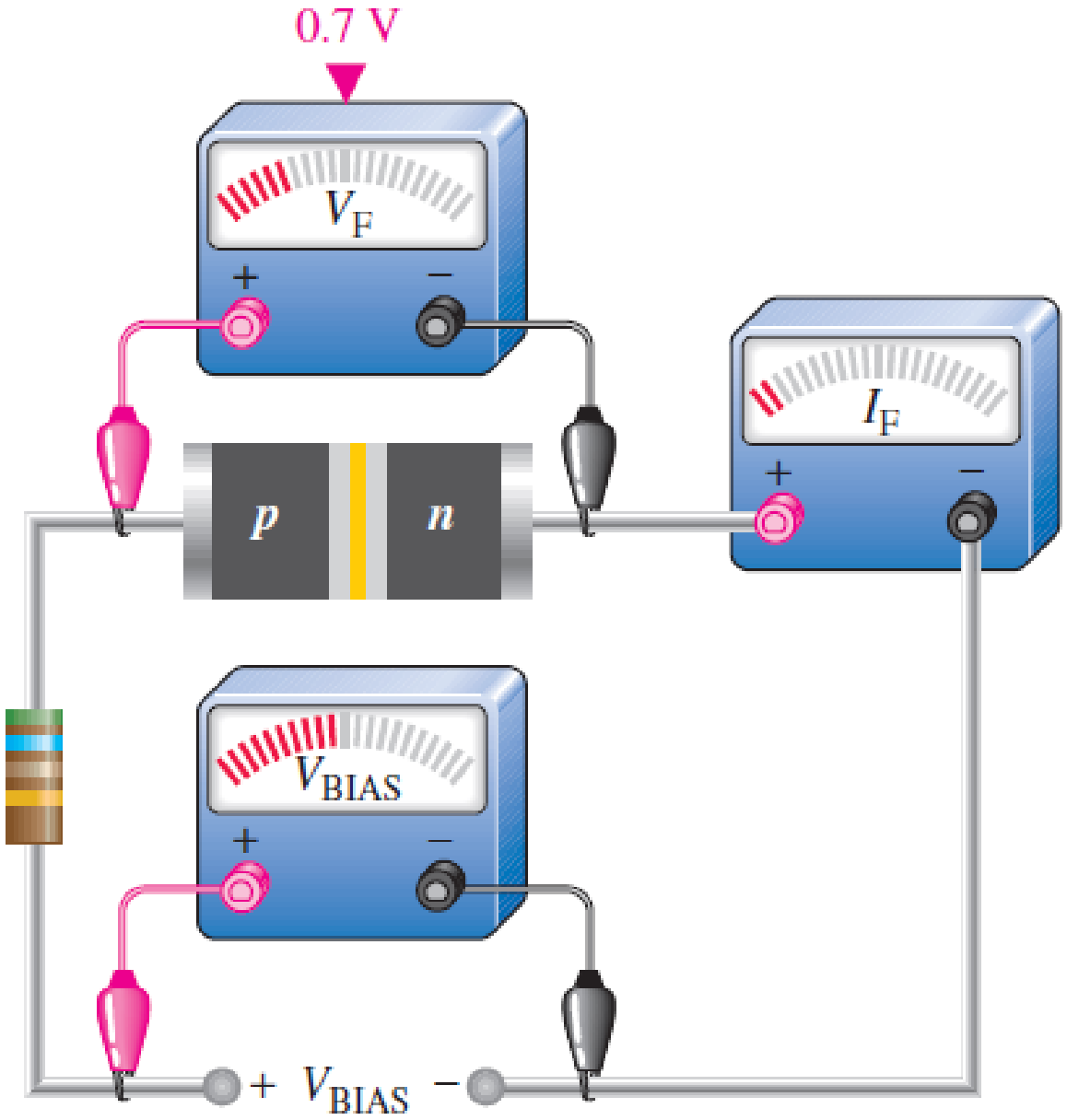


Current in a forward-biased diode

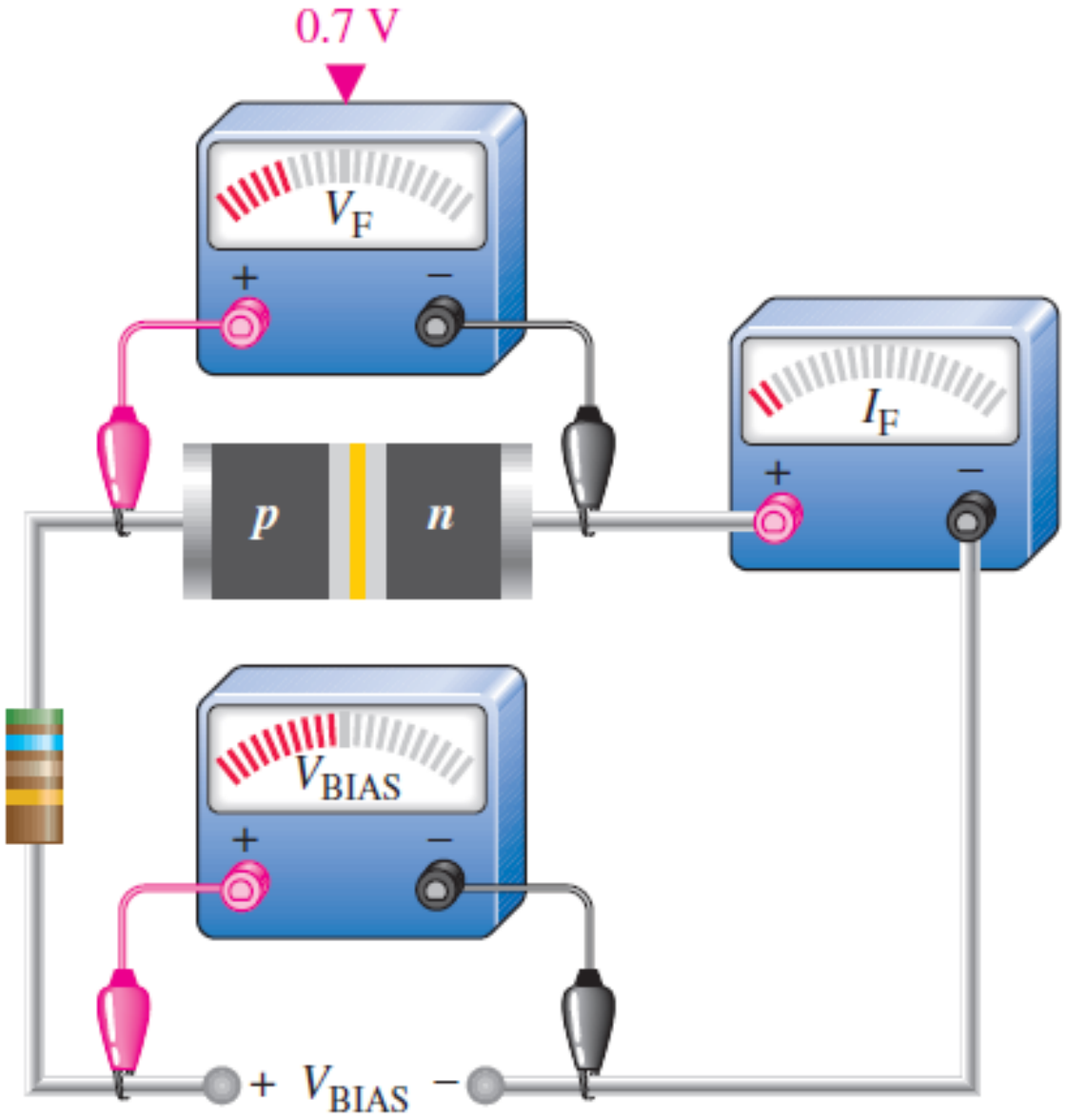
The depletion region narrows and a voltage drop is produced across the *pn* junction when the diode is forward-biased.



(a) No bias voltage. The *pn* junction of the diode is at equilibrium.



(b) Small forward-bias voltage ($V_F < 0.7$ V), very small forward current.



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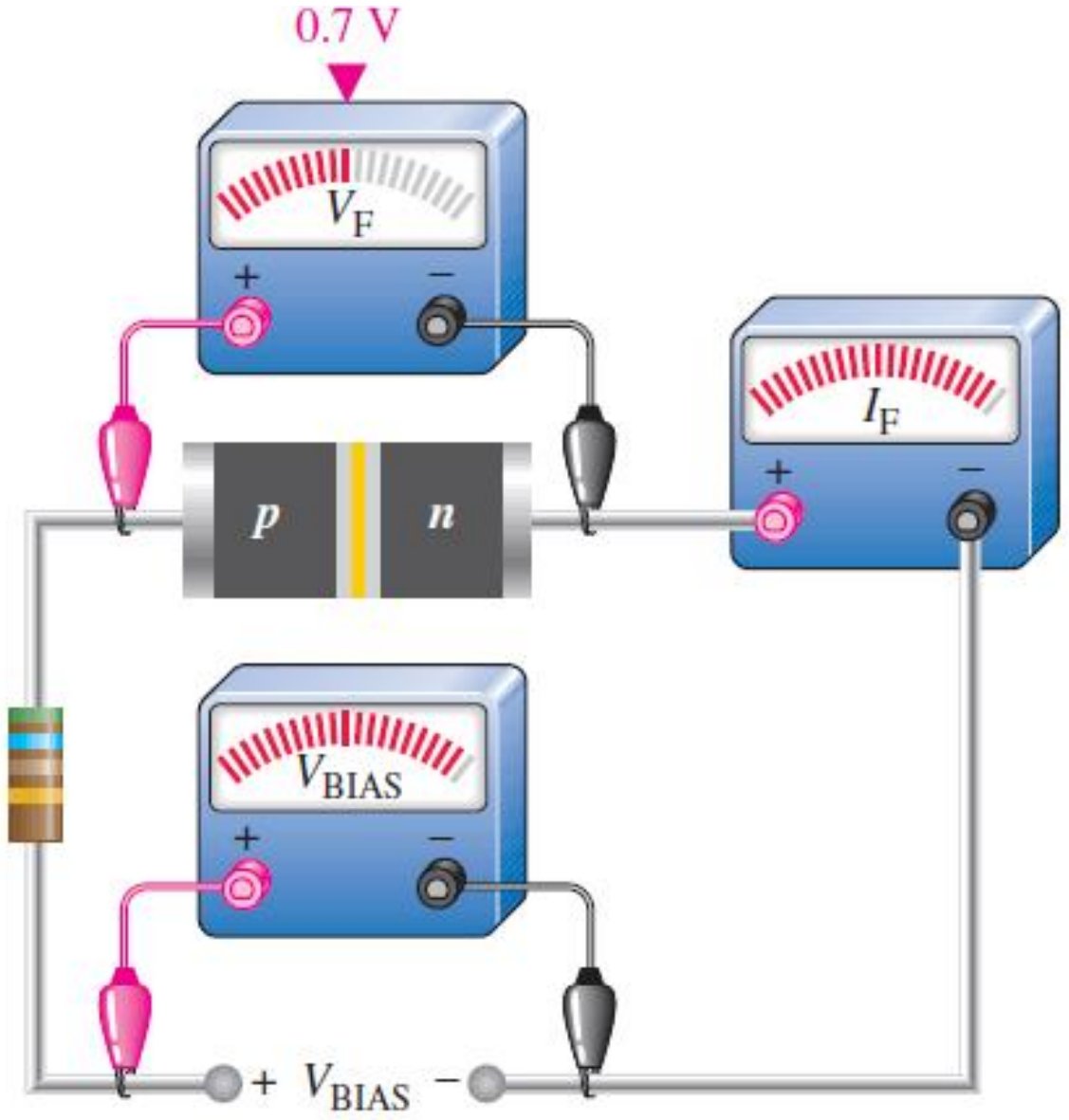
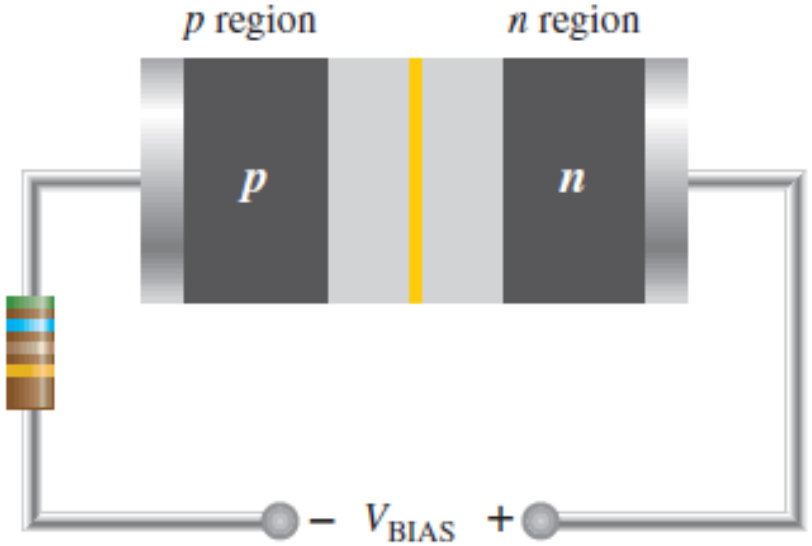


(c) Forward voltage reaches and remains at approximately 0.7 V. Forward current continues to increase as the bias voltage is increased.

Reverse Bias

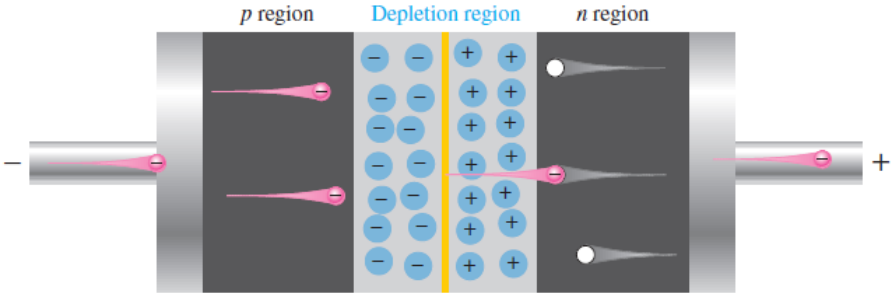


(a) Reverse-bias connection.

Reverse bias is the condition that prevents current through the diode.

Figure (a) shows a dc voltage source connected to reverse-bias the diode. Notice that the negative terminal VBIAS of the source is connected to the *p* region and the positive terminal is connected to the *n* region

When the diode is reverse-biased, the depletion region effectively acts as an insulator between the layers of oppositely charged ions, forming an effective capacitance



however, a very small current produced by minority carriers during reverse bias. This current is typically in the micro Ampere or nana Ampere range. The reverse current is dependent primarily on the junction temperature and not on the amount of reverse-biased voltage. A temperature increase causes an increase in reverse current, ***Reverse Breakdown*** If the external reverse-bias voltage is increased to a large enough value, **reverse breakdown** occurs.

Diode Characteristic Curve

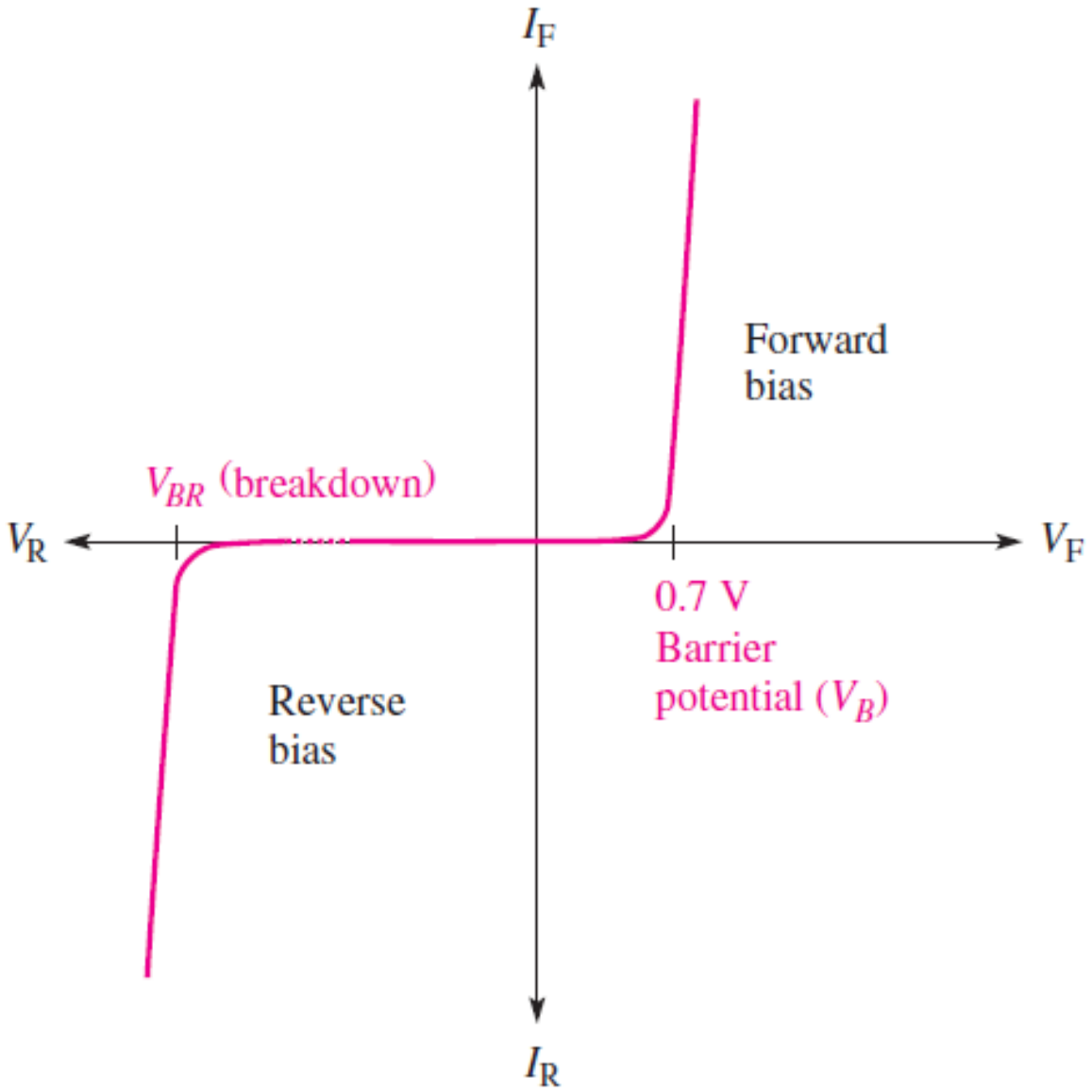
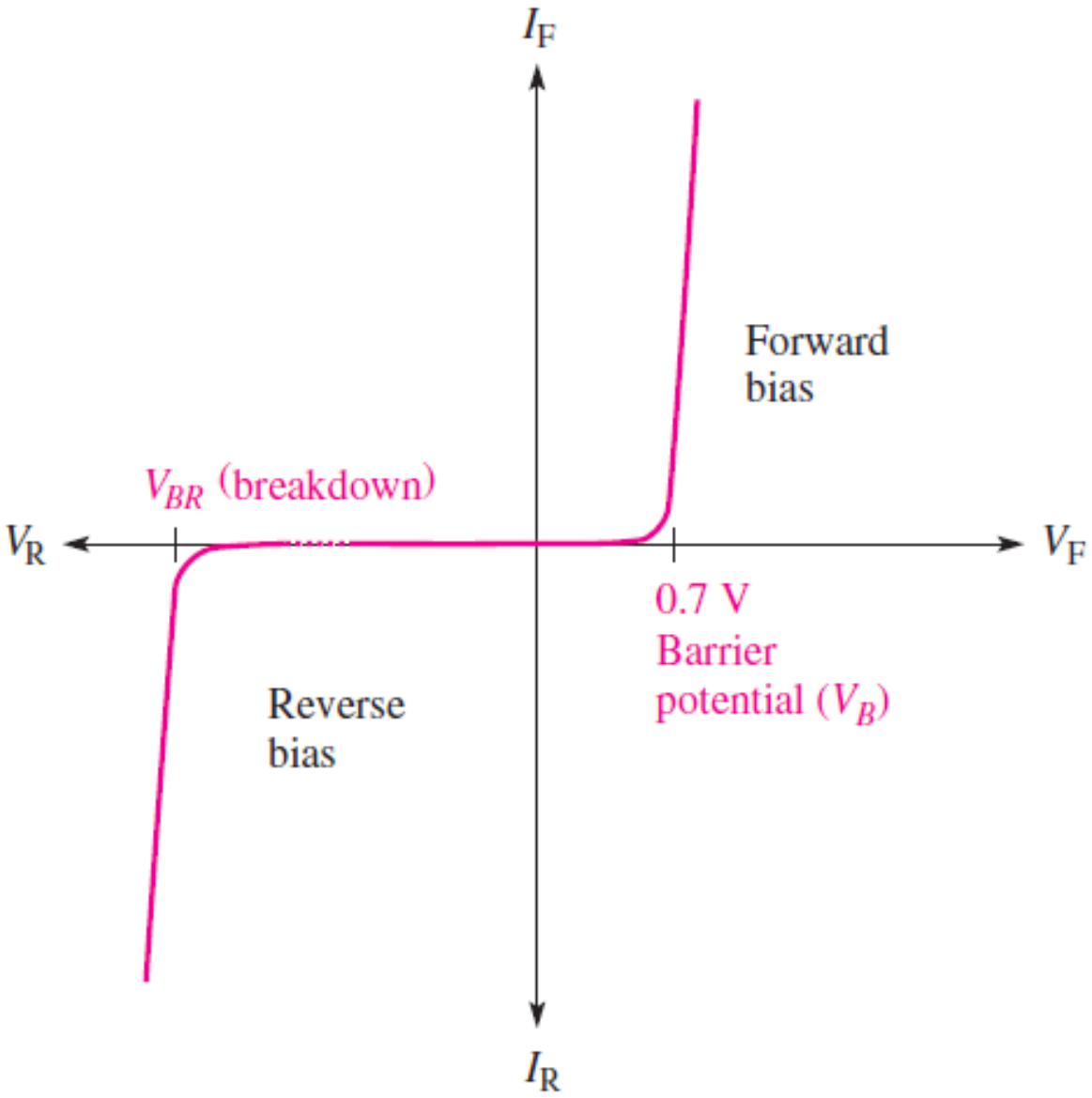


Figure is a graph of diode voltage versus current, known as a V-I characteristic curve.

The upper right quadrant of the graph represents the forward-biased condition. As you can see, there is very little forward current (I_F) for forward voltages (V_F) below the barrier potential.

As the forward voltage approaches the value of the barrier potential, the current begins to increase. Once the forward voltage reaches the barrier potential, the current increases drastically and must be limited by a series resistor. The voltage across the forward-biased diode remains approximately equal to the barrier potential.

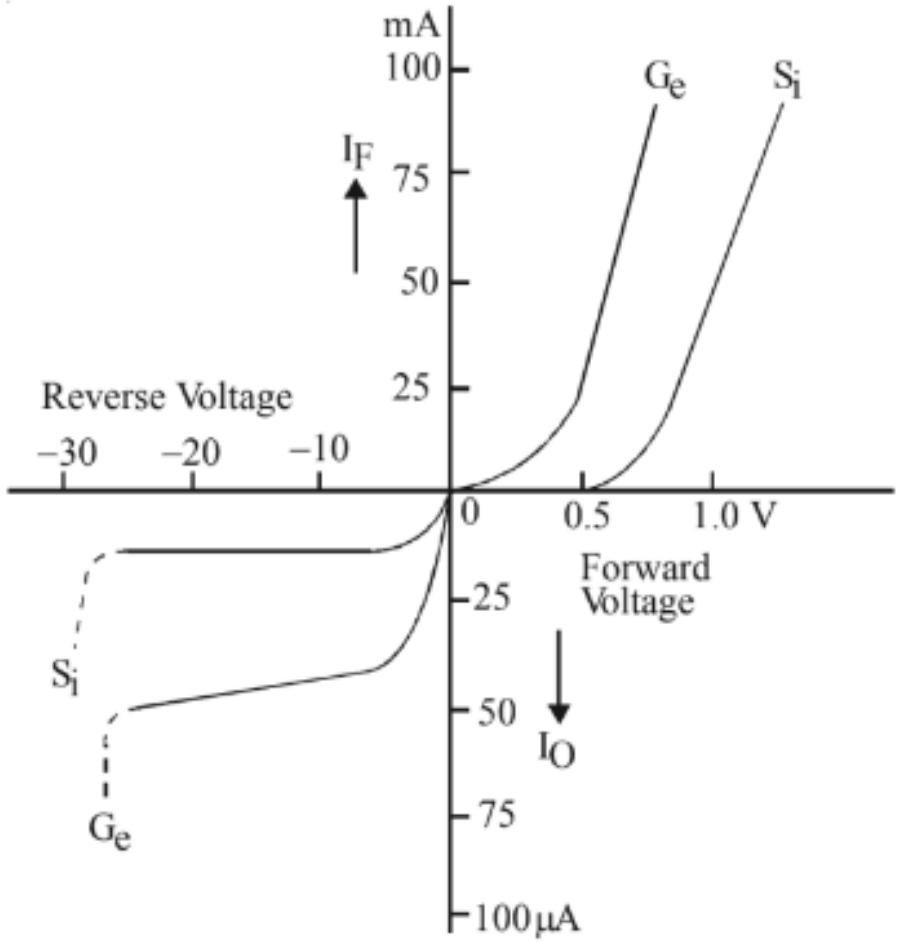
Diode Characteristic Curve

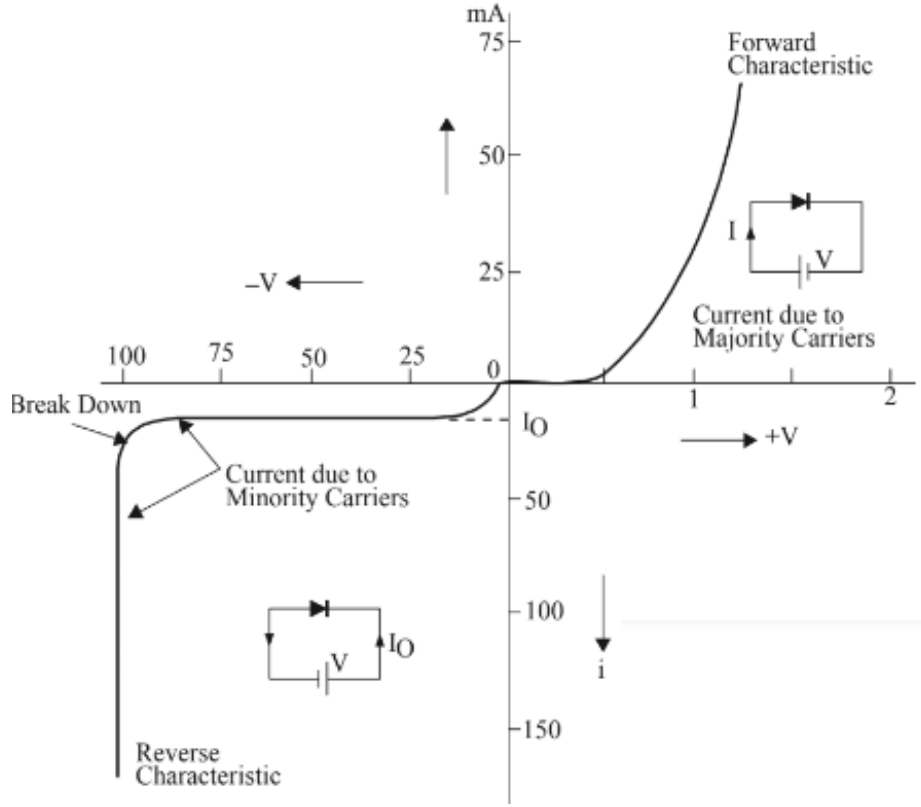


The lower left quadrant of the graph represents the reverse-biased condition.

As the reverse voltage (V_R). increases to the left, the current remains near zero until the breakdown voltage (V_{BR}) is reached. When breakdown occurs, there is a large reverse current which, if not limited, can destroy the diode.

Typically, the breakdown voltage is greater than 50 V for most rectifier diodes. Remember that most diodes should not be operated in reverse breakdown





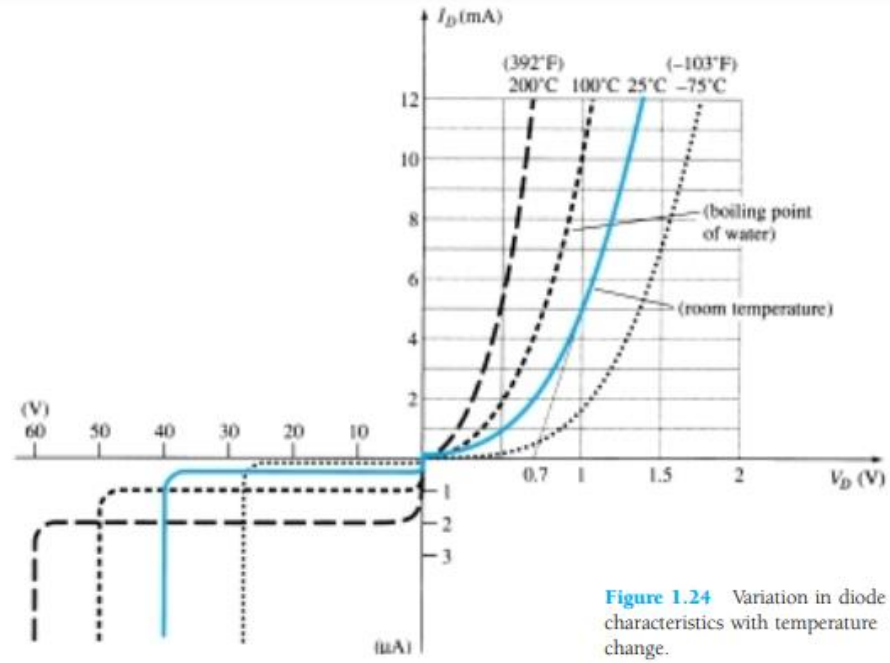
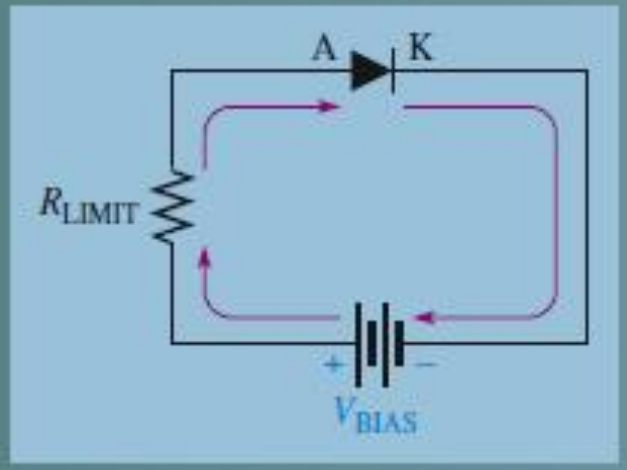


Figure 1.24 Variation in diode characteristics with temperature change.

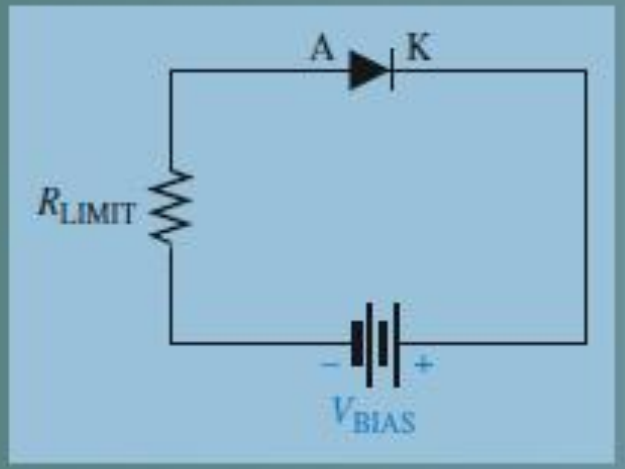
SUMMARY OF DIODE BIAS

FORWARD BIAS: PERMITS MAJORITY-CARRIER CURRENT



- Bias voltage connections: positive to anode (A); negative to cathode (K).
- The bias voltage must be greater than the barrier potential.
- Barrier potential: 0.7 V for silicon.
- Majority carriers provide the forward current.
- The depletion region narrows.

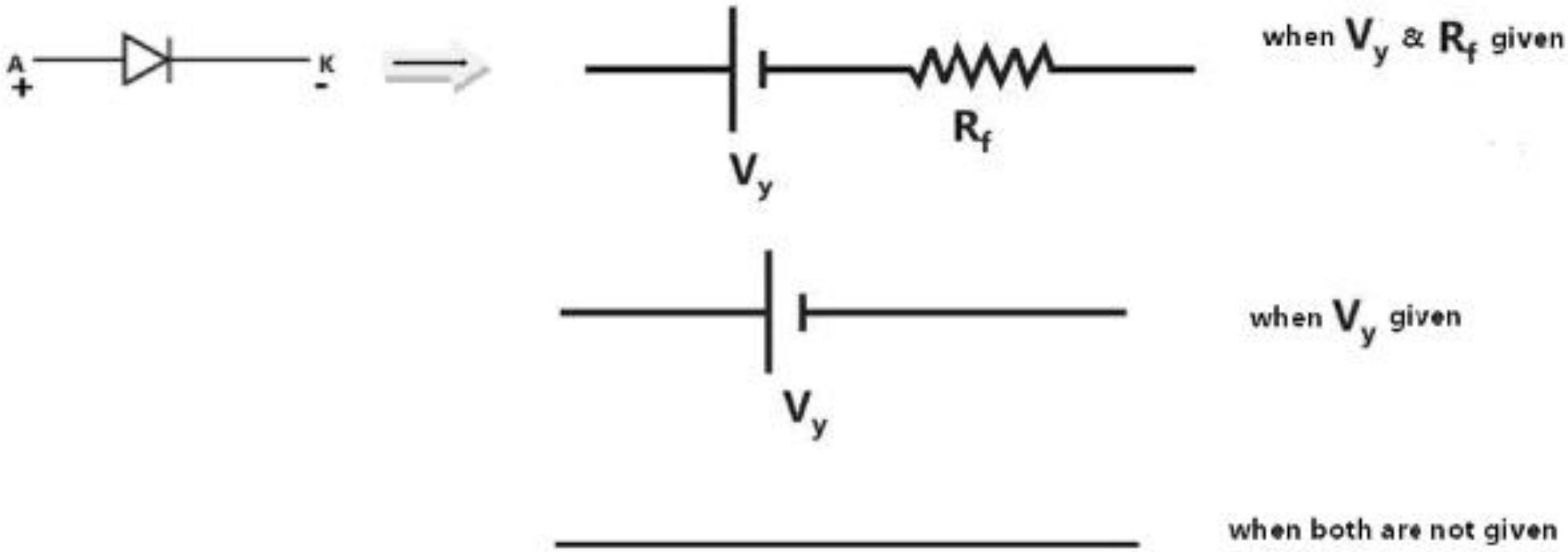
REVERSE BIAS: PREVENTS MAJORITY-CARRIER CURRENT



- Bias voltage connections: positive to cathode (K); negative to anode (A).
- The bias voltage must be less than the breakdown voltage.
- There is no majority carrier current after transition time.
- Minority carriers provide a negligibly small reverse current.
- The depletion region widens.

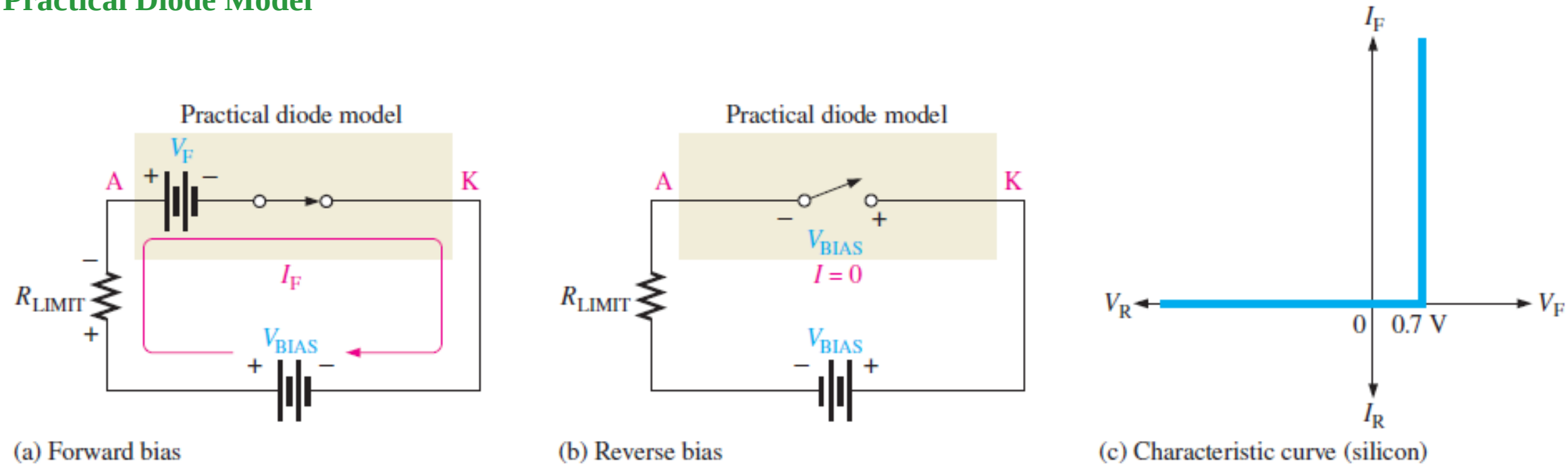
Equivalent circuit of diode

- Forward Bias



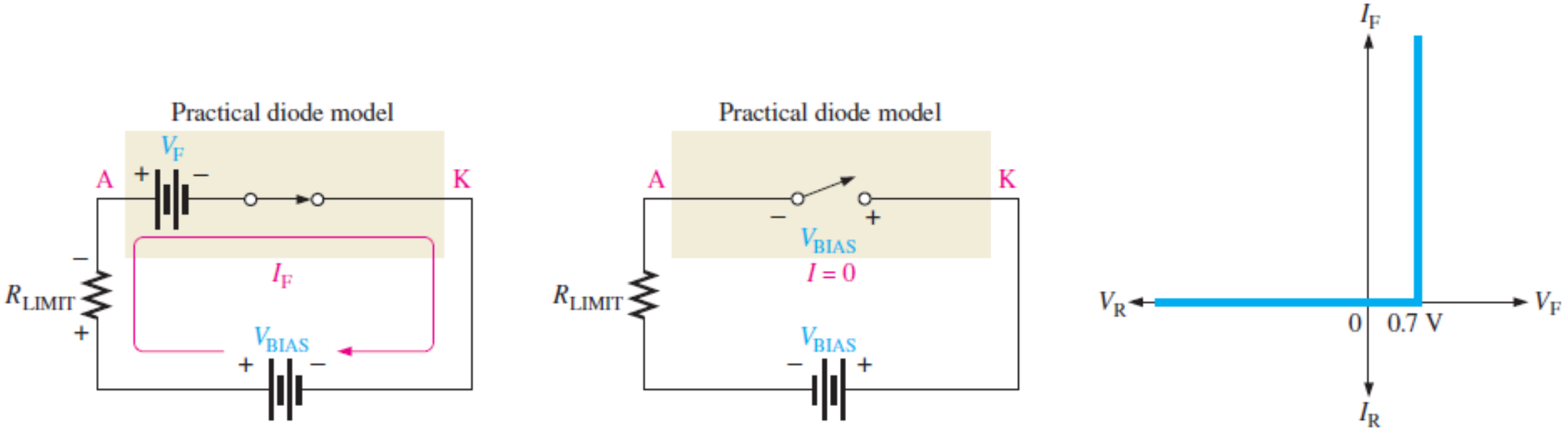
- Reverse Bias

The Practical Diode Model



(a) Forward bias (b) Reverse bias (c) Characteristic curve (silicon)

The practical model includes the barrier potential. When the diode is forward-biased, it is equivalent to a closed switch in series with a small equivalent voltage source (VF) equal to the barrier potential (0.7 V) with the positive side toward the anode, as indicated in Figure(a). This equivalent voltage source represents the barrier potential that must be exceeded by the bias voltage before the diode will conduct and is not an active source of voltage. When conducting, a voltage drop of 0.7 V appears across the diode, When the diode is reverse-biased, it is equivalent to an open switch just as in the ideal model, as shown in Figure (b). The barrier potential does not affect reverse bias, so it is not a factor



(a) Forward bias (b) Reverse bias (c) Characteristic curve (silicon)

The forward current is determined as follows by first applying Kirchhoff's voltage law to Figure (a):

$$V_{BIAS} - V_F - V_{R_{LIMIT}} = 0$$

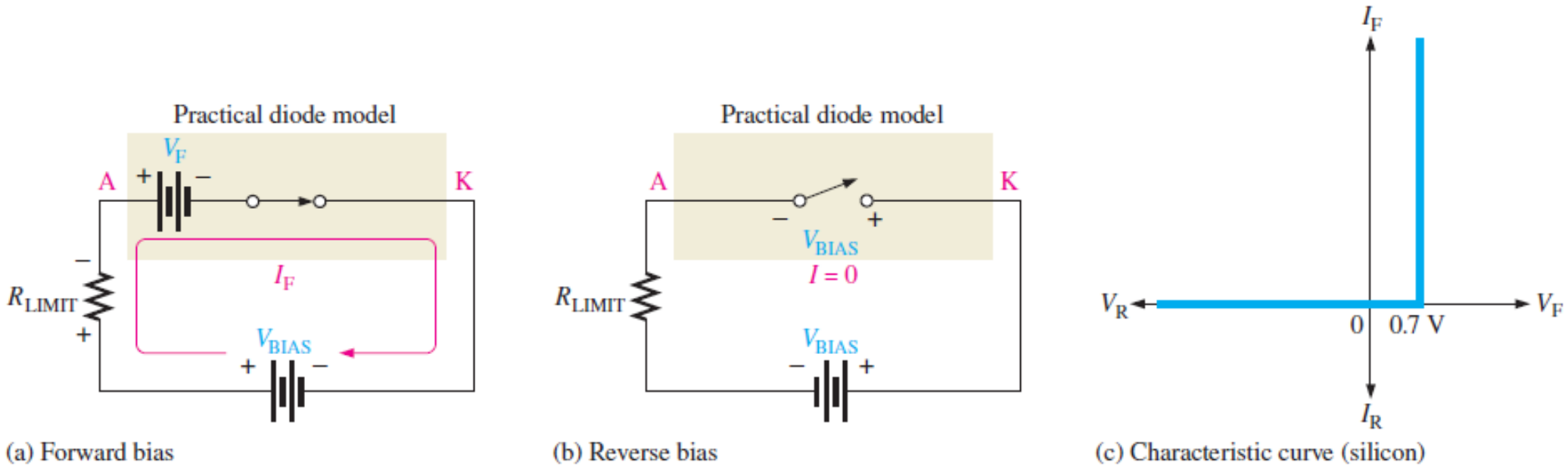
$$V_{R_{LIMIT}} = I_F R_{LIMIT}$$

Substituting and solving for IF $I_F = \dfrac{V_{BIAS} - V_F}{R_{LIMIT}}$

The diode is assumed to have zero reverse current, as indicated by the portion of the curve on the negative horizontal axis

$I_R = 0$ A

$V_R = V_{BIAS}$



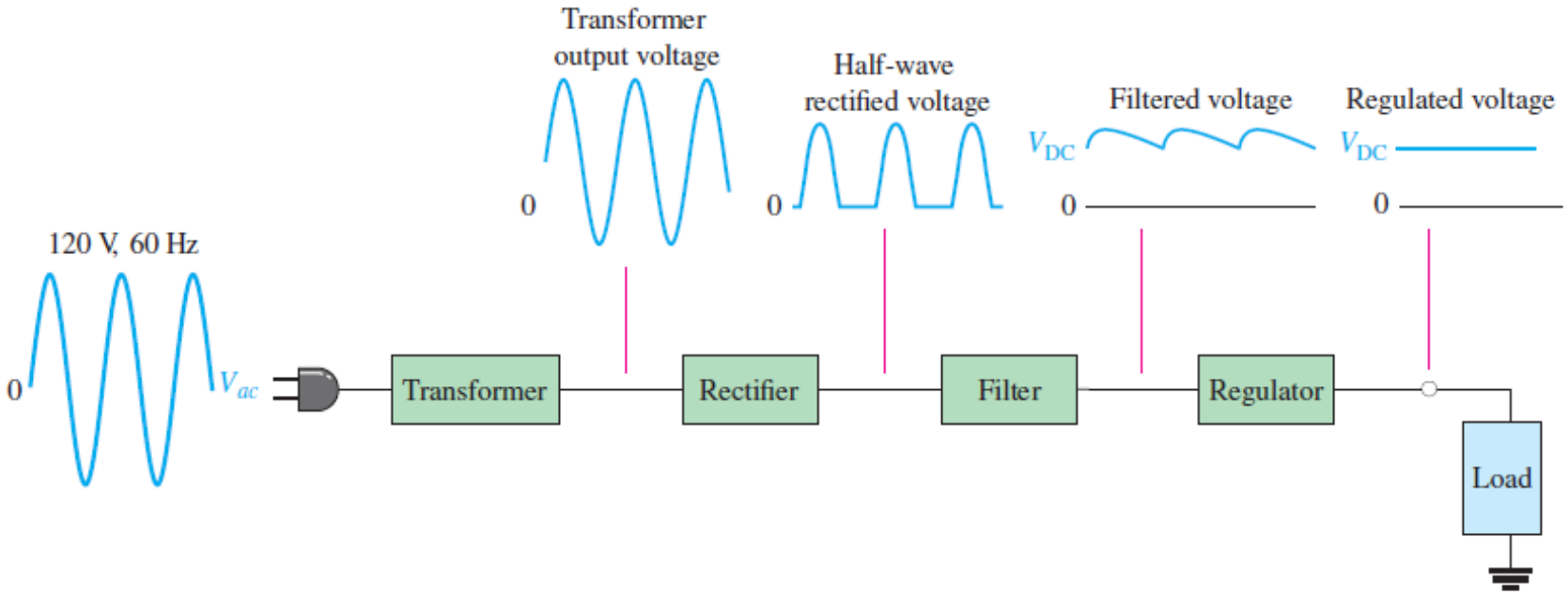
The practical model is useful when you are troubleshooting in lower-voltage circuits. In these cases, the 0.7 V drop across the diode may be significant and should be taken into account. The practical model is also useful when you are designing basic diode circuits.

Rectifier

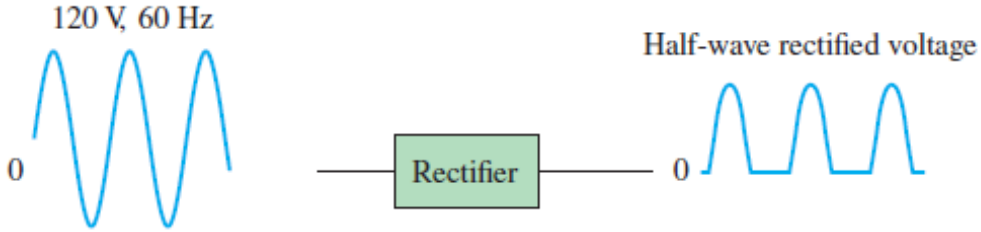
The rectifier can be either a half-wave rectifier or a full-wave rectifier.

The **rectifier** converts the ac input voltage to a pulsating dc voltage, called a half-wave rectified voltage, as shown in (b).

The **filter** eliminates the fluctuations in the rectified voltage and produces a relatively smooth dc voltage

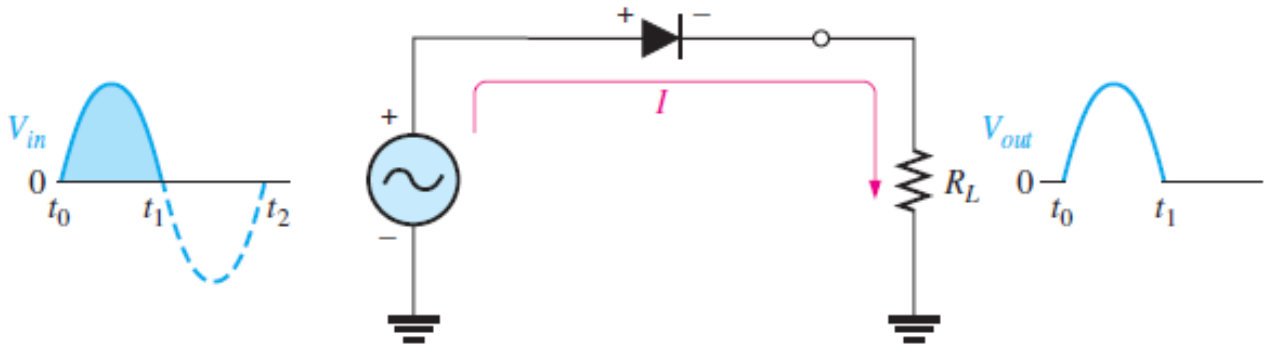


(a) Complete power supply with transformer, rectifier, filter, and regulator

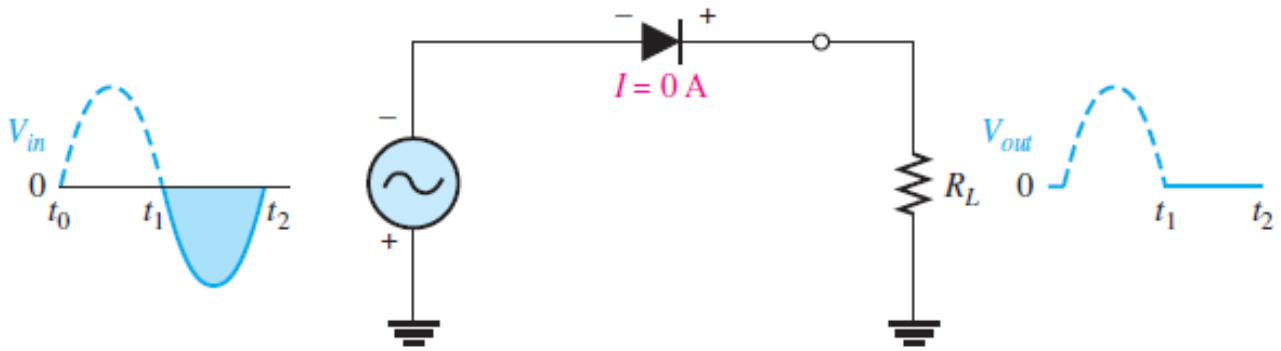


(b) Half-wave rectifier

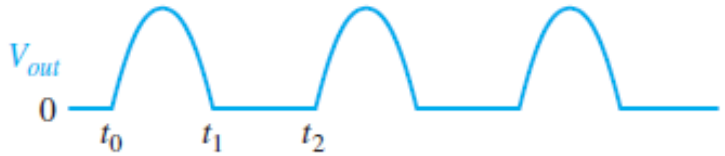
Half-Wave Rectifier Operation



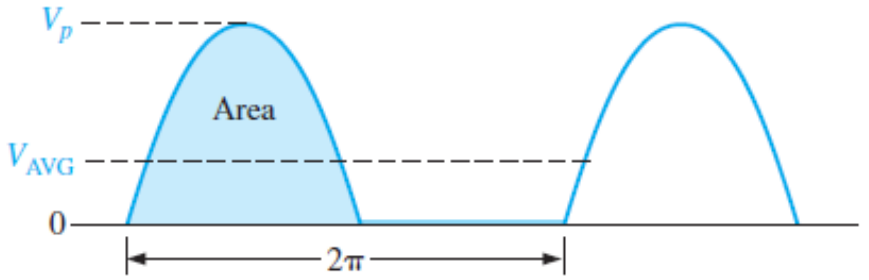
(a) During the positive alternation of the 60 Hz input voltage, the output voltage looks like the positive half of the input voltage. The current path is through ground back to the source.



(b) During the negative alternation of the input voltage, the current is 0, so the output voltage is also 0.



(c) 60 Hz half-wave output voltage for three input cycles



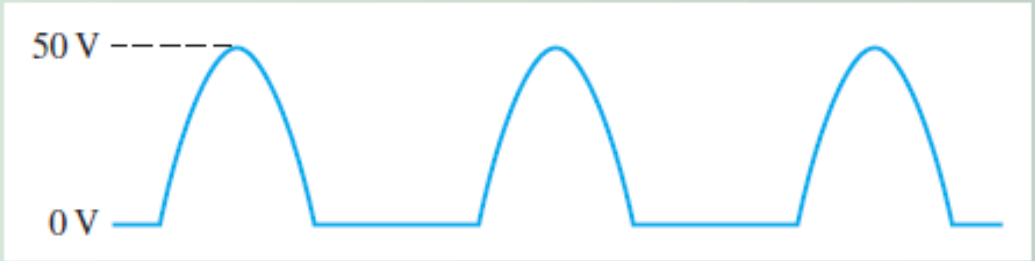
Average Value of the Half-Wave Output Voltage

The average value of the half-wave rectified output voltage is the value you would measure on a dc voltmeter

$$V_{AVG} = \frac{V_p}{\pi}$$

EXAMPLE 2–2 What is the average value of the half-wave rectified voltage in Figure 2–22?

▶ FIGURE 2–22



Solution

$$V_{AVG} = \frac{V_p}{\pi} = \frac{50\text{ V}}{\pi} = \mathbf{15.9\text{ V}}$$

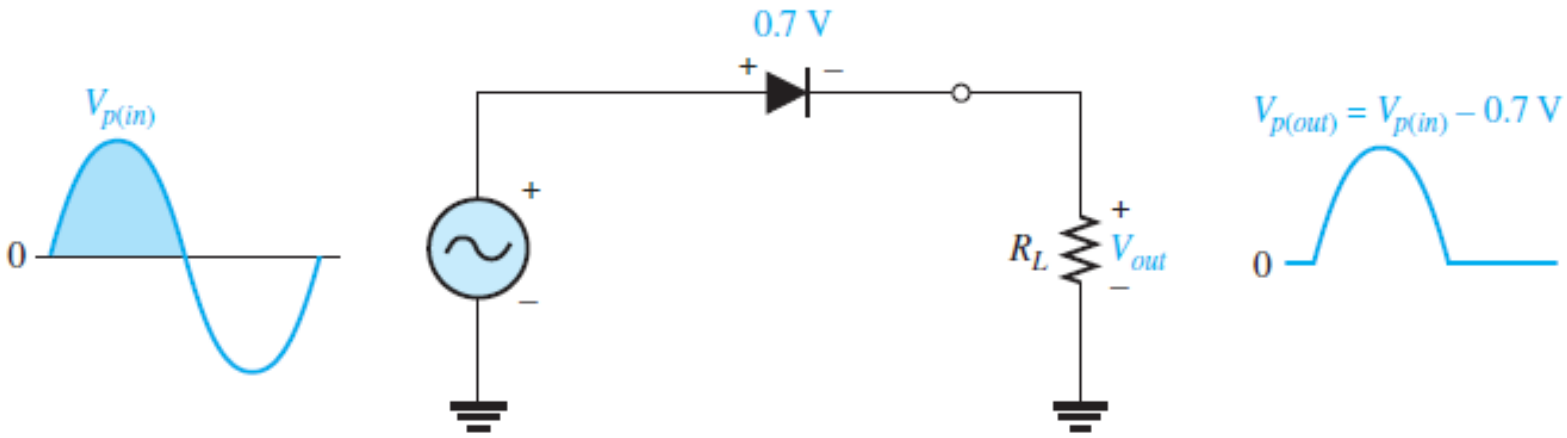
Notice that V_{AVG} is 31.8% of V_p.

Related Problem Determine the average value of the half-wave voltage if its peak amplitude is 12 V.

Effect of the Barrier Potential on the Half-Wave Rectifier Output

In the previous discussion, the diode was considered ideal. When the practical diode model is used with the barrier potential of 0.7 V taken into account, this is what happens. During the positive half-cycle, the input voltage must overcome the barrier potential before the diode becomes forward-biased. This results in a half-wave output with a peak value that is 0.7 V less than the peak value of the input, as shown in Figure

$$V_{p(out)} = V_{p(in)} - 0.7\ \text{V} \qquad \text{Equation 2–4}$$

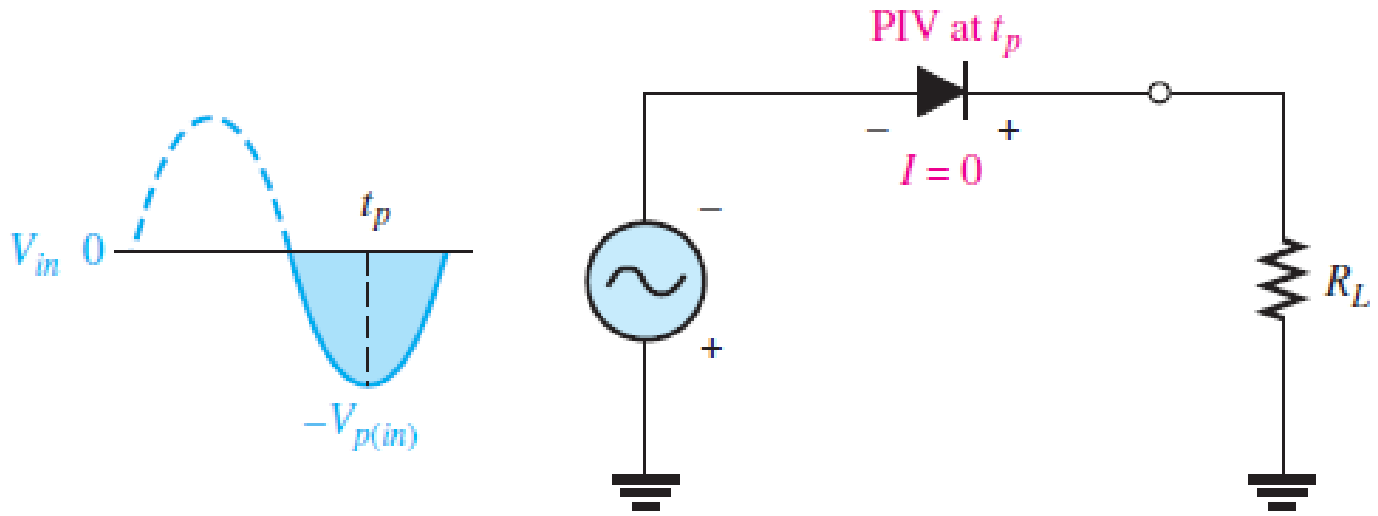


▲ FIGURE 2–23

The effect of the barrier potential on the half-wave rectified output voltage is to reduce the peak value of the input by about 0.7 V.

Peak Inverse Voltage (PIV)

The **peak inverse voltage (PIV)** equals the peak value of the input voltage, and the diode must be capable of withstanding at least this amount of repetitive reverse voltage. For the diode in Figure 2–26, the maximum value of reverse voltage, designated as PIV, occurs at the peak of each negative alternation of the input voltage when the diode is reverse-biased. A diode should be rated at least 20% higher than the PIV.



PIV = $V_{P(in)}$

▲ FIGURE 2–26

The PIV occurs at the peak of each half-cycle of the input voltage when the diode is reverse-biased. In this circuit, the PIV occurs at the peak of each negative half-cycle.

HALF-WAVE RECTIFICATION

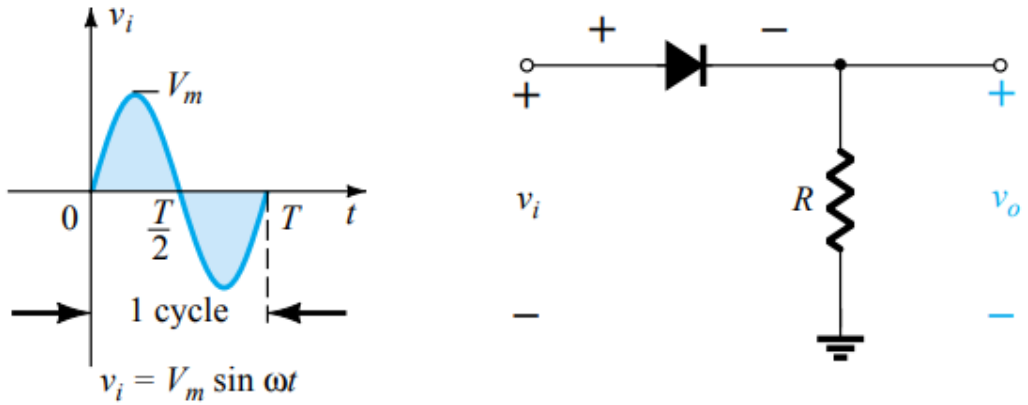


Figure 2.43 Half-wave rectifier.

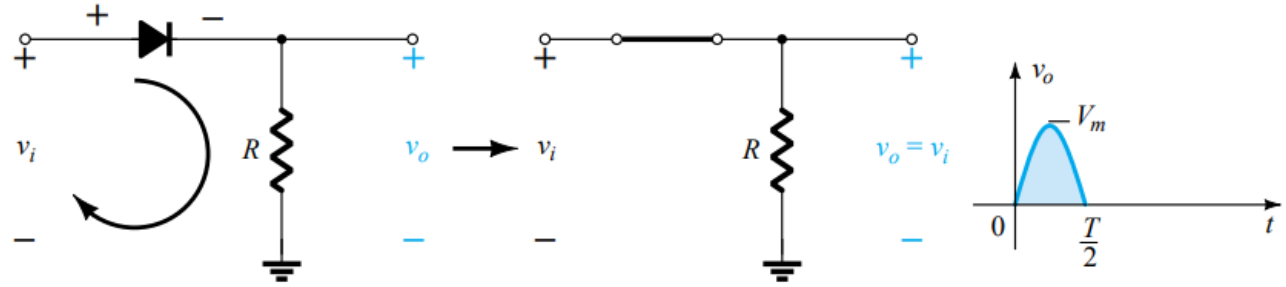
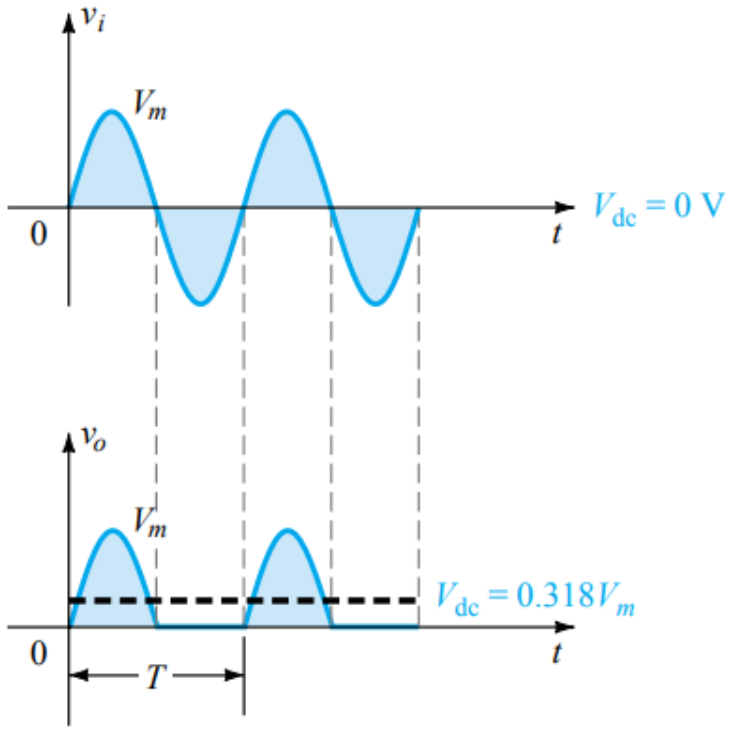


Figure 2.44 Conduction region ($0 \rightarrow T/2$).



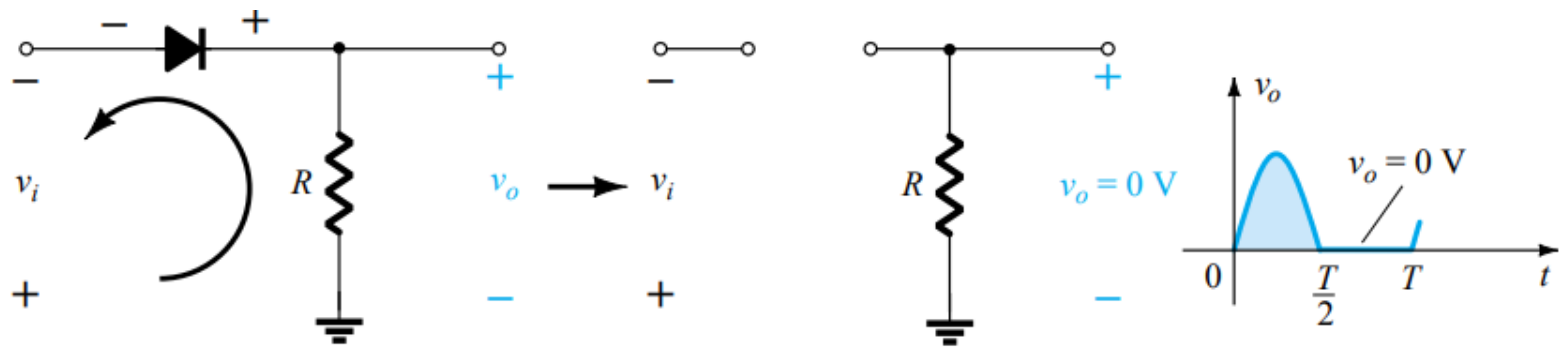
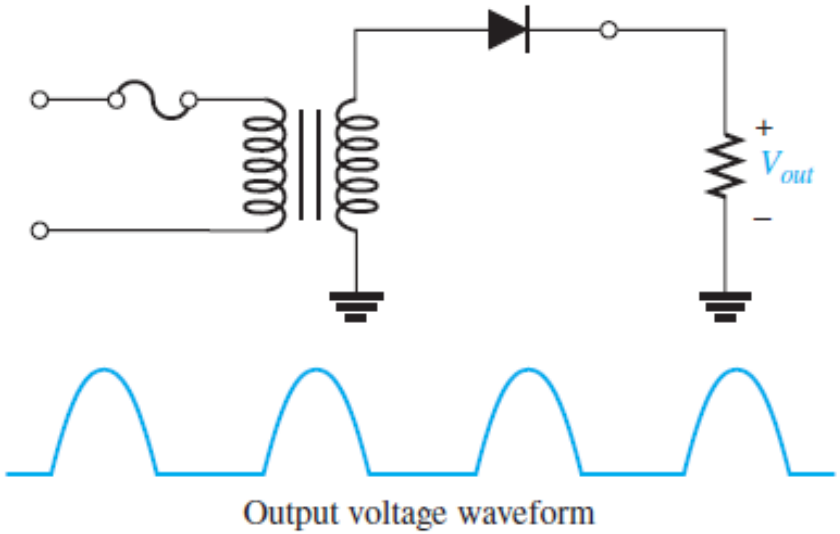


Figure 2.45 Nonconduction region ($T/2 \rightarrow T$).

HALF-WAVE RECTIFICATION



Output voltage waveform

- Peak value of output:

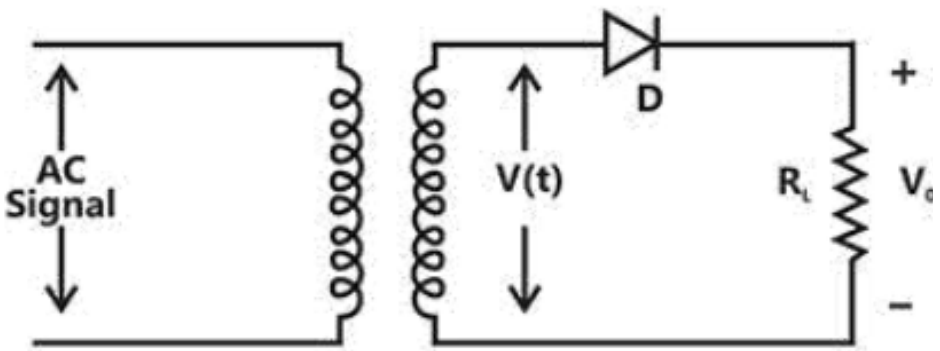
$$V_{p(out)} = V_{p(sec)} - 0.7\ \text{V}$$

- Average value of output:

$$V_{AVG} = \frac{V_{p(out)}}{\pi}$$

- Diode peak inverse voltage:

$$\text{PIV} = V_{p(sec)}$$



<u>During positive half wave cycle</u>

$$V_0 = V_m \sin\omega t \left[\frac{R_L}{R_f + R_L}\right]$$

R_f = diode resistance

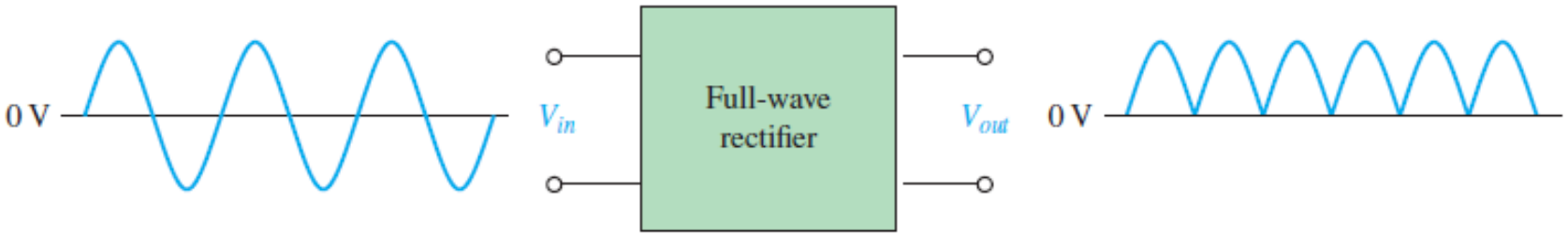
<u>During negative half cycle</u>

$V_0 = 0$

- $(V_0)_{avg} = \frac{V_m}{\pi}$
- $\eta = \frac{4}{\pi^2}\left(\frac{R_L}{R_f + R_L}\right) \times 100\%$
- $(V_0)_{RMS} = \frac{V_m}{2}$
- Form Factor = $\frac{V_{RMS}}{V_{avg}} = \pi/2$
- Ripple factor = $\sqrt{FF^2 - 1}$
- PIV = V_m

Full-wave rectifier

A **full-wave rectifier** allows unidirectional (one-way) current through the load during the entire 360deg. of the input cycle, whereas a half-wave rectifier allows current through the load only during one-half of the cycle. The result of full-wave rectification is an output voltage with a frequency twice the input frequency and that pulsates every half-cycle of the input, as shown in Figure



▲ FIGURE 2–29

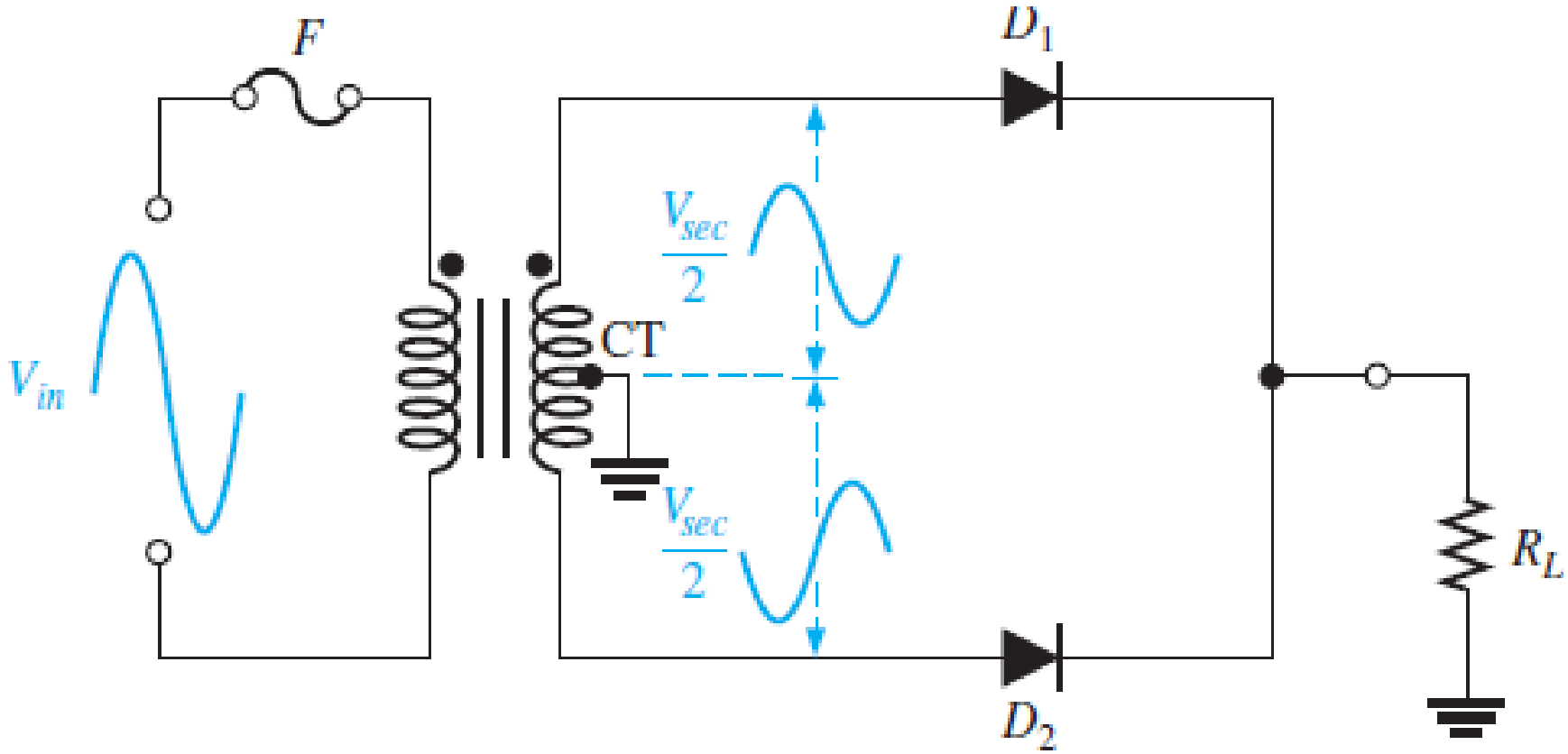
Full-wave rectification.

$$V_{AVG} = \frac{2V_p}{\pi}$$

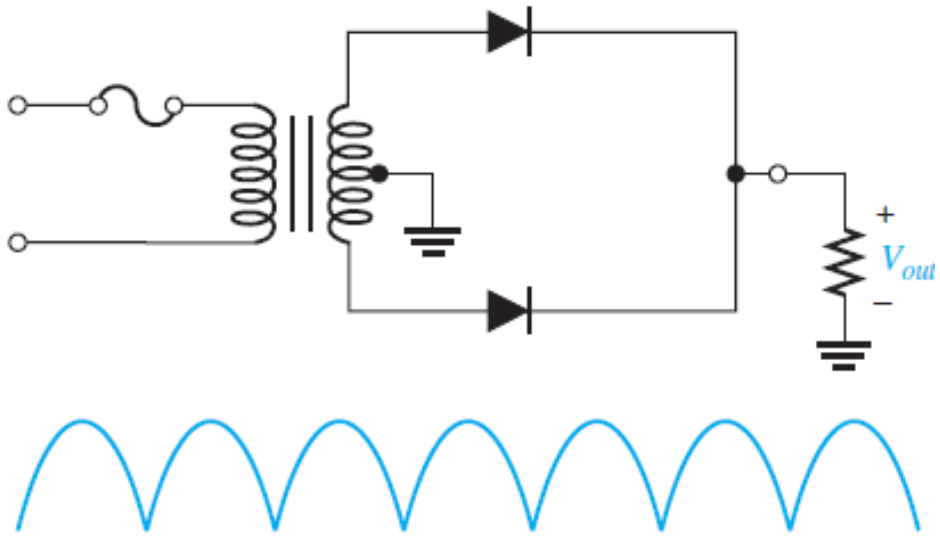
V_{AVG} is approximately 63.7% of V_p for a full-wave rectified voltage.

Center-Tapped Rectifier

A **center-tapped rectifier** is a type of full-wave rectifier that uses two diodes connected to the secondary of a center-tapped transformer



Center-Tapped Rectifier



Output voltage waveform

- Peak value of output:

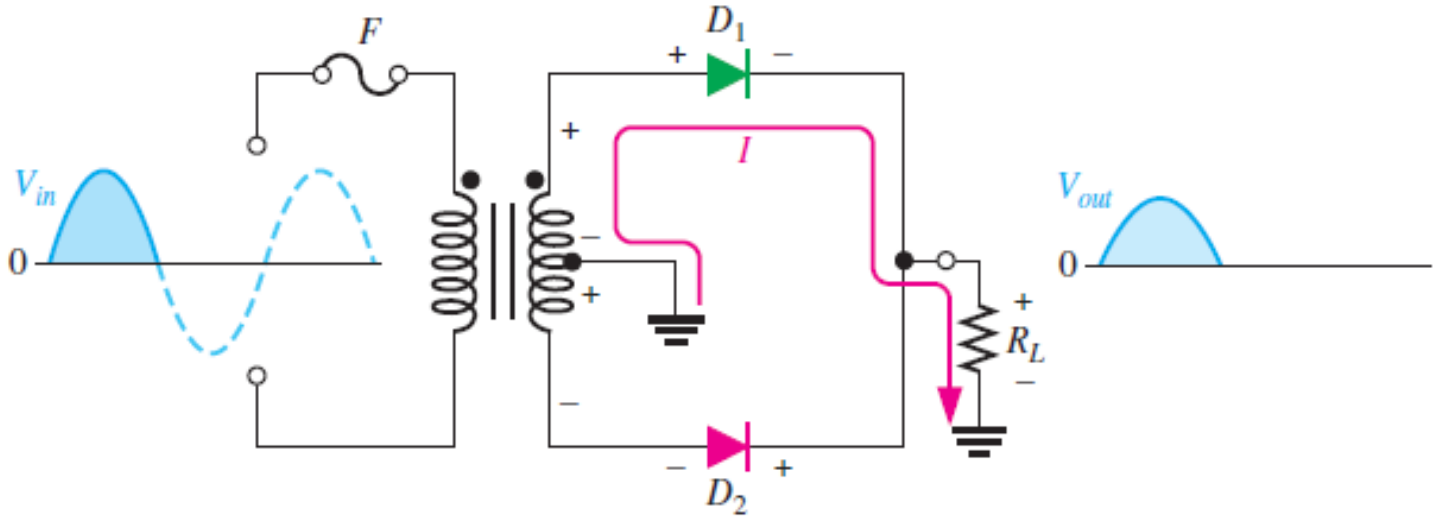
$$V_{p(out)} = \frac{V_{p(sec)}}{2} - 0.7\ \text{V}$$

- Average value of output:

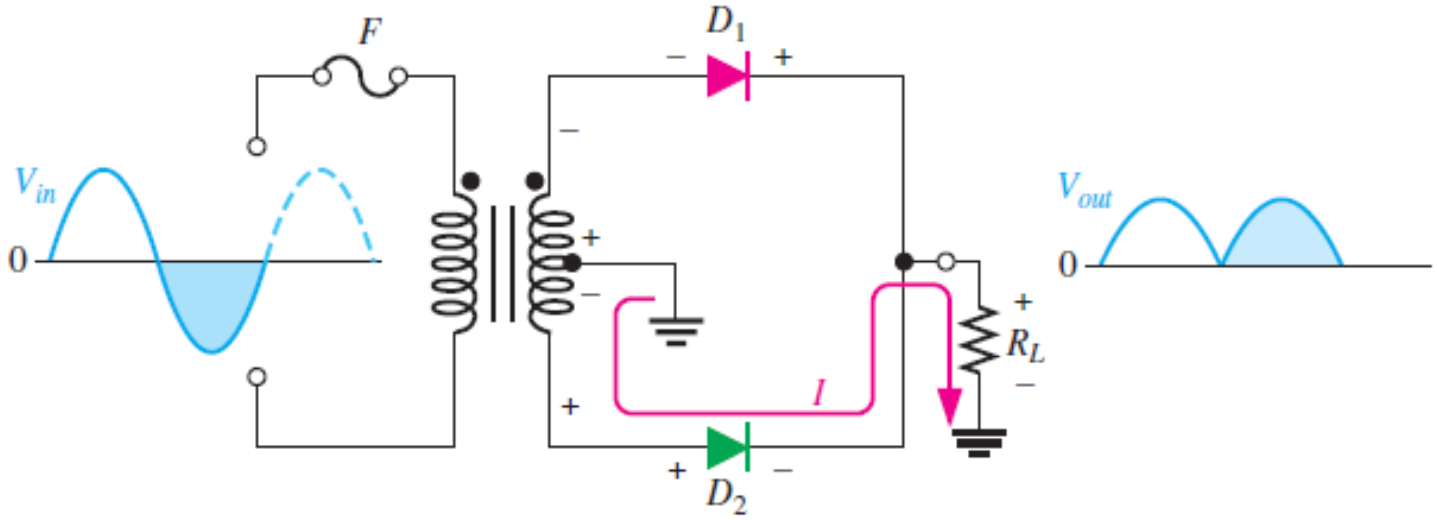
$$V_{AVG} = \frac{2V_{p(out)}}{\pi}$$

- Diode peak inverse voltage:

$$\text{PIV} = 2V_{p(out)} + 0.7\ \text{V}$$

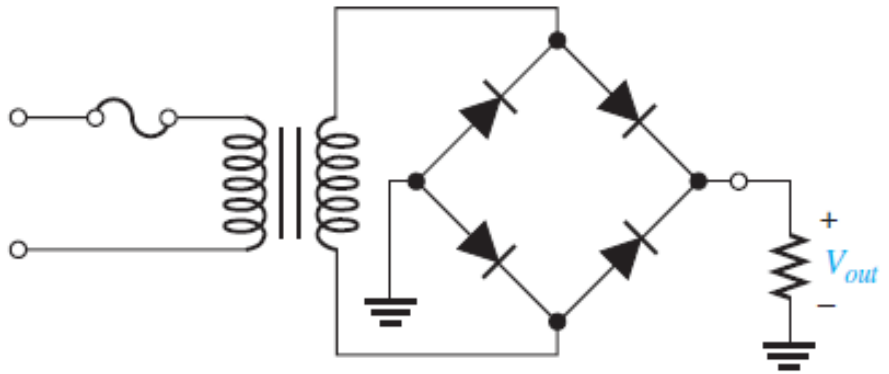


(a) During positive half-cycles, D_1 is forward-biased and D_2 is reverse-biased.



(b) During negative half-cycles, D_2 is forward-biased and D_1 is reverse-biased.

FULL-WAVE BRIDGE RECTIFICATION



Output voltage waveform

- Peak value of output:

$$V_{p(out)} = V_{p(sec)} - 1.4\ \text{V}$$

- Average value of output:

$$V_{AVG} = \frac{2V_{p(out)}}{\pi}$$

- Diode peak inverse voltage:

$$\text{PIV} = V_{p(out)} + 0.7\ \text{V}$$

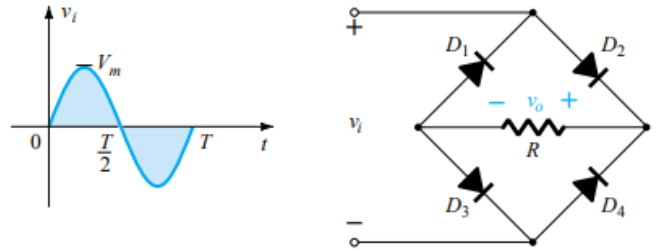


Figure 2.52 Full-wave bridge rectifier.

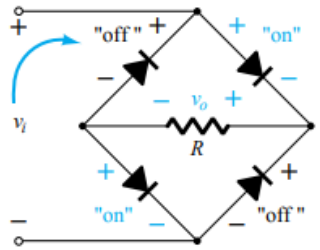


Figure 2.53 Network of Fig. 2.52 for the period $0 \rightarrow T/2$ of the input voltage v_i.

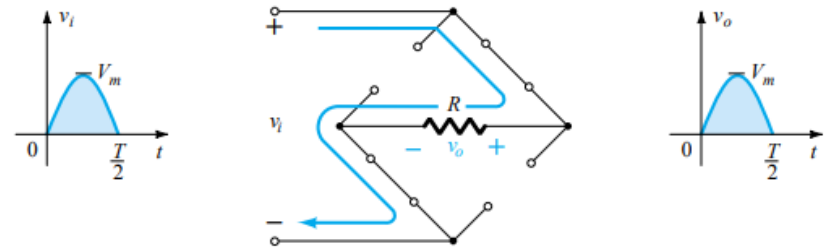


Figure 2.54 Conduction path for the positive region of v_i.

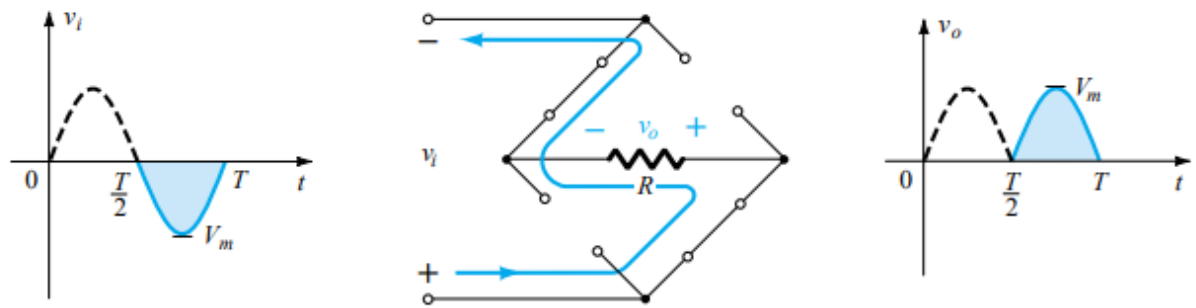


Figure 2.55 Conduction path for the negative region of v_i.

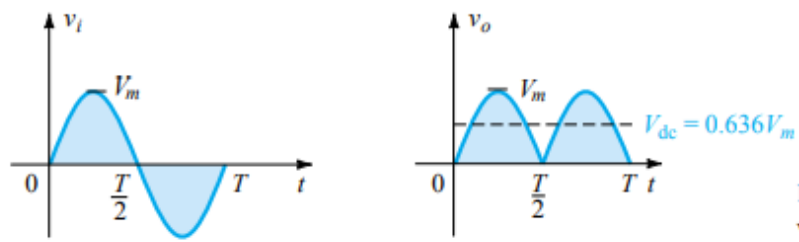
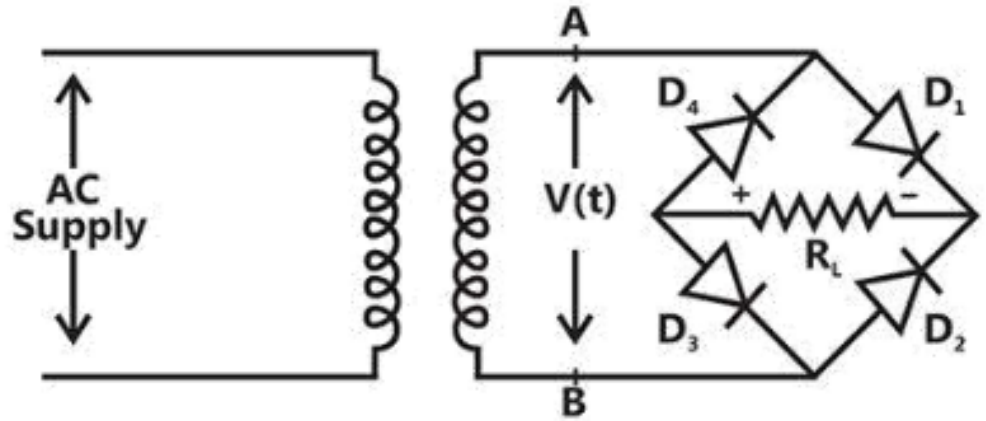


Figure 2.56 Input and output waveforms for a full-wave rectifier.

Bridge full wave rectifier



When +ve half wave cycle

$$V_o = V(t) \times \frac{R_L}{R_L + 2R_f}$$

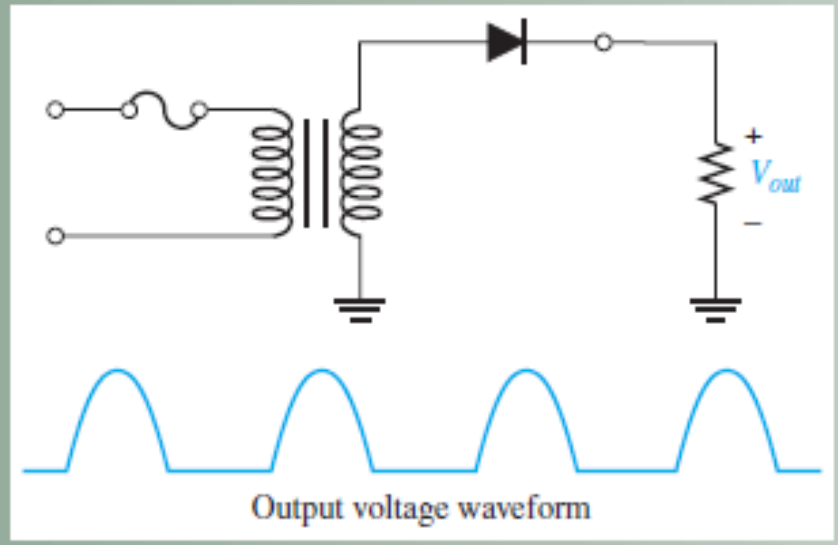
When –ve half wave cycle

$$V_o = -V(t) \times \frac{R_L}{R_L + 2R_f}$$

- $\left(V_o\right)_{avg} = \frac{2V_m}{\pi}$
- $\eta = \frac{8}{\pi^2}\left(\frac{1}{1+2\frac{R_f}{R_L}}\right) \times 100\%$
- $\left(V_o\right)_{RMS} = \frac{V_m}{\sqrt{2}}$
- $FF = \frac{\pi}{2\sqrt{2}}$
- $PIV = V_m$

SUMMARY OF POWER SUPPLY RECTIFIERS

HALF-WAVE RECTIFIER



Output voltage waveform

- Peak value of output:

$$V_{p(out)} = V_{p(sec)} - 0.7\ \text{V}$$

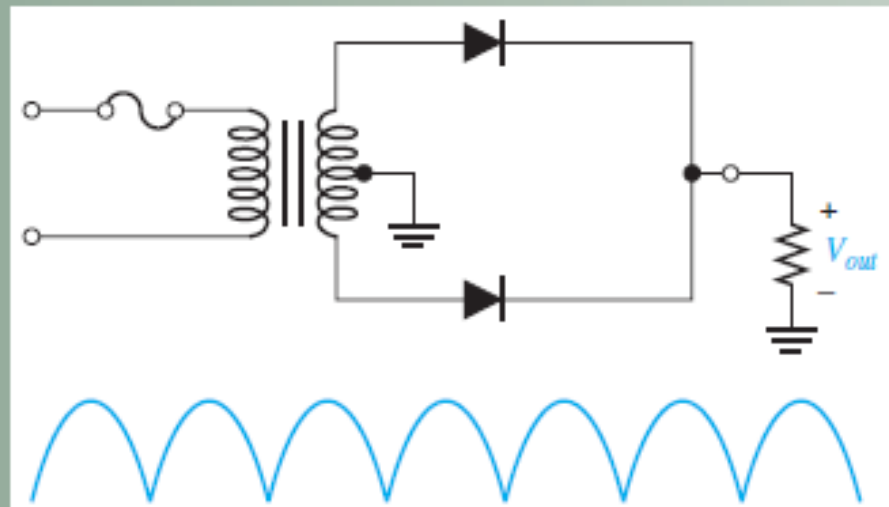
- Average value of output:

$$V_{AVG} = \frac{V_{p(out)}}{\pi}$$

- Diode peak inverse voltage:

$$\text{PIV} = V_{p(sec)}$$

CENTER-TAPPED FULL-WAVE RECTIFIER



Output voltage waveform

- Peak value of output:

$$V_{p(out)} = \frac{V_{p(sec)}}{2} - 0.7\ \text{V}$$

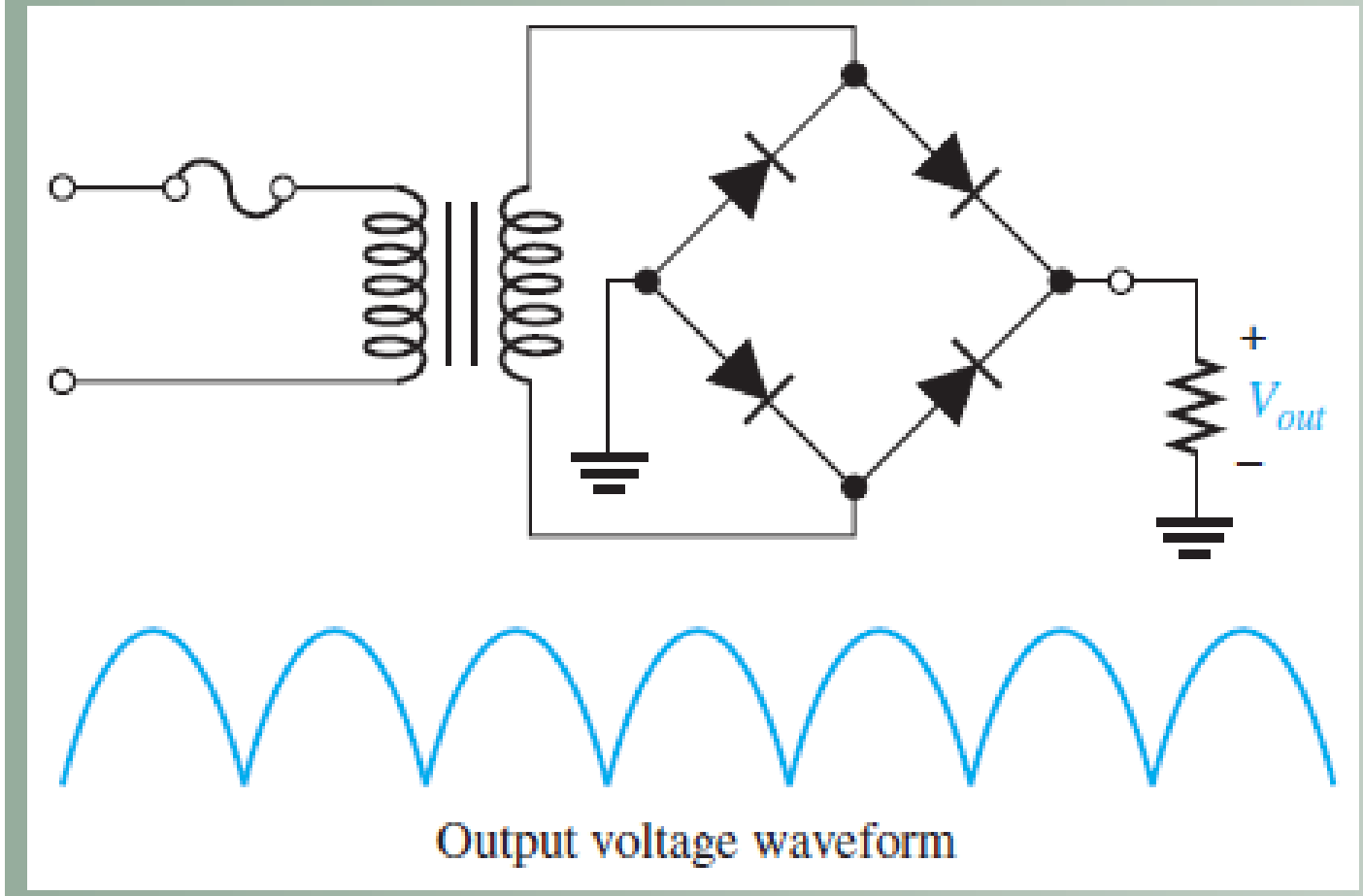
- Average value of output:

$$V_{AVG} = \frac{2V_{p(out)}}{\pi}$$

- Diode peak inverse voltage:

$$\text{PIV} = 2V_{p(out)} + 0.7\ \text{V}$$

BRIDGE FULL-WAVE RECTIFIER



Output voltage waveform

- Peak value of output:

$$V_{p(out)} = V_{p(sec)} - 1.4\ \text{V}$$

- Average value of output:

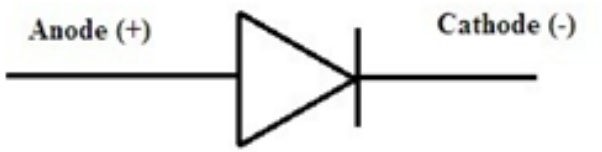
$$V_{AVG} = \frac{2V_{p(out)}}{\pi}$$

- Diode peak inverse voltage:

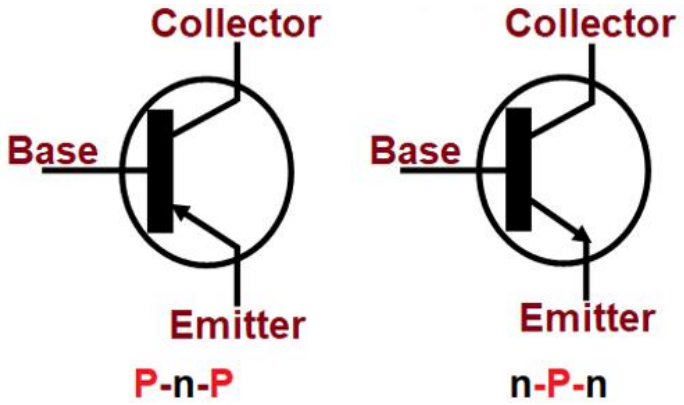
$$\text{PIV} = V_{p(out)} + 0.7\ \text{V}$$

Semiconductor Devices

Diode



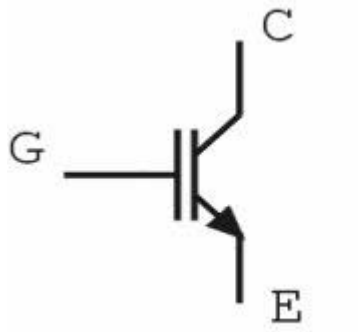
Bipolar Junction Transistor (BJT)



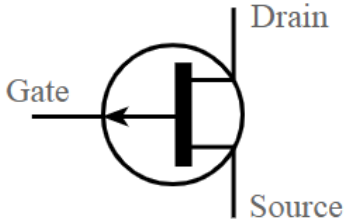
BJT Junctions	Operating Regions	Function
Collector-Base Junction	Cut-off region	OFF Switch
Base-Emitter Junction	Active region	Amplifier
	Saturation region	ON Switch

Semiconductor Devices

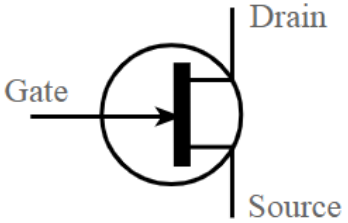
Insulated Gate Bipolar Transistor (IGBT)



Field Effect Transistor (FET)

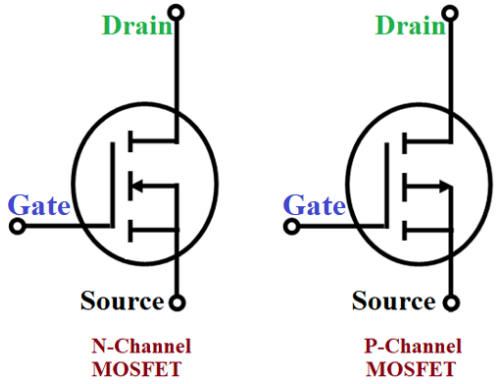


P-Channel



N-Channel

Metal Oxide Semiconductor Field Effect Transistor (MOSFET)



Important Terminologies

Gain (A): Ratio of output function to the input function.
Voltage Gain(A_V): It is defined as ratio of output voltage to the input voltage.
Current Gain (A_I): It is defined as ratio of output current to the input current.

Amplifier: An amplifier or electronic amplifier is an electronic device that can increase the power of a signal (a time-varying voltage or current).

Oscillator: An electronic oscillator is an electronic circuit that produces a periodic, oscillating electronic signal, often a sine wave or a square wave.

Module 1

Module-1: Diode Circuits: Diode clipping and clamping circuits.

Transistor Biasing and Stabilization:

The operating point, load line analysis, DC analysis and design of fixed bias circuit, emitter stabilized bias circuit, collector to base bias circuit, voltage divider bias circuit, modified DC bias with voltage feedback.

Bias stabilization and stability factors for fixed bias circuit, collector to base bias circuit and voltage divider bias circuit, bias compensation, Transistor switching circuits

Clipper Circuits or Limiters

The clipper circuits are used to remove the certain portions of the waveform above or below the certain levels, or Between the two reference voltages as per the requirement.

Classification of Clippers

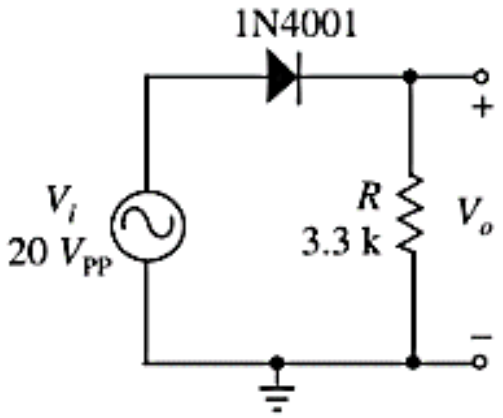
Series Clippers
1. Series Negative Clippers
2. Series Positive Clippers

Shunt Clippers
1. Shunt Negative Clippers
2. Shunt Positive Clippers

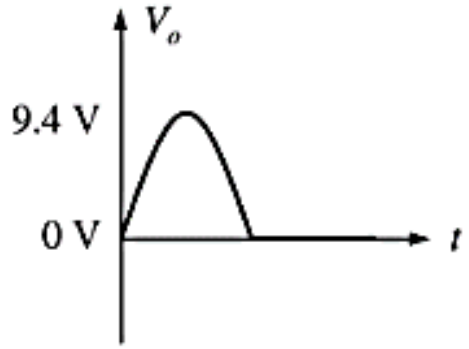
Double Ended Clippers

In series clippers the diode is connected in series with the load.

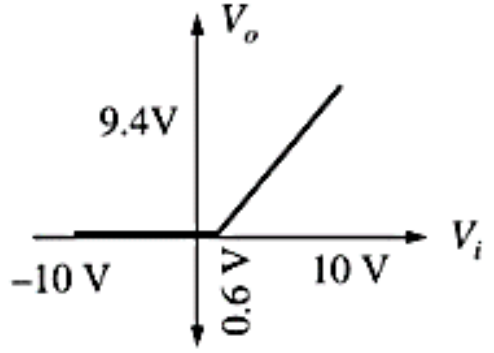
Series Negative Clipper Circuit (Unbiased)



(a) Circuit diagram



(b) Output waveform



(c) Transfer characteristics

The diode conducts (ON) for

$$v_I \geq V_K$$

Where,

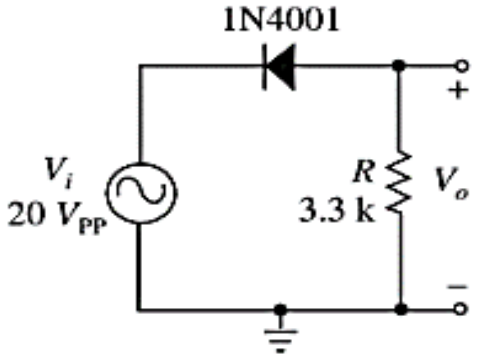
v_I = Input voltage

V_K = Voltage drop across diode

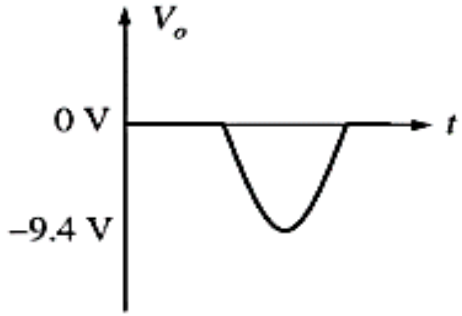
The diode is in OFF condition for

$$v_I \leq + V_K$$

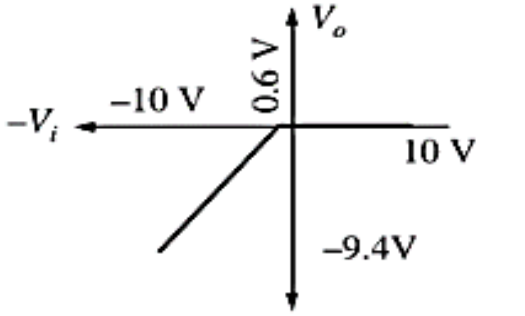
Series Positive Clipper Circuit (Unbiased)



(a) Circuit diagram



(b) Output waveform



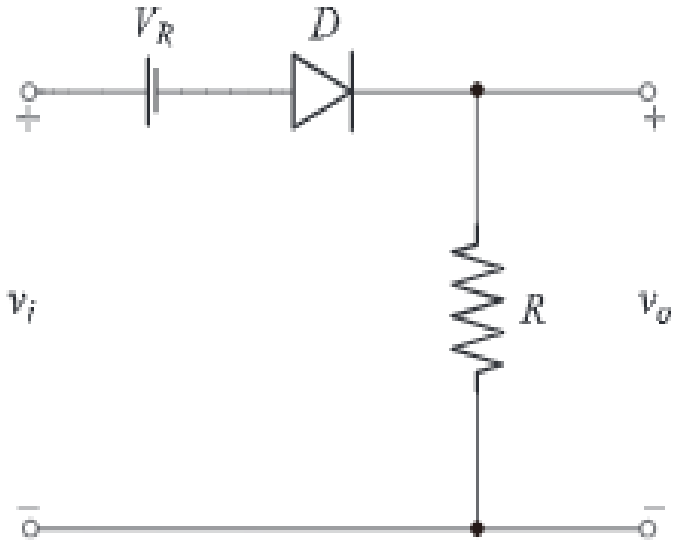
(c) Transfer characteristics

$V_{in(p-p)}$	$V_{o+(p)}$	$V_{o-(p)}$
8V		
12V		
20V		

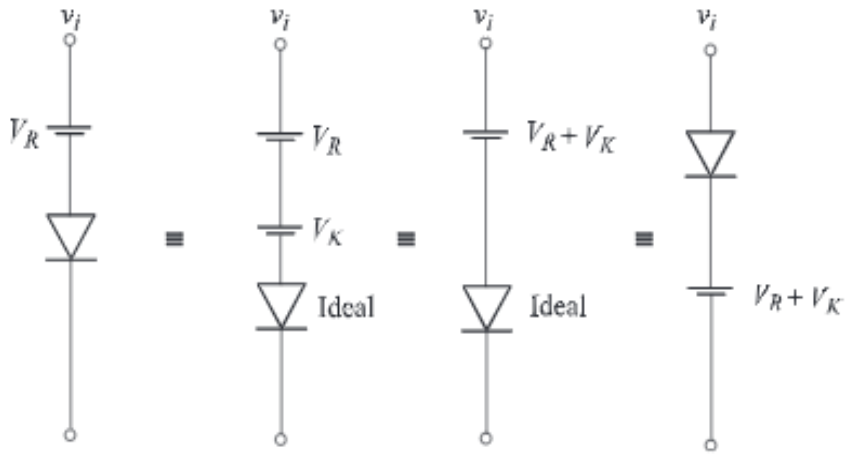
Series Negative Clippers (Biased)

In series clippers the diode is connected in series with the load.

Case-1



Circuit Diagram



Voltage on Diode Terminals

The diode conducts (ON) for

$$v_I \geq V_R + V_K$$

Where,

v_I = Input voltage

V_R= Reference voltage

V_K = Voltage drop across diode

Series Negative Clippers (Biased)

The diode conducts (ON) for

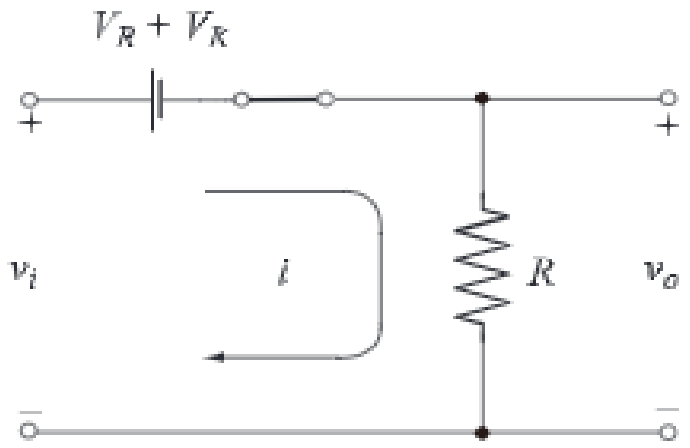
$$v_I \geq V_R + V_K$$

Where,

v_I = Input voltage

V_R = Reference voltage

V_K = Voltage drop across diode



Diode ON Condition

Apply KVL to the circuit, we get;

$$v_i - [V_R + V_K] - v_o = 0$$

$$v_o = v_i - [V_R + V_K] \quad \text{for} \quad v_I \geq V_R + V_K$$

when $v_i = v_m$, $v_o = v_m - [V_R + V_K]$

Since $V_R + V_K$ **is constant**

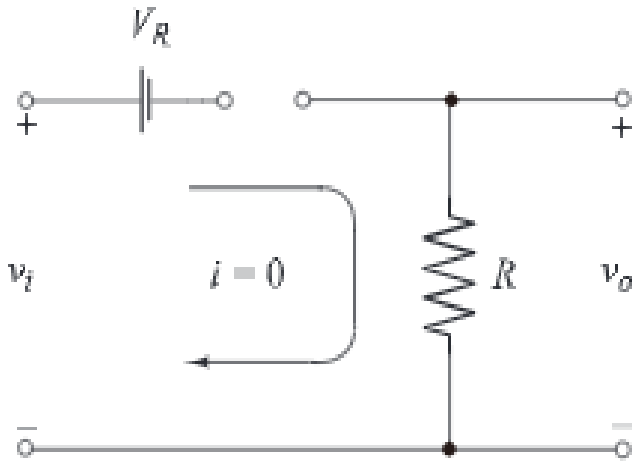
$$\Delta v_o = \Delta v_i$$

Hence slope $\frac{\Delta v_o}{\Delta v_i} = 1$

Series Negative Clippers (Biased)

The diode is in OFF condition for

$$v_I \leq V_R + V_K$$

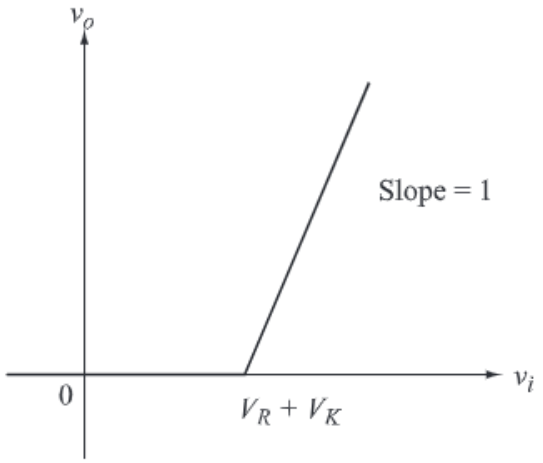


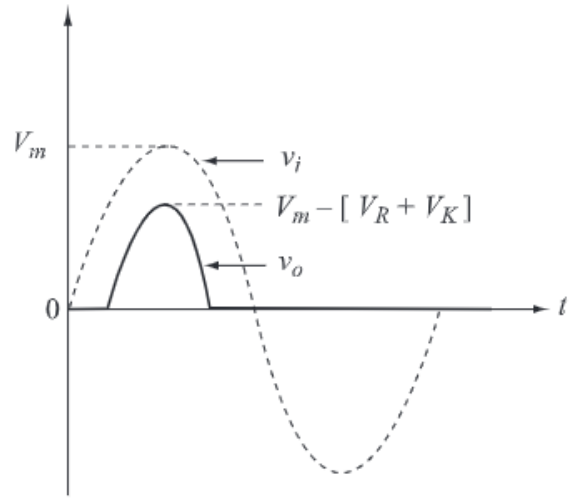
Diode OFF Condition

Apply KVL to the circuit, we get;

$$v_o = iR = 0$$

Hence slope $\frac{\Delta v_o}{\Delta v_i} = 0$

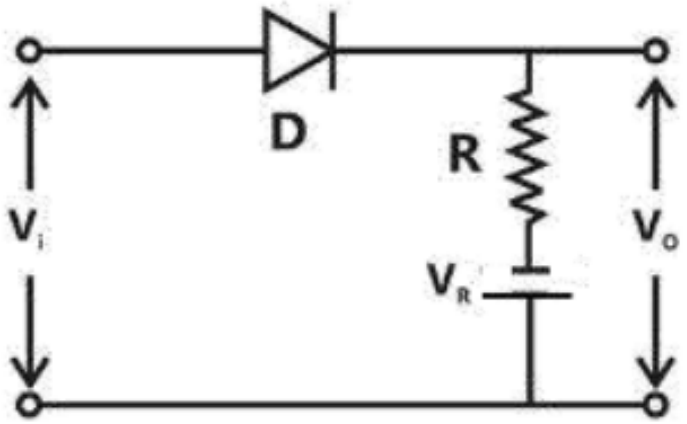




Transfer Characteristics and Output voltage Waveform

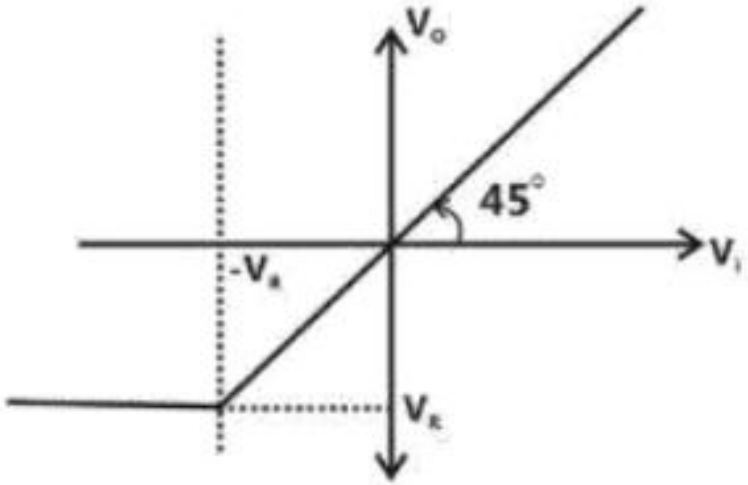
Series Negative Clippers (Biased)

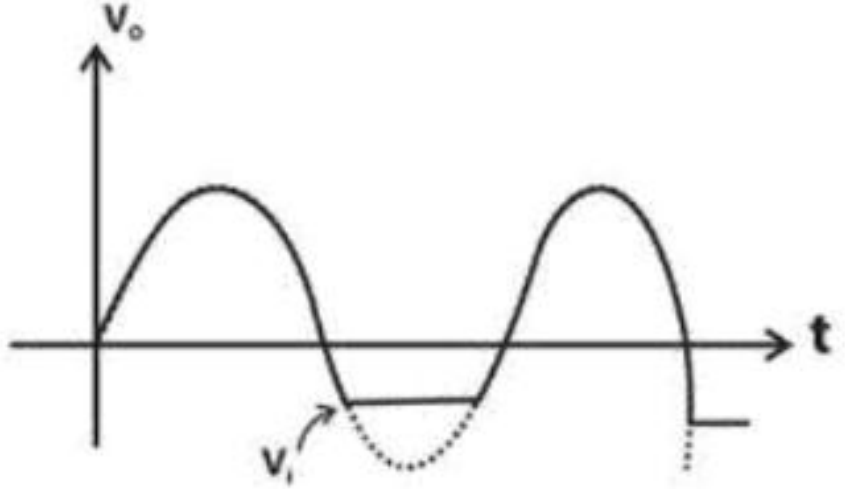
Case-2



$V_i = V_m \sin\omega t$: When $V_i < -V_R \Rightarrow V_o = -V_R$

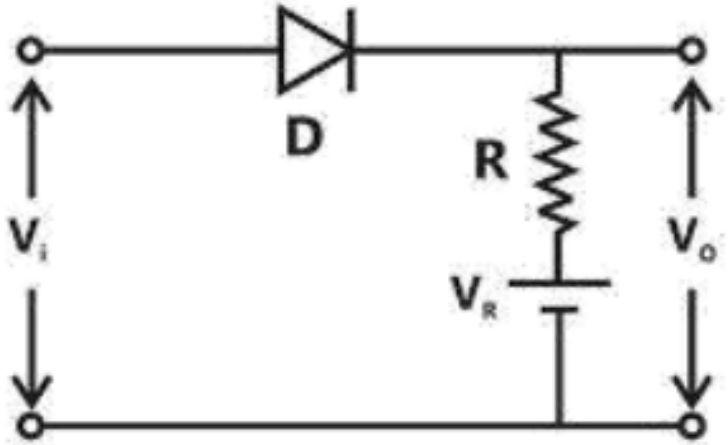
$V_m > -V_R$ When $V_i > -V_R \Rightarrow V_o = V_i$





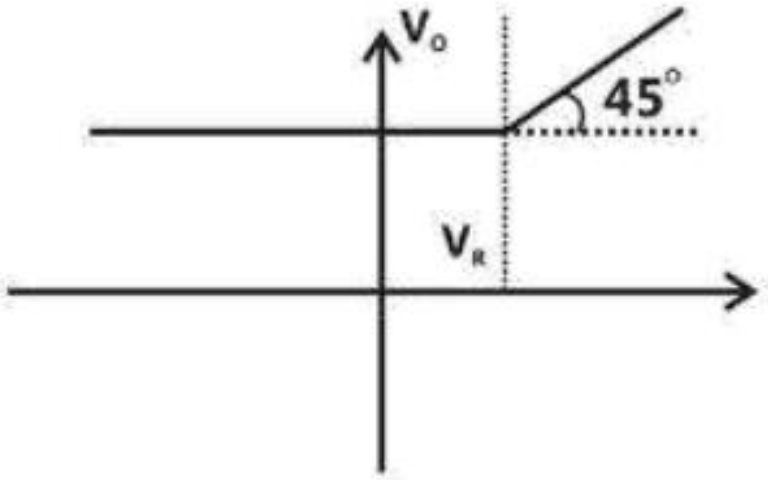
Series Positive Clippers (Biased)

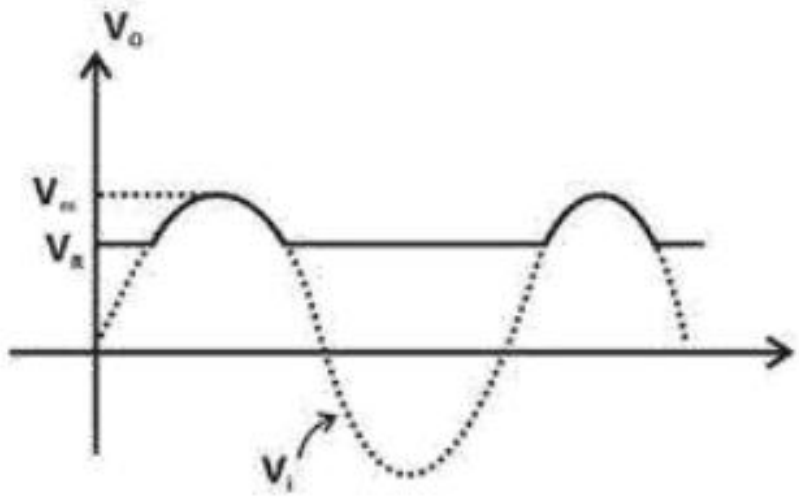
Case-2



$V_i = V_m \sin\omega t$: When $V_i < V_R$ => $V_O = V_R$

$V_m > V_R$ When $V_i > V_R$ => $V_O = V_i$

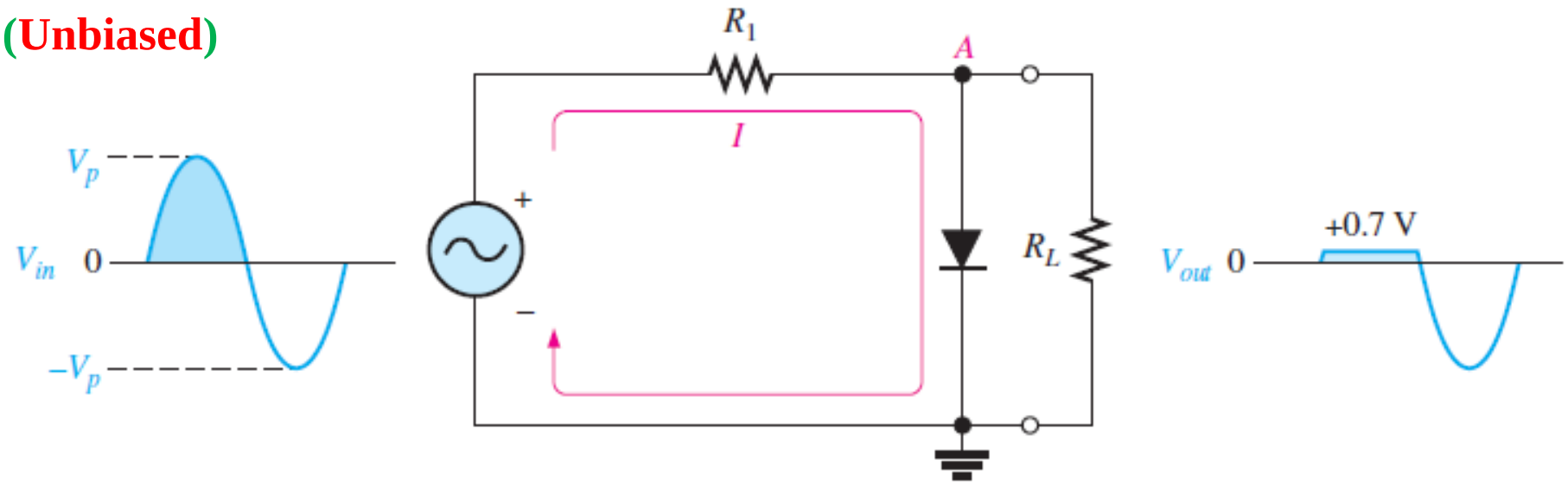




Shunt Positive Clippers (Unbiased)

Shunt Positive Clipper Circuit (Unbiased)

In Shunt/Parallel clippers the diode is connected in Parallel with the load.



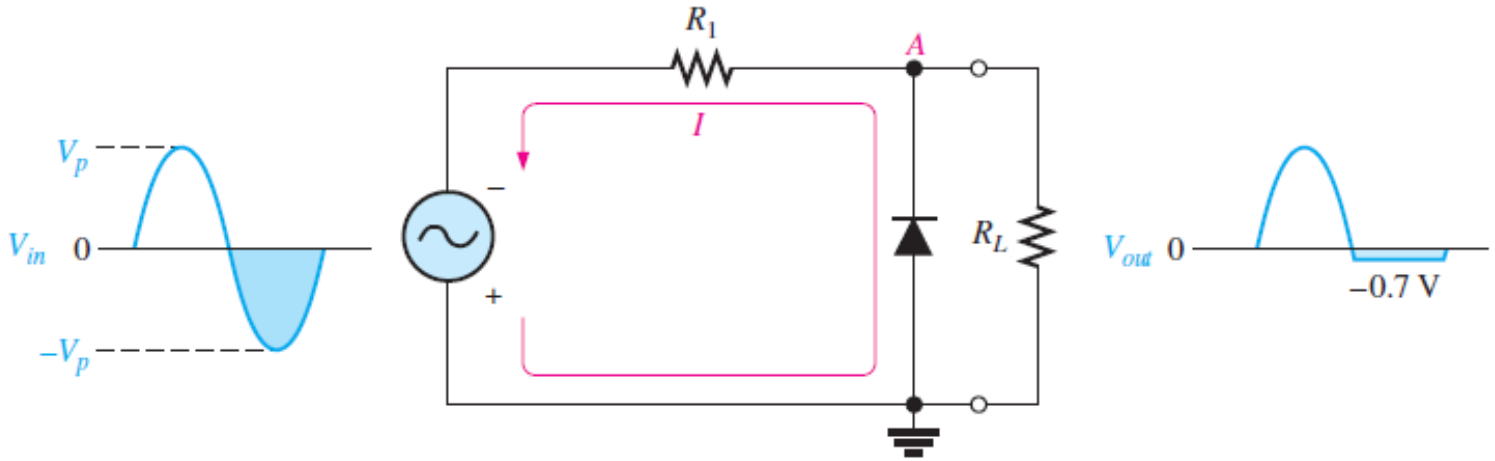
(a) Limiting of the positive alternation. The diode is forward-biased during the positive alternation (above 0.7 V) and reverse-biased during the negative alternation.

- As the input voltage goes positive, the diode becomes forward biased and conducts current.
- Point A is limited to +0.7 V when the input voltage exceeds this value.
- When the input voltage goes back below 0.7 V, the diode is reverse-biased and appears as an open.
- The output voltage looks like the negative part of the input voltage, but with a magnitude determined by the voltage divider formed by *R*1 and the load resistor, *RL*, as follows:

$$V_{out} = \left(\frac{R_L}{R_1 + R_L}\right) V_{in}$$

If R1 is small compared to RL, then Vout ~ Vin

Shunt Negative Clipper Circuit (Unbiased)



(b) Limiting of the negative alternation. The diode is forward-biased during the negative alternation (below –0.7 V) and reverse-biased during the positive alternation.

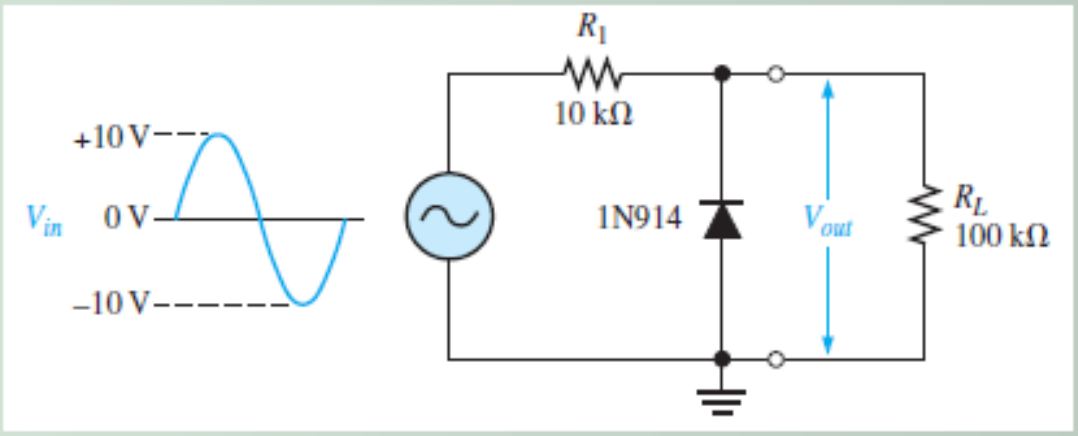
- If the diode is turned around, as in Figure (b), the negative part of the input voltage is clipped off.
- When the diode is forward-biased during the negative part of the input voltage, point A is held at -0.7 V by the diode drop.
- When the input voltage goes above -0.7 V, the diode is no longer forward-biased; and a voltage appears across RL proportional to the input voltage

$$V_{out} = \left(\frac{R_L}{R_1 + R_L}\right) V_{in}$$

If R1 is small compared to RL, then Vout ~ Vin

Shunt Negative Clipper Circuit (Unbiased)

What would you expect to see displayed on an oscilloscope connected across R_L in the limiter shown in Figure 2–53?

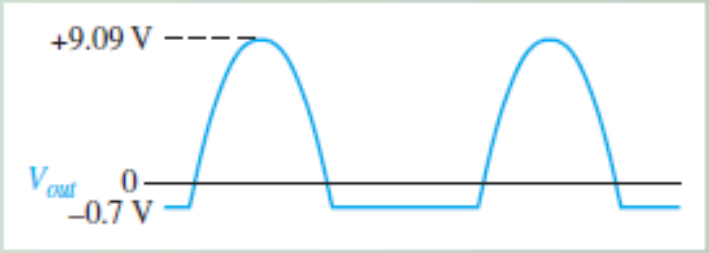


▲ FIGURE 2–53

The diode is forward-biased and conducts when the input voltage goes below −0.7 V. So, for the negative limiter, determine the peak output voltage across R_L by the following equation:

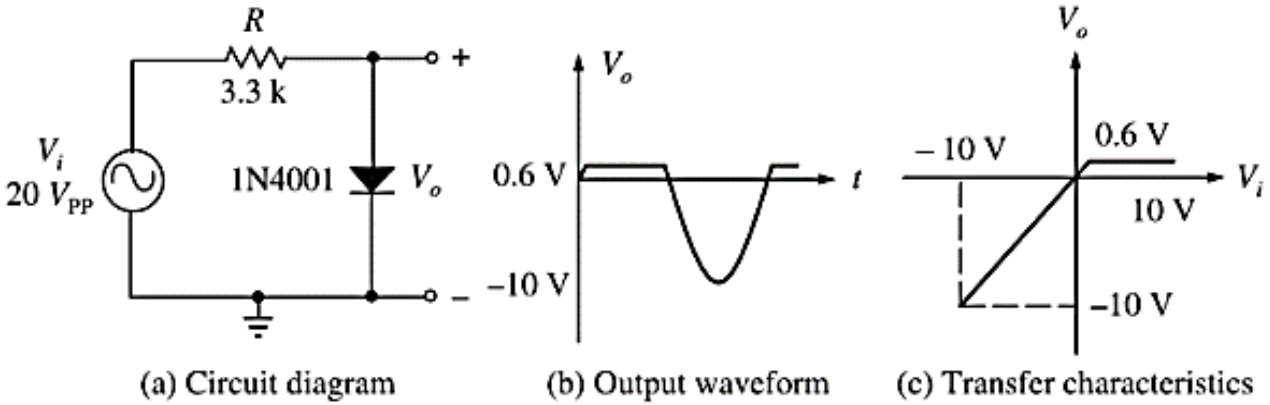
$$V_{p(out)} = \left(\frac{R_L}{R_1 + R_L}\right)V_{p(in)} = \left(\frac{100\,\text{k}\Omega}{110\,\text{k}\Omega}\right)10\text{ V} = 9.09\text{ V}$$

The scope will display an output waveform as shown in Figure 2–54.



▲ FIGURE 2–54

Shunt Positive Clipper Circuit (Unbiased)



(a) Circuit diagram (b) Output waveform (c) Transfer characteristics

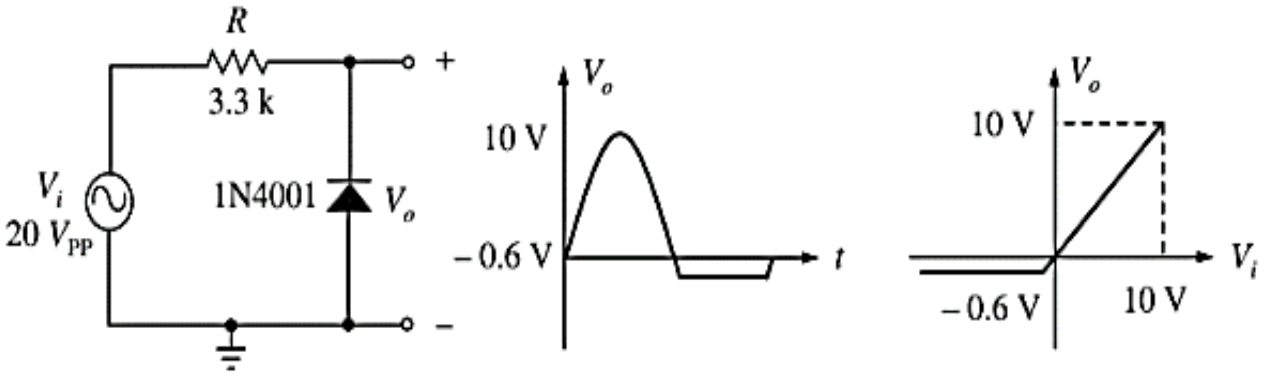
Circuit Operation;

for $v_i \geq +V_K$ Diode is ON $v_O = V_K$

for $v_i \leq V_K$ Diode is OFF $v_o = v_i$

$V_{in(p-p)}$	$V_{o+(p)}$	$V_{o-(p)}$
8V 12V 20V		

Shunt Negative Clipper Circuit (Unbiased)



(a) Circuit diagram (b) Output waveform (c) Transfer characteristics

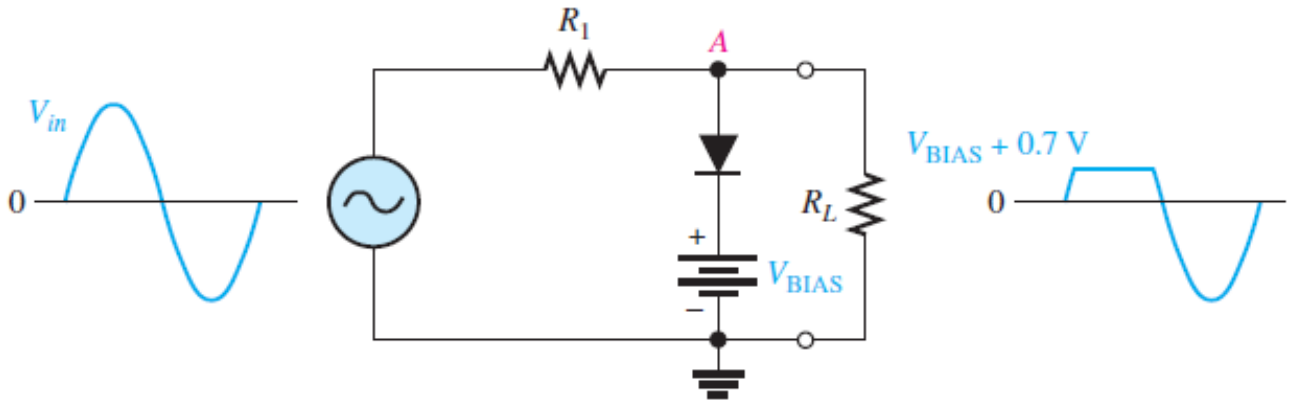
Circuit Operation;

for $v_I \leq -V_K$ Diode is ON $v_O = -V_K$

for $v_i \geq -V_K$ Diode is OFF $v_o = v_i$

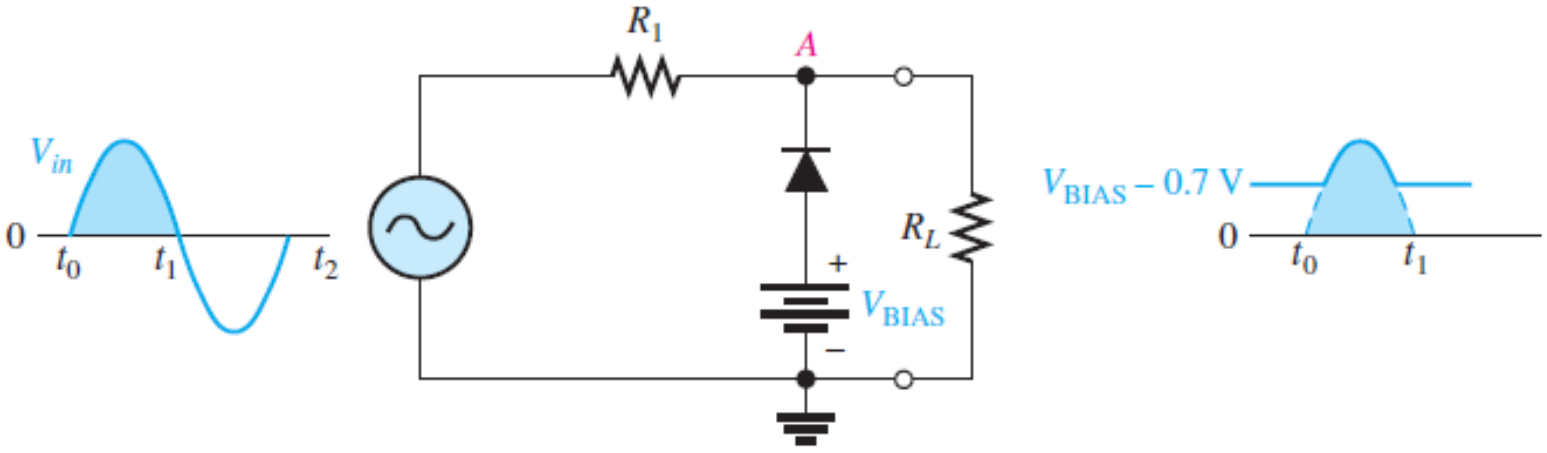
Shunt Biased Positive Clippers

- The level to which an AC voltage is limited can be adjusted by adding a bias voltage, V_{BIAS} (V_{ref}), in series with the diode, as shown in Figure.
- The voltage at point A must equal (V_{BIAS} + 0.7 V) before the diode will become forward-biased and conduct.
- Once the diode begins to conduct, the voltage at point A is limited to (V_{BIAS} + 0.7 V) so that all input voltage above this level is clipped off



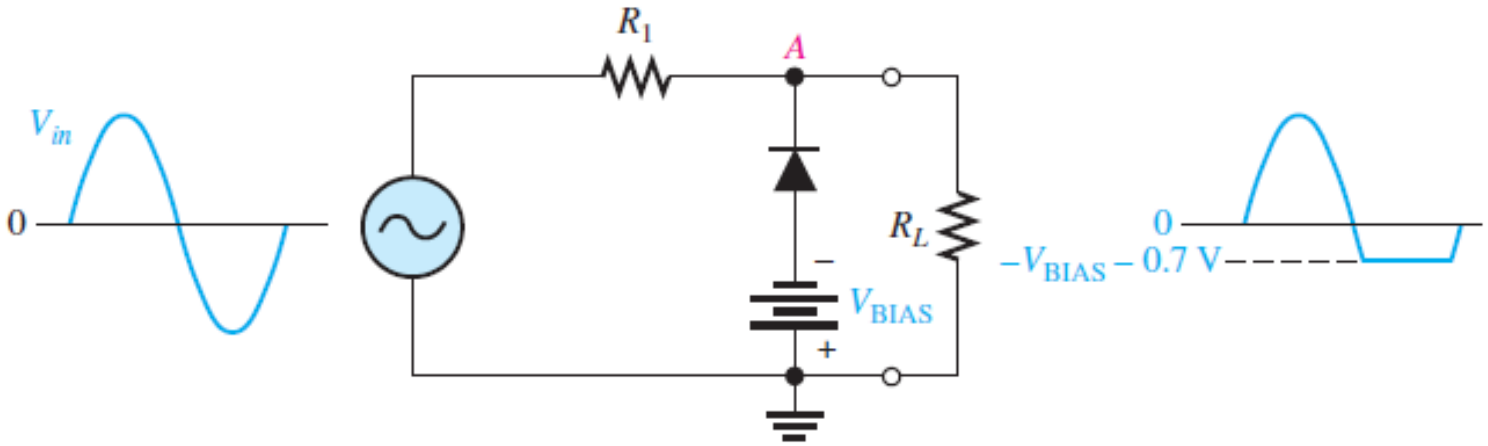
A Positive Limiter

- By turning the diode around, the positive limiter can be modified to limit the output voltage to the portion of the input voltage waveform above (VBIAS - 0.7V), as shown by the output waveform in Figure



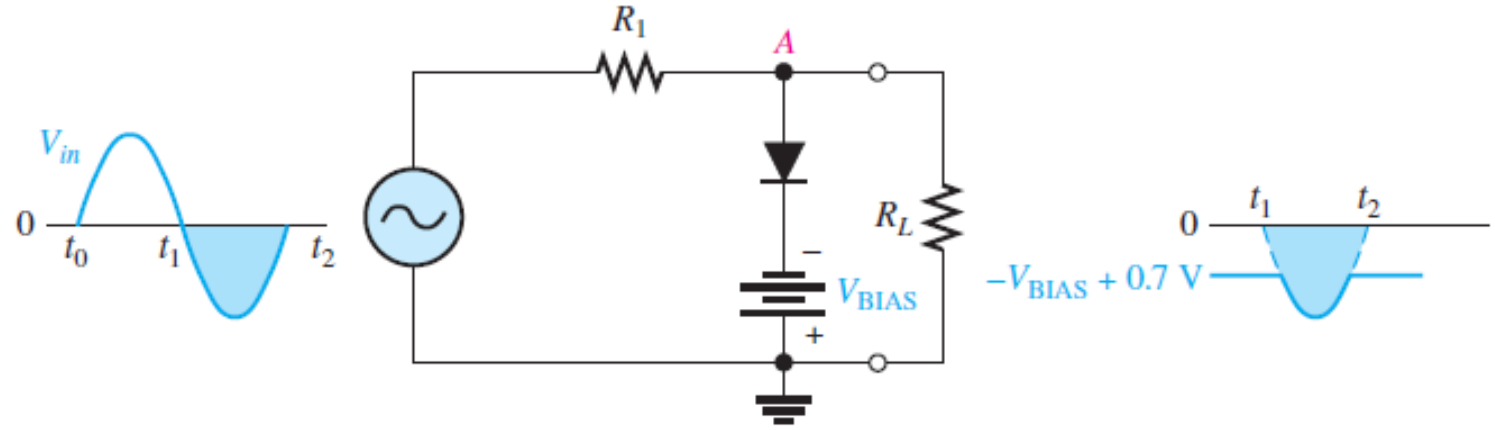
Shunt Biased Negative Clippers

- To limit a voltage to a specified negative level, the diode and bias voltage must be connected as in Figure.
- In this case, the voltage at point A must go below (-V_{BIAS} - 0.7 V) to forward-bias the diode and initiate limiting action as shown
- Once the diode begins to conduct, the voltage at point A is limited to (-V_{BIAS} - 0.7 V) so that all input voltage below this level is clipped off



A Biased Negative Limiter

- By turning the diode around, the negative limiter can be modified to limit the output voltage to the portion of the input voltage waveform below (-V_{BIAS} + 0.7 V), as shown by the output waveform

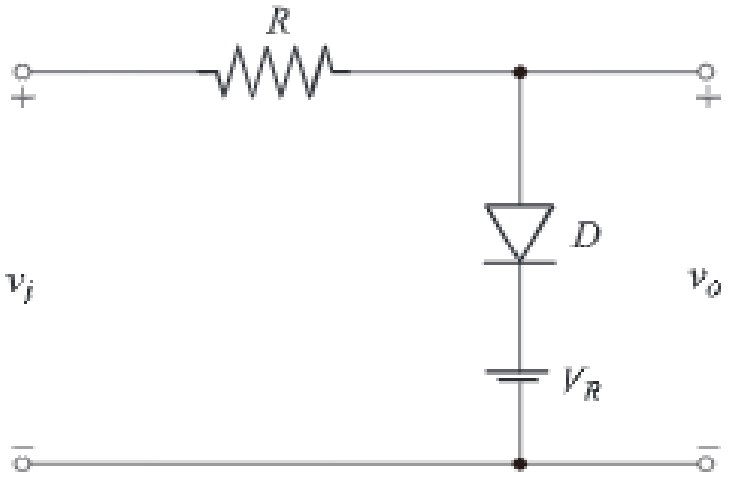


Shunt Positive Clippers (Biased)

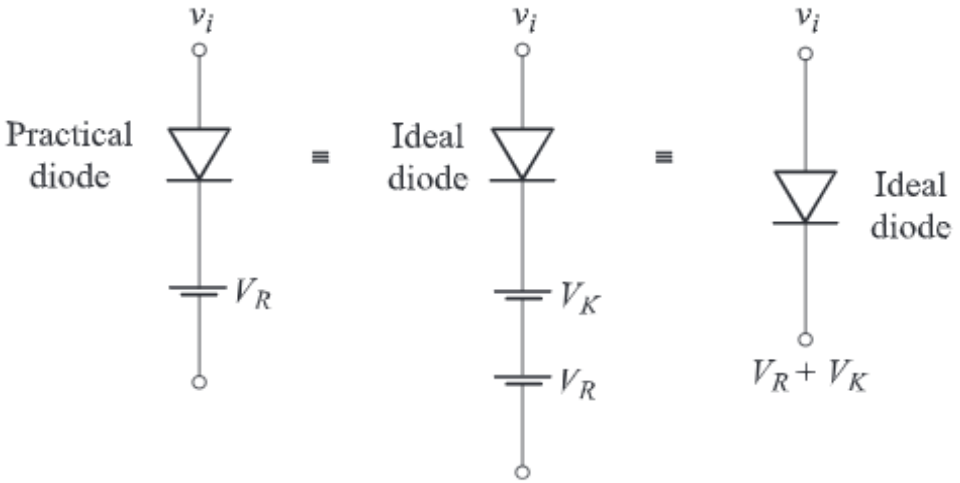
CASE 1

- The level to which an AC voltage is limited can be adjusted by adding a bias voltage, V_{BIAS} (V_{ref}), in series with the diode, as shown in Figure.

v_I = Input voltage
V_R= Reference voltage/ Bias Voltage
V_K = Voltage drop across diode



Circuit Diagram



Voltage on Diode Terminals

Shunt Positive Clippers (Biased)

The diode conducts (ON) for

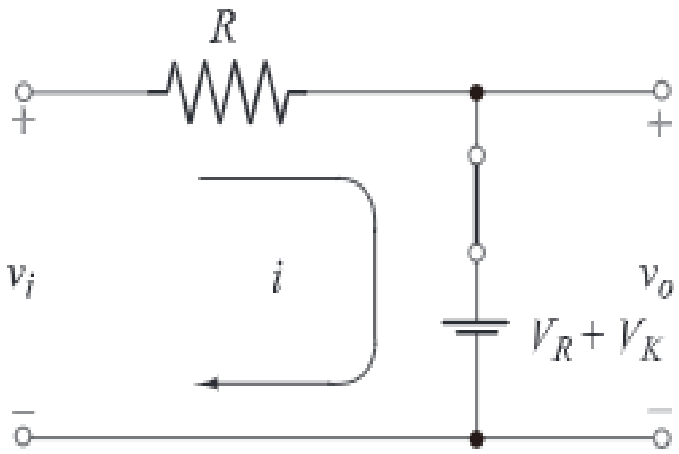
$$v_I \geq V_R + V_K$$

Where,

v_I = Input voltage

V_R = Reference voltage

V_K = Voltage drop across diode



Diode ON Condition

Apply KVL to the circuit, we get;

$v_O = V_R + V_K$ for $v_I \geq V_R + V_K$

Since $V_R + V_K$ is constant

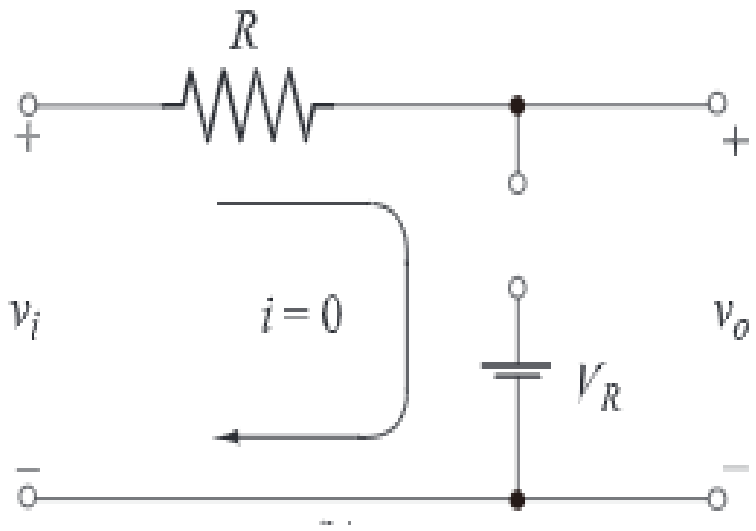
$\Delta v_o = 0$

Hence slope $\frac{\Delta v_o}{\Delta v_i} = 0$

Shunt Positive Clippers (Biased)

The diode is in OFF condition for

$$v_I \leq V_R + V_K$$



Diode OFF Condition

Apply KVL to the circuit, we get;

$v_i - iR - v_o = 0$

Neglecting the drop iR

$v_o = v_i$ **for** $v_i \leq V_R + V_K$

$\Delta v_o = \Delta v_i$

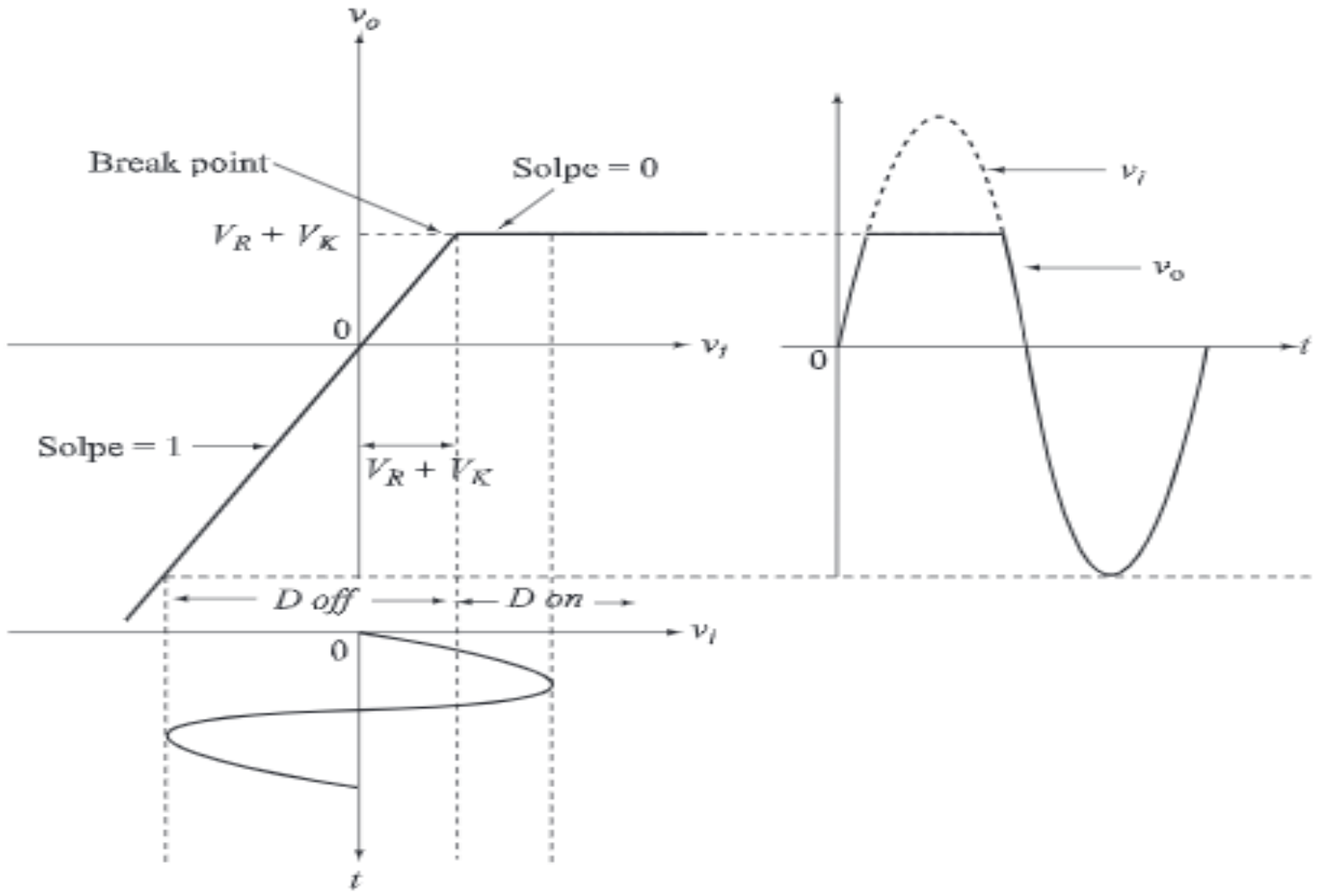
Hence slope $\frac{\Delta v_o}{\Delta v_i} = 1$

Shunt Positive Clippers (Biased)

Circuit Operation;

$v_O = V_R + V_K$ for $v_I \geq V_R + V_K$

$v_o = v_i$, for $v_i \leq V_R + V_K$

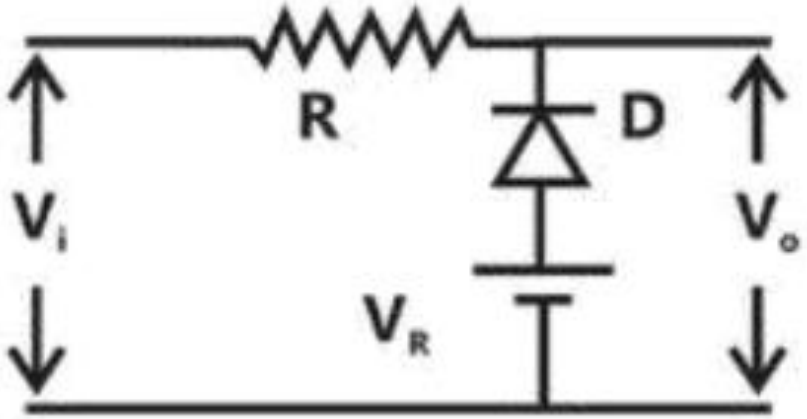


Transfer Characteristics and Output voltage Waveform

Shunt Positive Clippers (Biased)

CASE 2

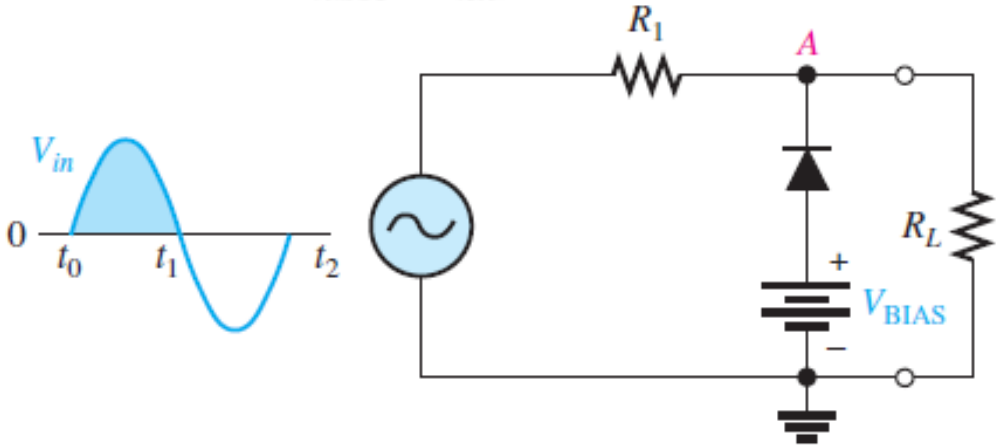
- By turning the diode around of Case-1, the positive limiter can be modified to limit the output voltage to the portion of the input voltage waveform above (V_{BIAS} - 0.7V), as shown by the output waveform in Figure

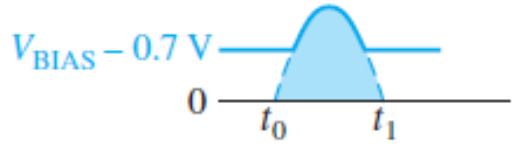


When $V_i < V_R$, D is ON

$V_o = V_R$

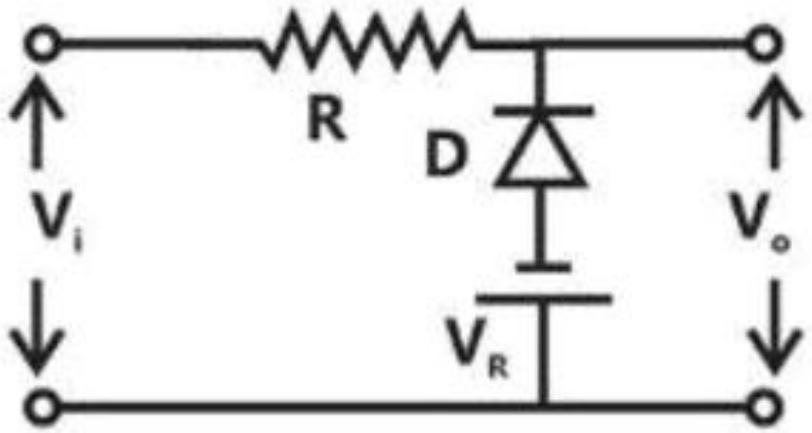
When $V_i > V_R$, D is OFF





Shunt Negative Clippers (Biased)

CASE 3



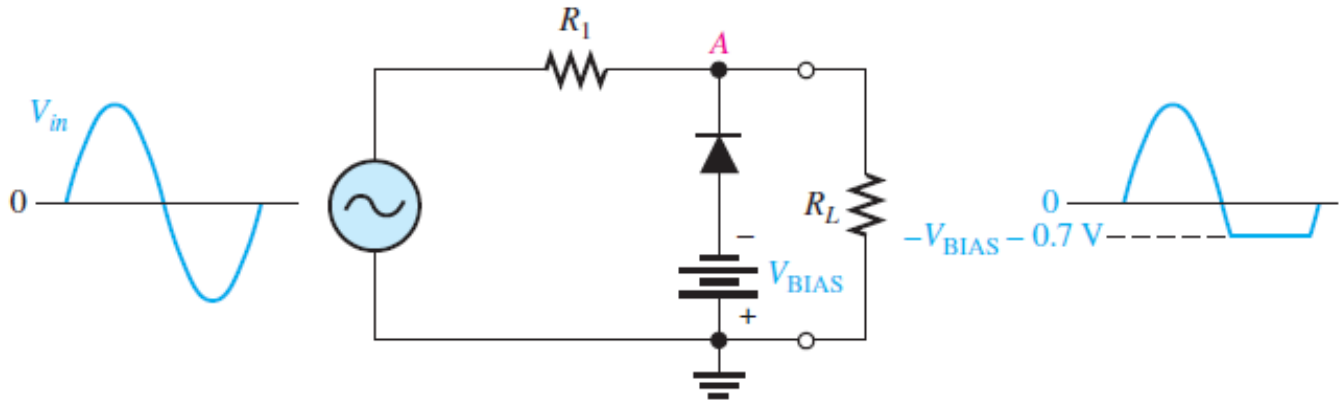
When $V_i < -V_R$, D is ON

$V_o = -V_R$

When $V_i > -V_R$, D is OFF

$V_o = V_i$

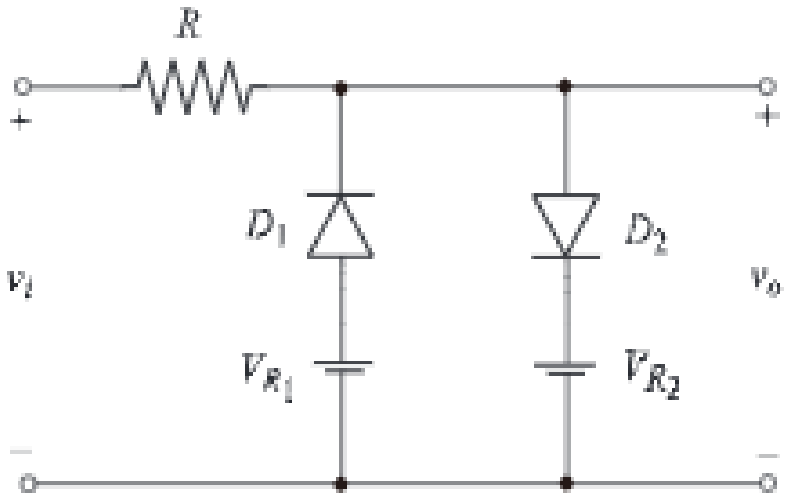
- To limit a voltage to a specified negative level, the diode and bias voltage must be connected as in Figure.
- In this case, the voltage at point A must go below ($-V_{BIAS}$ - 0.7 V) to forward-bias the diode and initiate limiting action as shown
- Once the diode begins to conduct, the voltage at point A is limited to ($-V_{BIAS}$ - 0.7 V) so that all input voltage below this level is clipped off



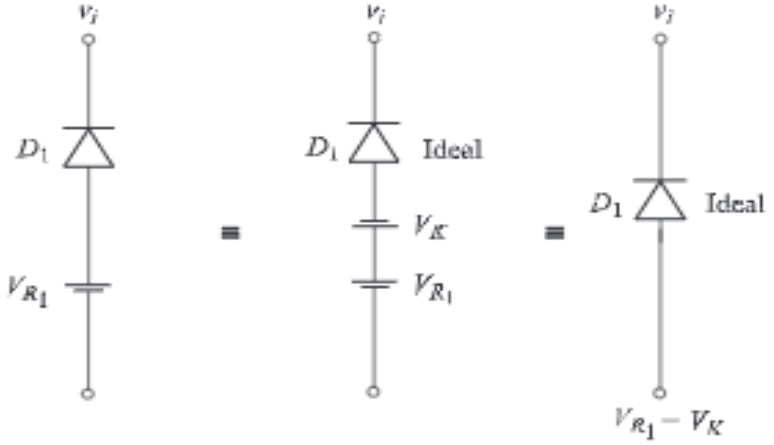
Double Ended Clippers

Two shunt clippers can be combined to obtain clipping at two independent levels.

CASE 1



Circuit Diagram



Voltage on Diode (D_1)Terminals

Note:

V_{R1} and V_{R2} are positive
V_{R1} forward biases D_1
V_{R2} reverse biases D_2
$V_{R2} > V_{R1}$

Double Ended Clippers

The diode D_1 conducts (ON) for

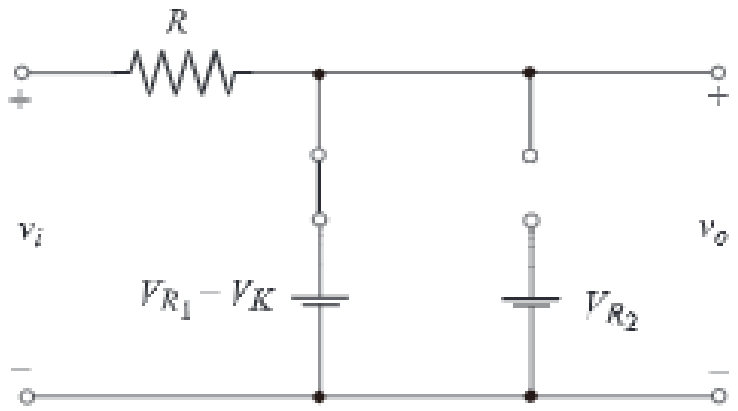
$$v_I \leq V_{R1} - V_K$$

Where,

v_I = Input voltage

V_{R1}= Reference voltage

V_K = Voltage drop across diode



Diode D_1 ON Condition

Apply KVL to the circuit, we get;

$v_o = V_{R1} - V_K$ for $v_I \leq V_{R1} - V_K$

Hence slope $\frac{\Delta v_o}{\Delta v_i} = 0$

Double Ended Clippers

The diode D_2 conducts (ON) for

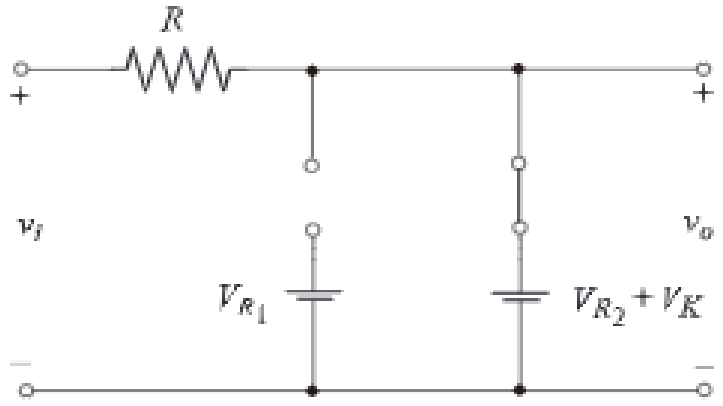
$$v_I \geq V_{R2} + V_K$$

Where,

v_I = Input voltage

V_{R2}= Reference voltage

V_K = Voltage drop across diode



Diode D_2 ON Condition

Apply KVL to the circuit, we get;

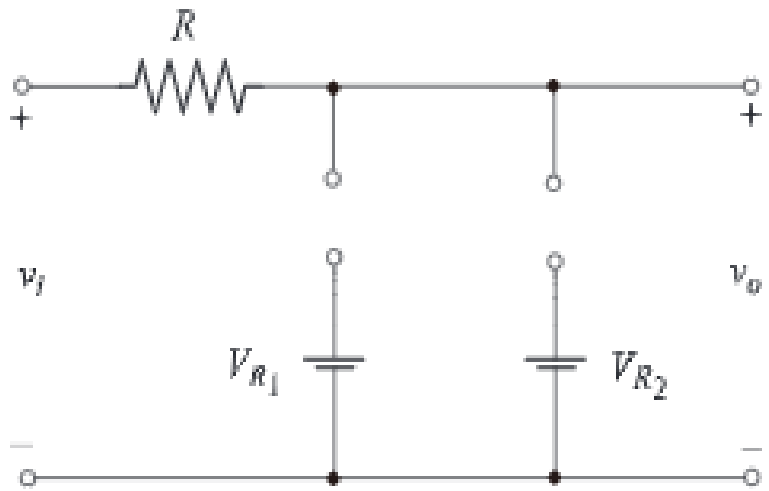
$v_o = V_{R2} + V_K$ **for** $v_I \geq V_{R2} + V_K$

Hence slope $\frac{\Delta v_o}{\Delta v_i} = 0$

Double Ended Clippers

For $(V_{R1} - V_K) < v_i < (V_{R2} + V_K)$

D_1 & D_2 are in OFF condition



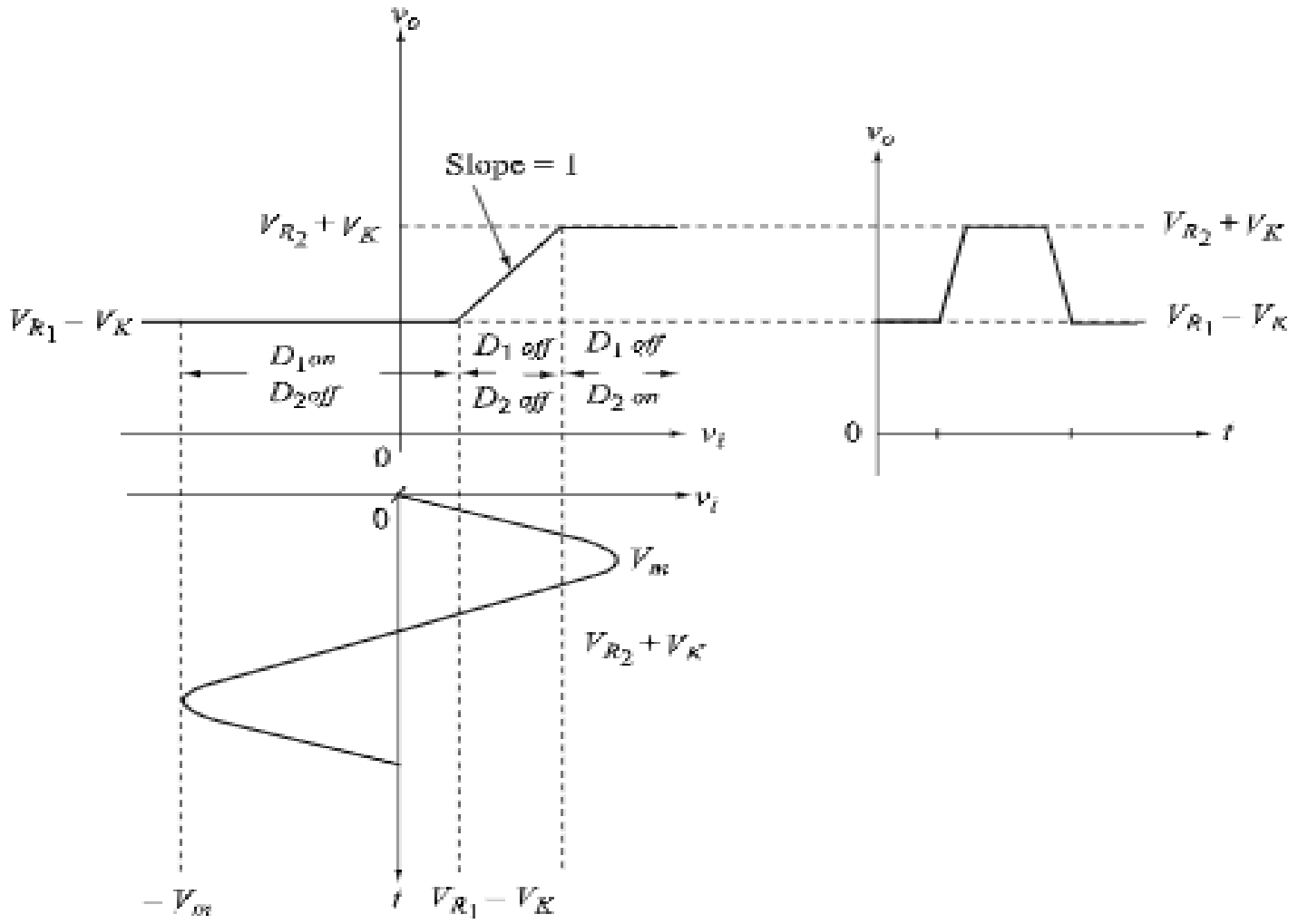
Diode D_1 & D_2 OFF Condition

Apply KVL to the circuit, we get;

$v_o = v_i$

Hence slope $\frac{\Delta v_o}{\Delta v_i} = 1$

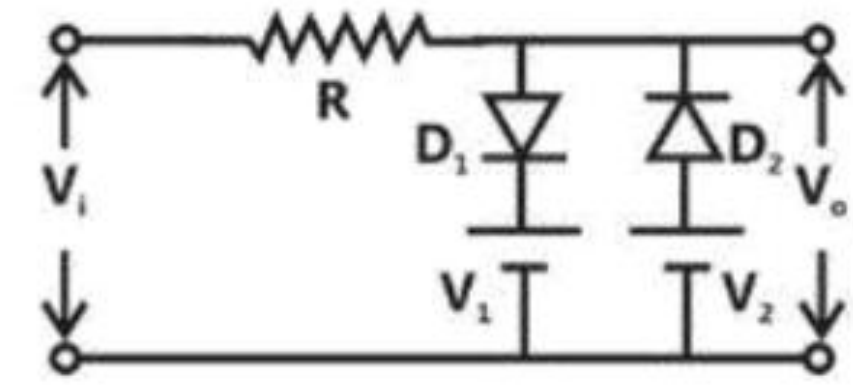
Double Ended Clippers

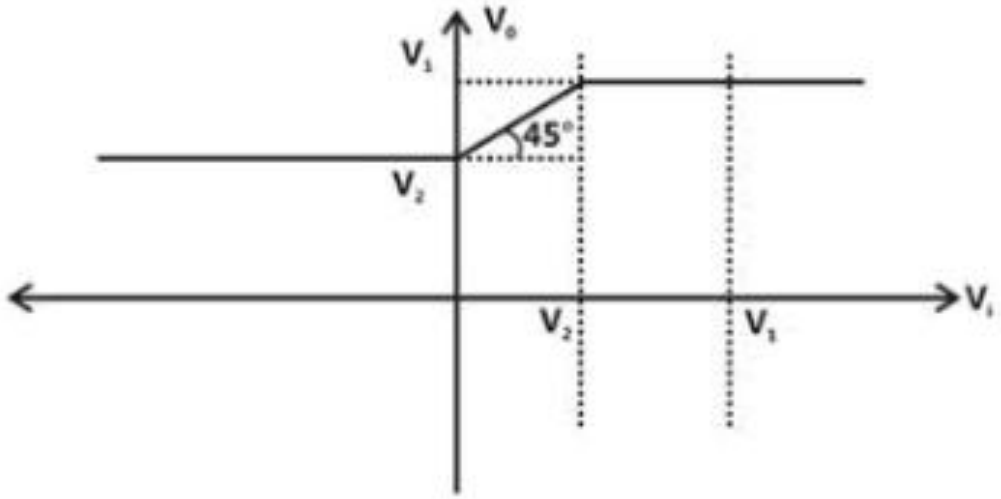


Transfer Characteristics and Output voltage Waveform

Double Ended Clippers

CASE 2





When $V_i < V_2$, D_1 is OFF & D_2 is ON

$V_0 = V_2$

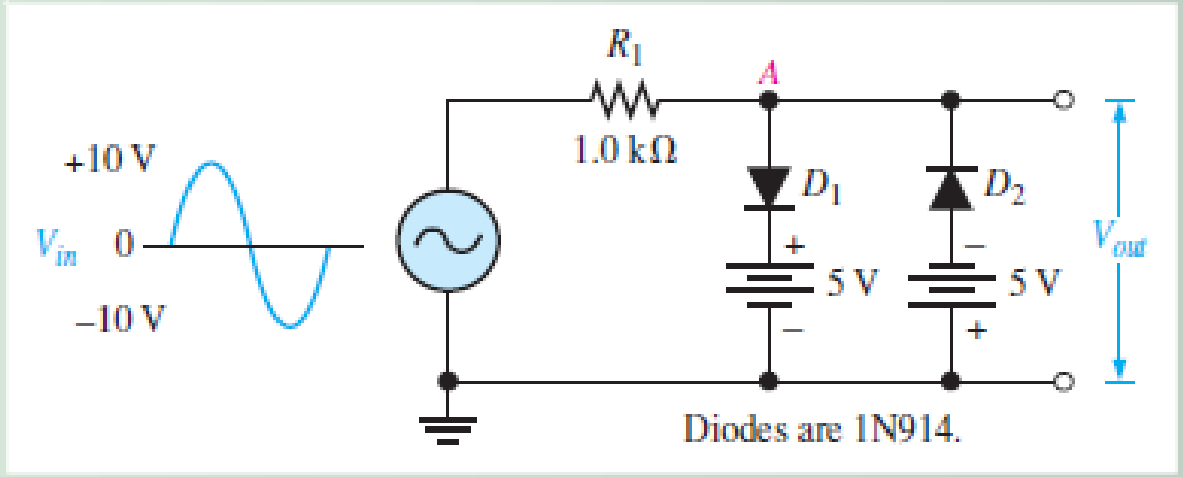
When $V_i \geq V_2$ & $V_i < V_1$, D_2 is OFF & D_1 is OFF

$V_o = V_i$

When $V_i > V_1$, D_2 is OFF D_l is ON

$V_o = V_1$

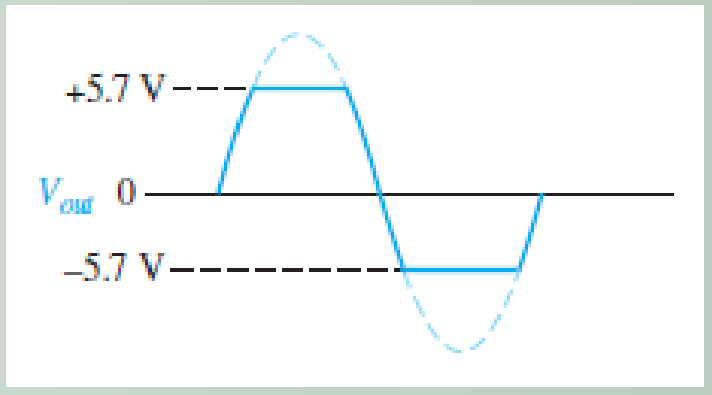
Figure 2–58 shows a circuit combining a positive limiter with a negative limiter. Determine the output voltage waveform.



When the voltage at point *A* reaches +5.7 V, diode D_1 conducts and limits the waveform to +5.7 V. Diode D_2 does not conduct until the voltage reaches −5.7 V. Therefore, positive voltages above +5.7 V and negative voltages below −5.7 V are clipped off. The resulting output voltage waveform is shown in Figure 2–59.

▶ **FIGURE 2–59**

Output voltage waveform for Figure 2–58.



Clamper Circuits

A Clamper adds a dc level to an ac voltage.

Clamper circuits can also be referred to as D.C Restorers, Baseline Stabilizers, DC Reinserters, Level Shifter

Classification of Clampers

1. **Positive Clampers**
2. **Negative Clampers**

Assumptions

1. **The time constant $\tau = RC$ is designed to very large by selecting large values of R and C.**

Clamper Circuits

Clamping circuits are used to add dc level (positive or negative) to the input AC signal, it moves the entire signal up or down to place the peaks at the desired reference level.

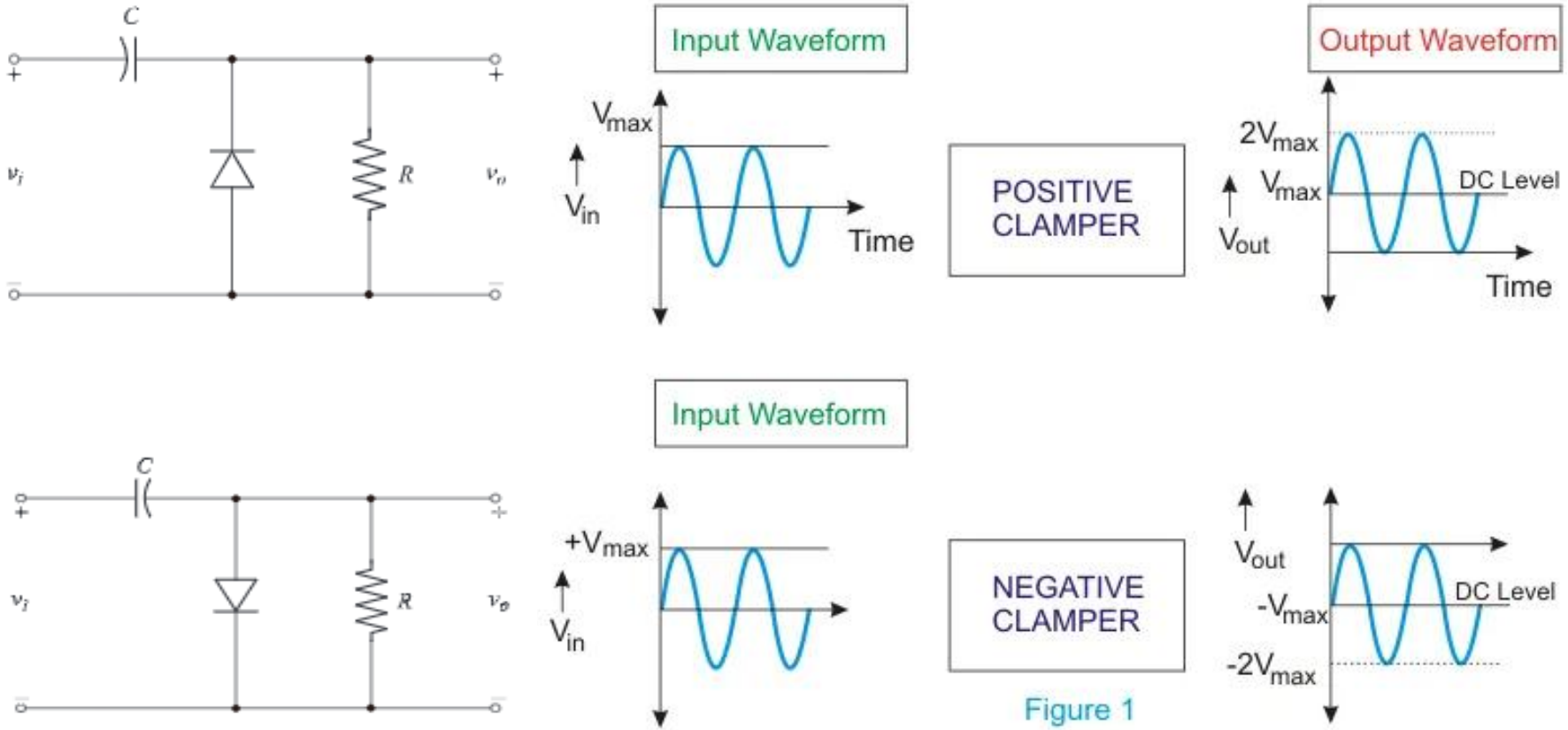


Figure 1

The positive clamper circuit adds the positive dc level to the input signal

when it shifts the signal to the upward or positive sides, both the negative peak and the zero levels will meet, which is **called the positive clamper circuit**

A simple negative clamper circuit is used to add a negative level to the ac output.

When it shifts the signal to the downside or negative side, both the positive peak and the zero levels will meet, which we refer to as the **negative clamper circuit**

- The minimum number of components of a clamping circuit is three a capacitor, a resistor, and a diode. In some cases, a DC supply is also needed to give an additional shift.

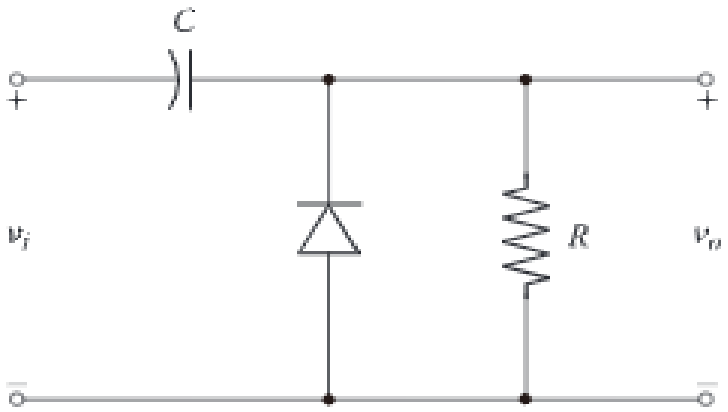
- The nature of the waveform remains the same, but the difference is in the shifted level (up or down). The peak to the peak value of the waveform will never change.

- The peak value and average value of the input waveform and the clamped output will be different.

- The time constant of the circuit (RC) must have to be ten times the time period of the entering (input) AC voltage for the better clamping action.

Positive Clamper Circuits

The positive clamper circuit adds the positive dc level to the input AC signal.

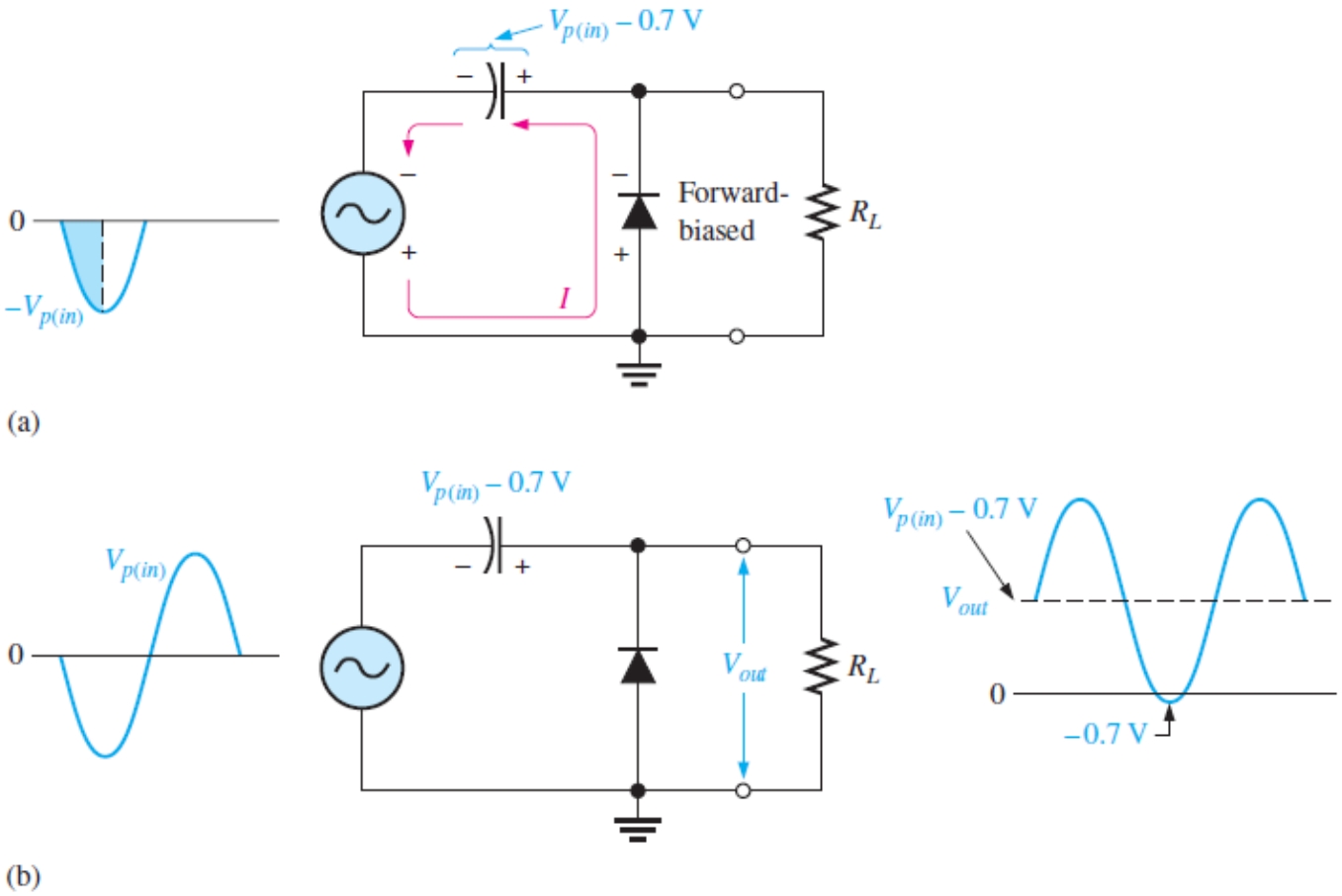


Circuit Diagram

- **The diode conducts during negative half cycle.**
- **The capacitor gets charged to a voltage level of V_M** (Peak of the input)
- **The charging time constant is $\tau = RC$.**

- **The diode is in OFF condition during positive half cycle.**
- **The capacitor gets discharged into R.**

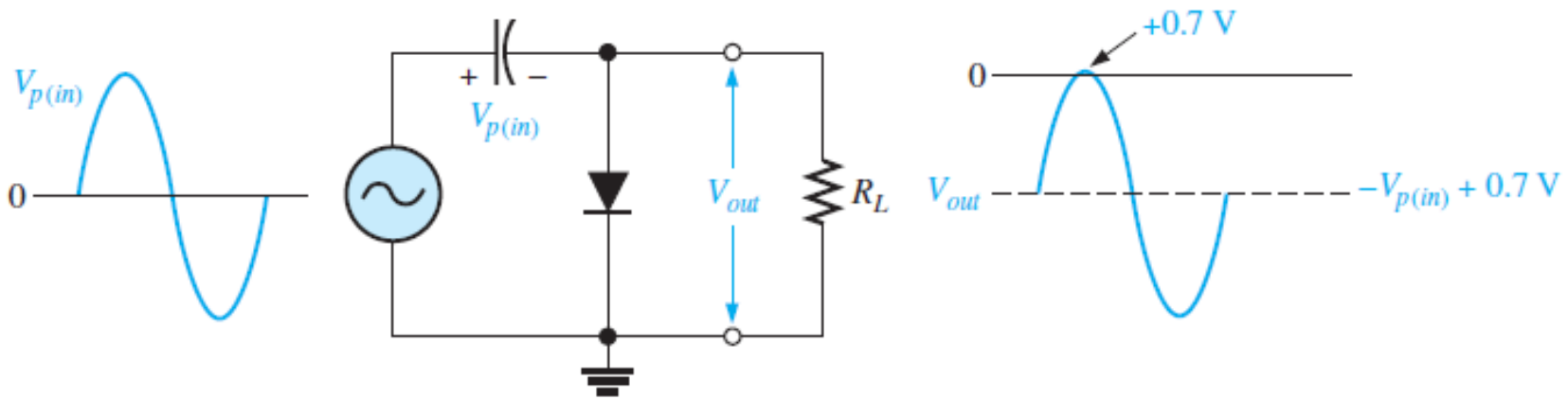
- The operation of this circuit can be seen by considering the first negative half-cycle of the input voltage. When the input voltage initially goes negative, the diode is forward biased, allowing the capacitor to charge to near the peak of the input (Vp(in) - 0.7 V), as shown in Figure(a). Just after the negative peak, the diode is reverse-biased. This is because the cathode is held near Vp(in) - 0.7 V by the charge on the capacitor. The capacitor can only discharge through the high resistance of RL. So, from the peak of one negative half-cycle to the next, the capacitor discharges very little. The amount that is discharged, of course, depends on the value of RL.



Positive clamper operation

- If the capacitor discharges during the period of the input wave, clamping action is affected. If the *RC* time constant is 100 times the period, the clamping action is excellent.
- An *RC* time constant of ten times the period will have a small amount of distortion at the ground level due to the charging current.
- The net effect of the clamping action is that the capacitor retains a charge approximately equal to the peak value of the input less the diode drop. The capacitor voltage acts essentially as a battery in series with the input voltage. The dc voltage of the capacitor adds to the input voltage by superposition, as in Figure(b).

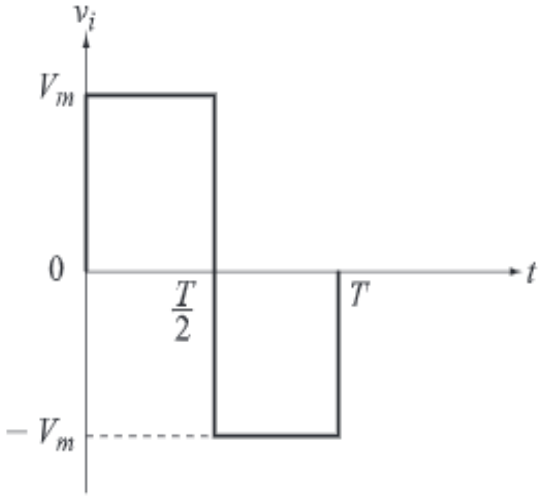
- If the diode is turned around, a negative dc voltage is added to the input voltage to produce the output voltage as shown in Figure



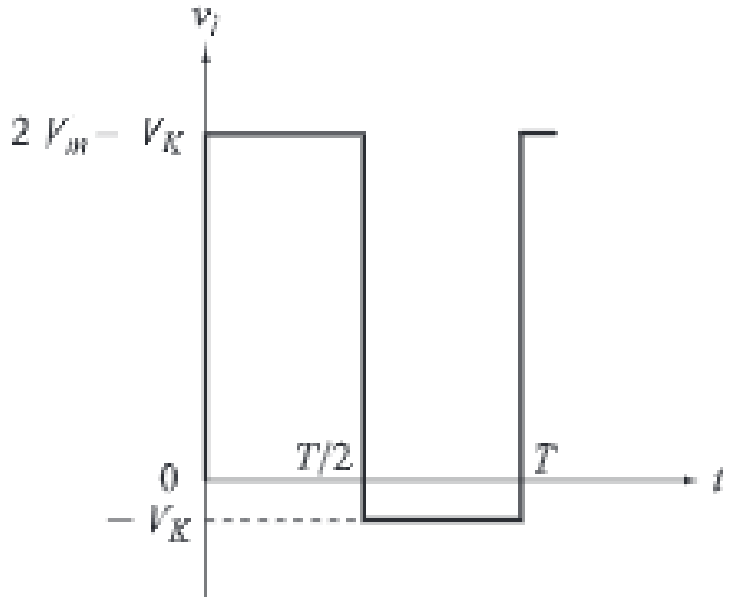
Negative clamper

Positive Clamper Circuits

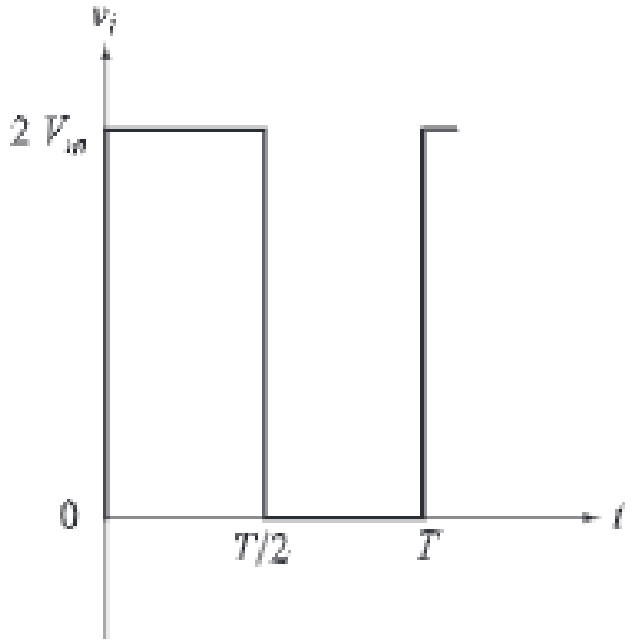
Input voltage level v_i	Output voltage level	
	Practical diode $v_o = v_i + [V_m - V_K]$	Ideal diode $v_o = v_i + V_m$
0	$V_m - V_K$	V_m
V_m	$2V_m - V_K$	$2V_m$
$-V_m$	$-V_K$	0



Input Signal



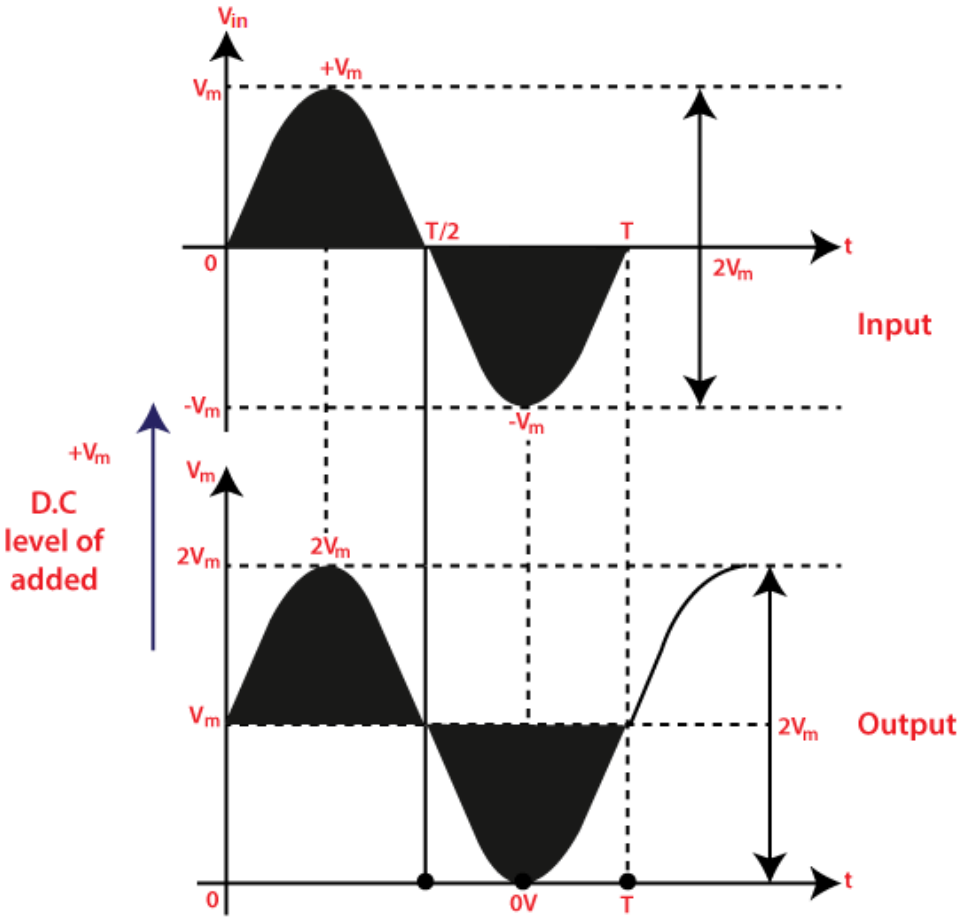
Output waveform for Practical diode



Output waveform for Ideal diode

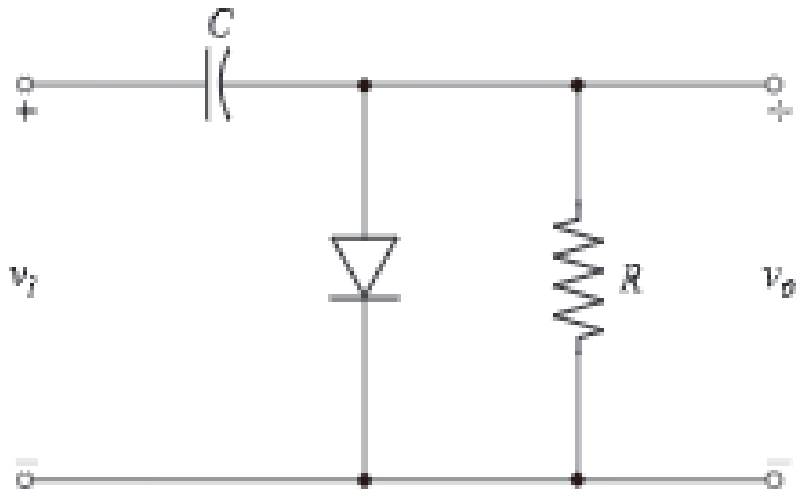
Positive Clamper Circuits

Input voltage level v_i	Output voltage level	
	Practical diode $v_o = v_i + [V_m - V_K]$	Ideal diode $v_o = v_i + V_m$
0	$V_m - V_K$	V_m
V_m	$2V_m - V_K$	$2V_m$
$-V_m$	$-V_K$	0



Negative Clamper Circuits

A simple negative clamper circuit is used to add a negative level to the ac output.

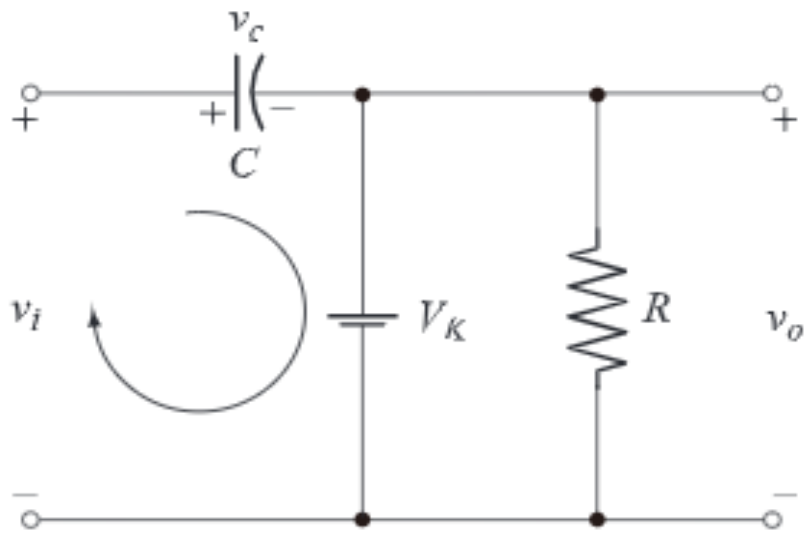


Circuit Diagram

- **The diode conducts during positive half cycle.**
- **The capacitor gets charged to a voltage level of V_M.**
- **The charging time constant is $\tau_f = r_f C$.**

Where,
r_f = diode internal resistance
C = Capacitor

Negative Clamper Circuits



Diode ON condition

Apply KVL to the circuit, we get;

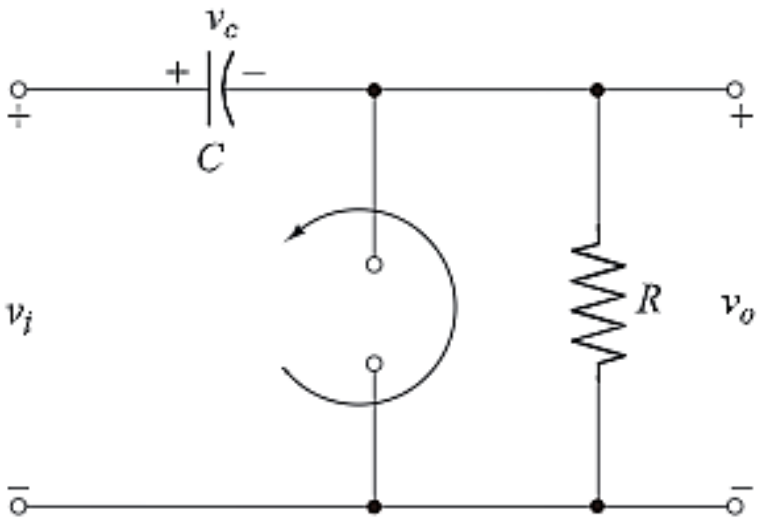
$v_i - v_c - V_K = 0$

$v_c = V_K - v_i$

When $v_i = V_M$;

$v_c = V_K - V_M$

Negative Clamper Circuits



Diode in OFF condition

- **The diode is in OFF condition during negative half cycle.**
- **The capacitor gets discharged into R.**
- **The charging time constant is $\tau = RC$.**

Apply the KVL for the circuit we get;

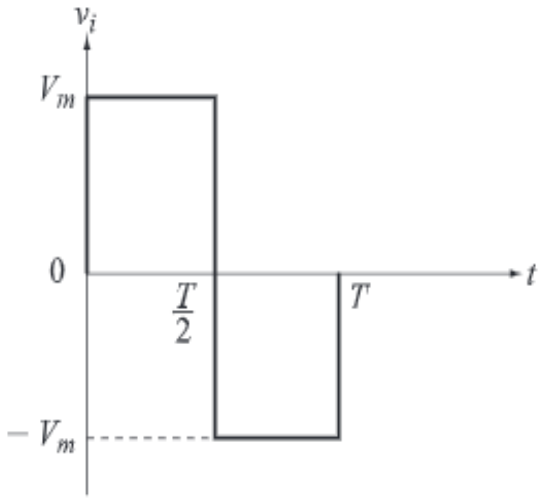
$v_i - v_c - v_o = 0$

$v_o = v_i - v_c$

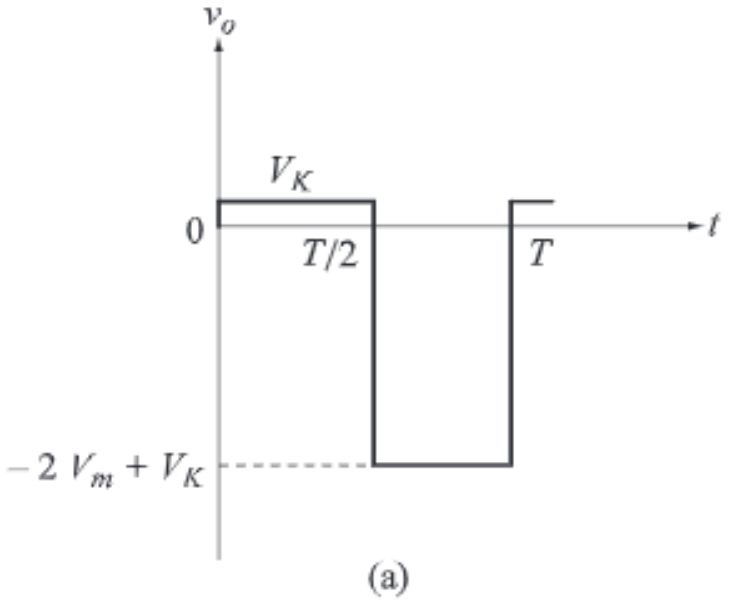
When $v_c = V_M - V_K$;

$v_o = v_i - [V_M - V_K]$

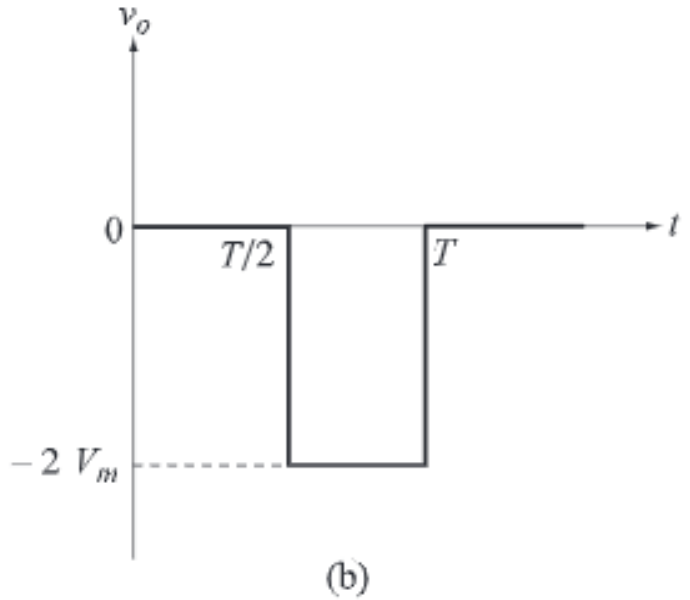
Input voltage level v_i	Output voltage level	
	Practical diode $v_o = v_i - [V_m - V_K]$	Ideal diode $v_o = v_i - V_m$
0	$-[V_m - V_K]$	$-V_m$
V_m	V_K	0
$-V_m$	$-2V_m + V_K$	$-2V_m$



Input Signal



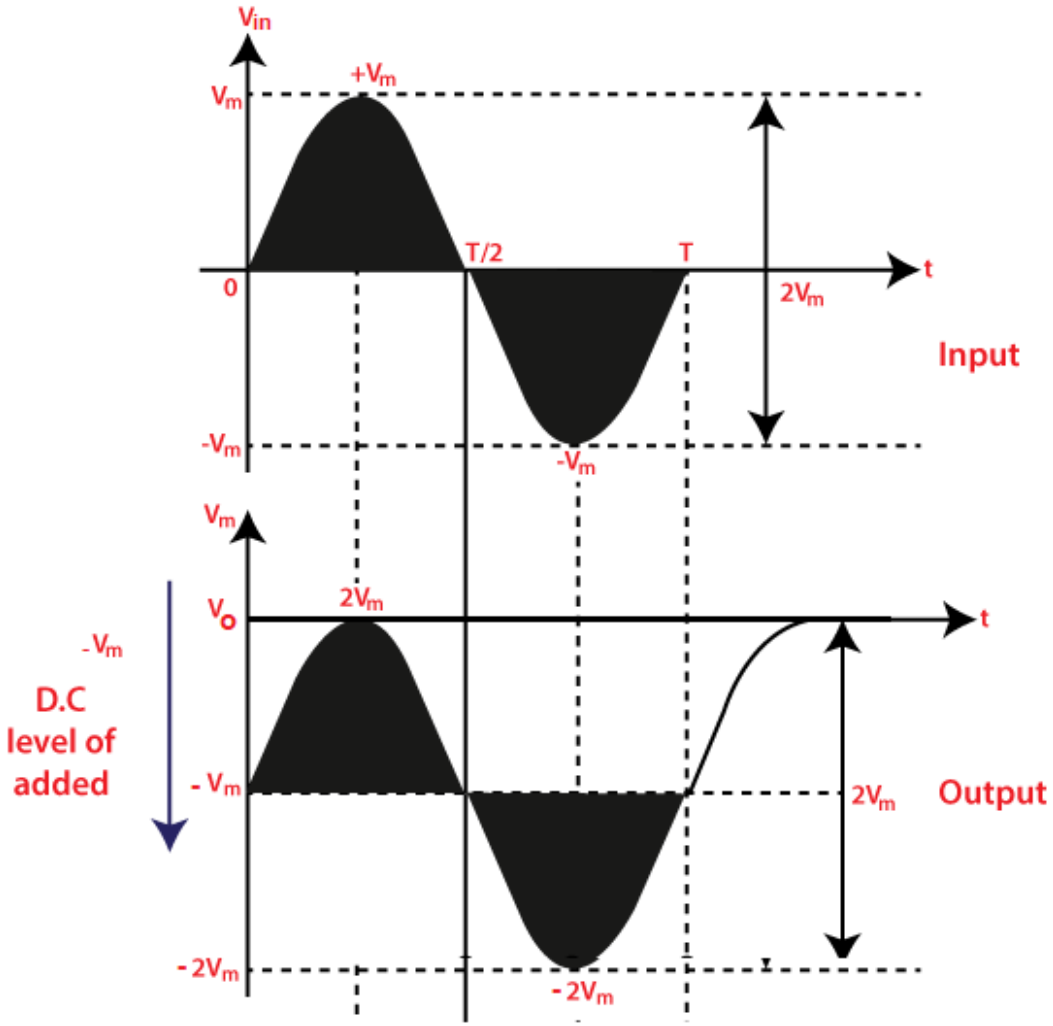
Output waveform for Practical diode



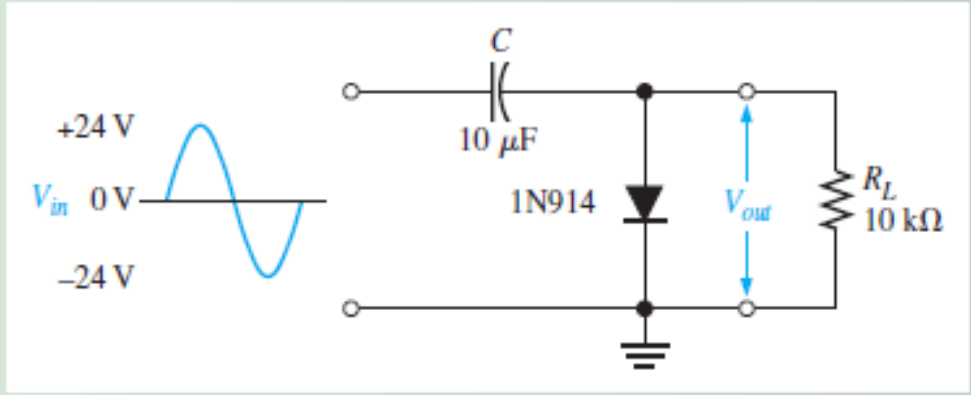
Output waveform for Ideal diode

Negative Clamper Circuits

Input voltage level v_i	*Output voltage level*	
	Practical diode $v_o = v_i - [V_m - V_K]$	*Ideal diode* $v_o = v_i - V_m$
0	$-[V_m - V_K]$	$-V_m$
V_m	V_K	0
$-V_m$	$-2V_m + V_K$	$-2V_m$



What is the output voltage that you would expect to observe across R_L in the clamping circuit of Figure 2–65? Assume that *RC* is long compared to the period to prevent significant capacitor discharge.



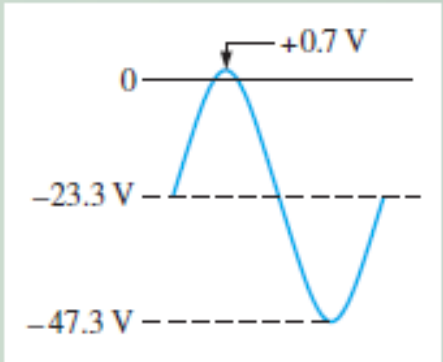
Ideally, a negative dc value equal to the input peak less the diode drop is inserted by the clamping circuit.

$$V_{DC} \cong -(V_{p(in)} - 0.7\text{ V}) = -(24\text{ V} - 0.7\text{ V}) = \mathbf{-23.3\text{ V}}$$

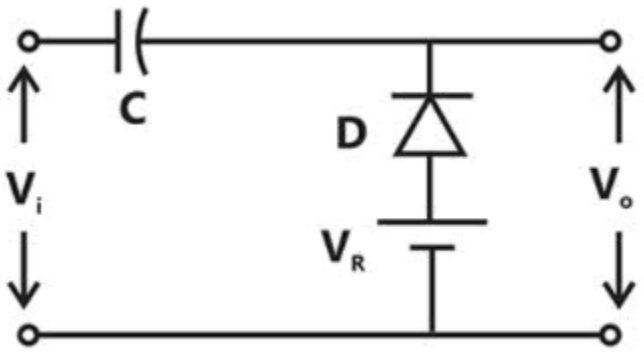
Actually, the capacitor will discharge slightly between peaks, and, as a result, the output voltage will have an average value of slightly less than that calculated above. The output waveform goes to approximately +0.7 V, as shown in Figure 2–66.

▶ **FIGURE 2–66**

Output waveform across R_L for Figure 2–65.



Addition of Battery in Clamper (Biased Positive Clamping Circuit)



When $V_R = 0$

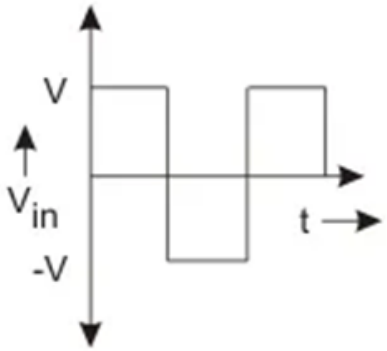
-ve peak is shifted to 0

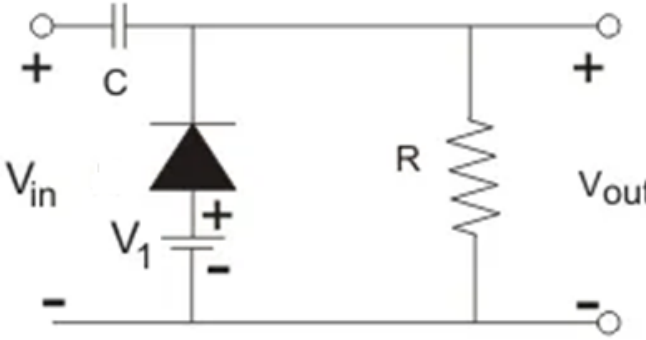
+ve peak is shifted to $2V_m$

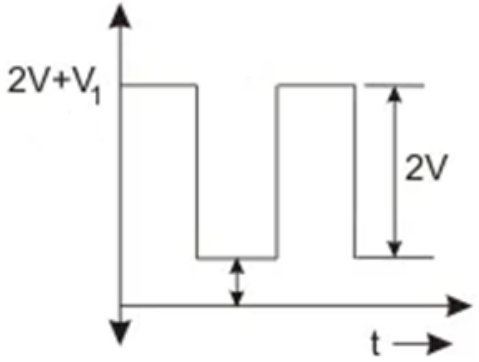
When $V_R \neq 0$

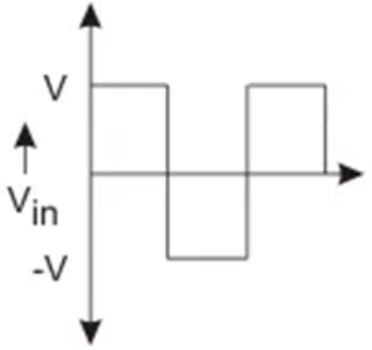
-Ve peak is shifted to V_R

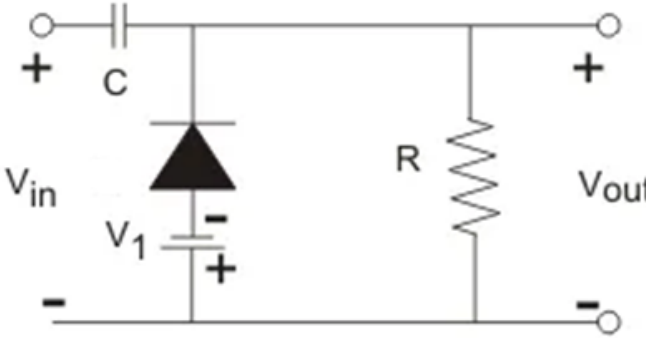
+ve peak is shifted to $2V_m + V_R$











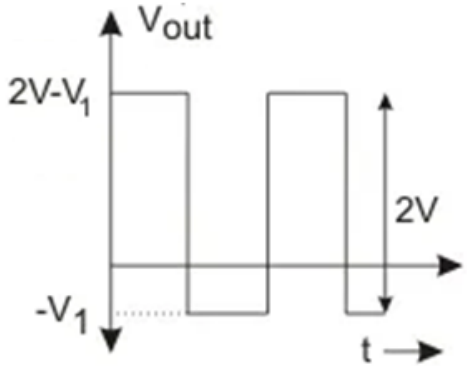
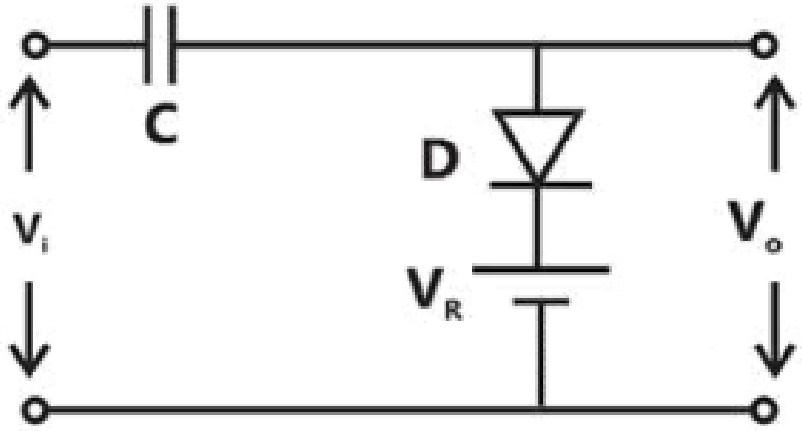
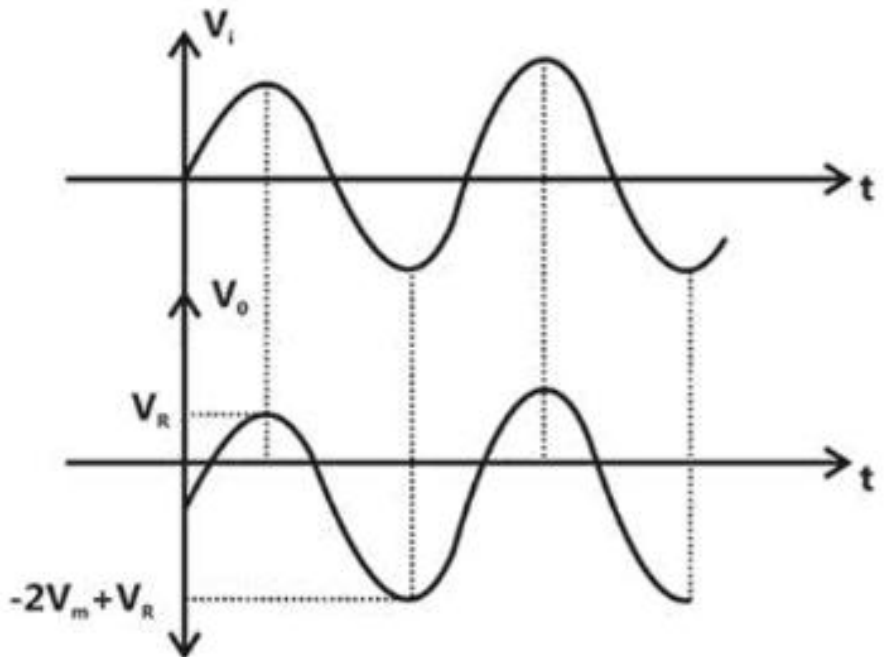


Figure 4

Biased Negative Clamping circuit





When $V_R = 0$

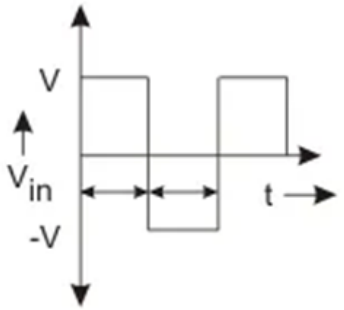
+ve peak is shifted to 0

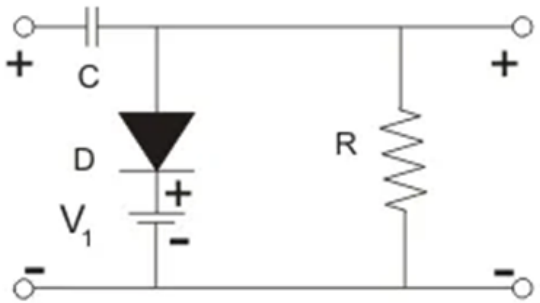
-ve peak is shifted to $-2V_m$

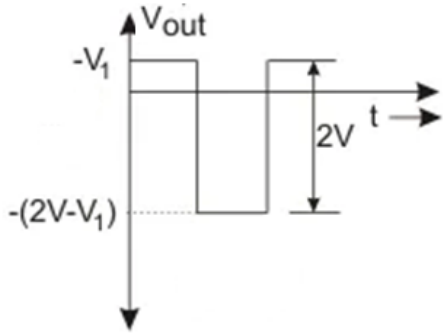
When $V_R \neq 0$

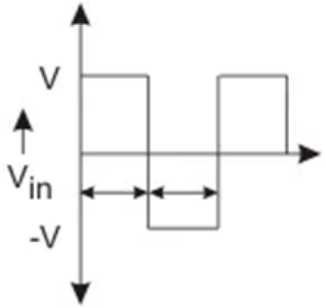
+ve peak is shifted to V_R

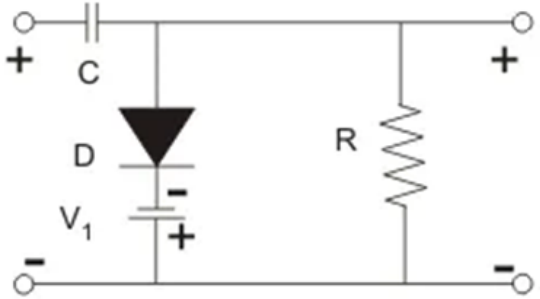
-ve peak is shifted to $-2\ V_m + V_R$











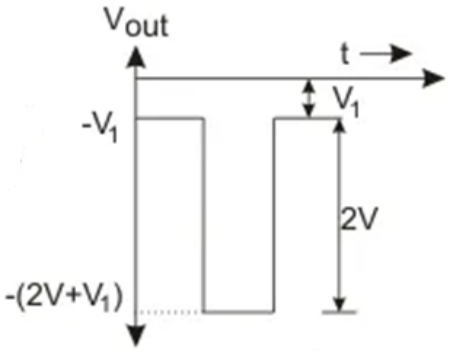


Figure 5

Applications

Clippers

1. Used for the generation and shaping of waveforms
2. Used for the protection of circuits from spikes
3. Used for amplitude restorers
4. Used as voltage limiters
5. Used in television circuits
6. Used in FM transmitters

Clampers

1. Used as direct current restorers
2. Used to remove distortions
3. Used as voltage multipliers
4. Used for the protection of amplifiers
5. Used as test equipment
6. Used as base-line stabilizer

A T M E

College of Engineering

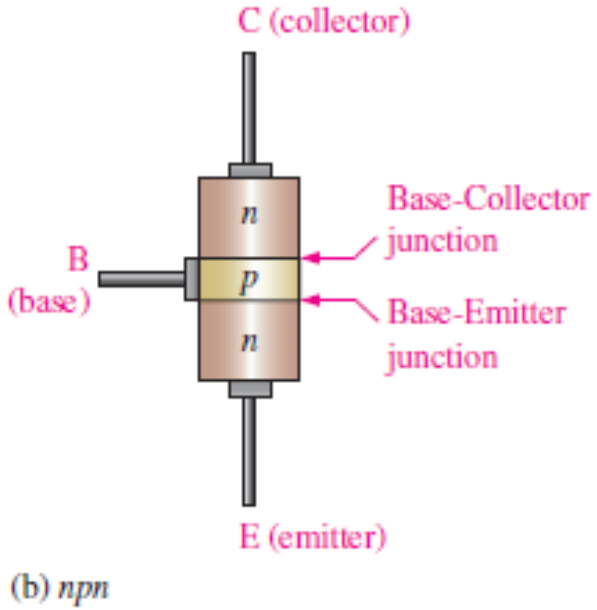
Department of EEE
Emitting Elite Energy

Analog Electronic Circuits
Module-I: Transistor Biasing

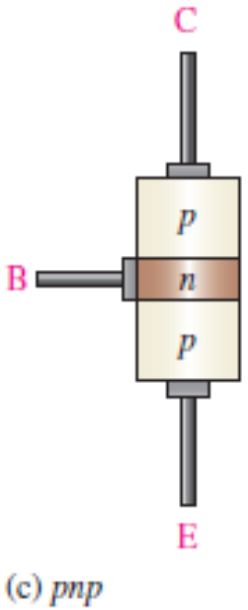
Transistor Biasing

Bipolar Junction Transistor (BJT)

The **BJT** is constructed with three doped semiconductor regions separated by two pn junctions



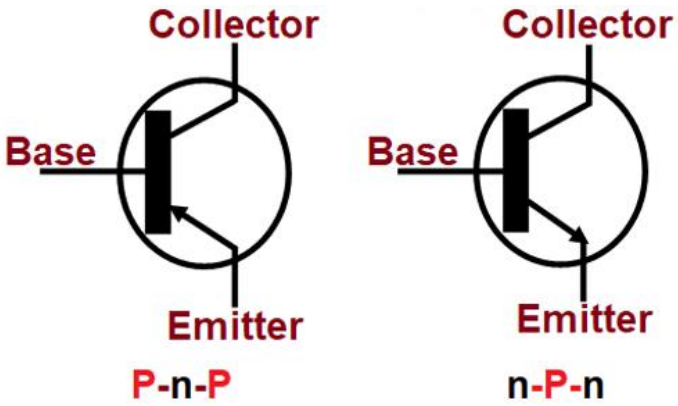
(b) *npn*



(c) *pnp*

Junctions of Transistor

- ❑ **Collector – Base Junction**
- ❑ **Base- Emitter Junction**



Symbols.

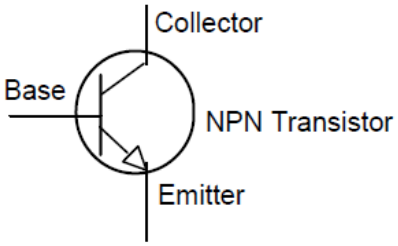
Operating regions of BJT

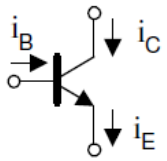
Operating Regions	Emitter-Base Junction	Collector-Base Junction	Function
Cut-off region	**Reverse Biased**	**Reverse Biased**	**OFF Switch**
Active region	**Forward Biased**	**Reverse Biased**	**Amplifier**
Saturation region	**Forward Biased**	**Forward Biased**	**ON Switch**

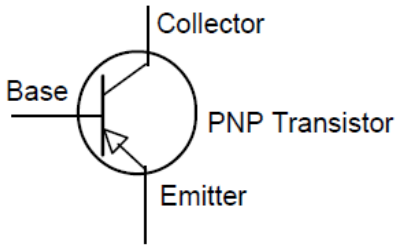
The arrow on the emitter inside the transistor symbols points in the direction of conventional current

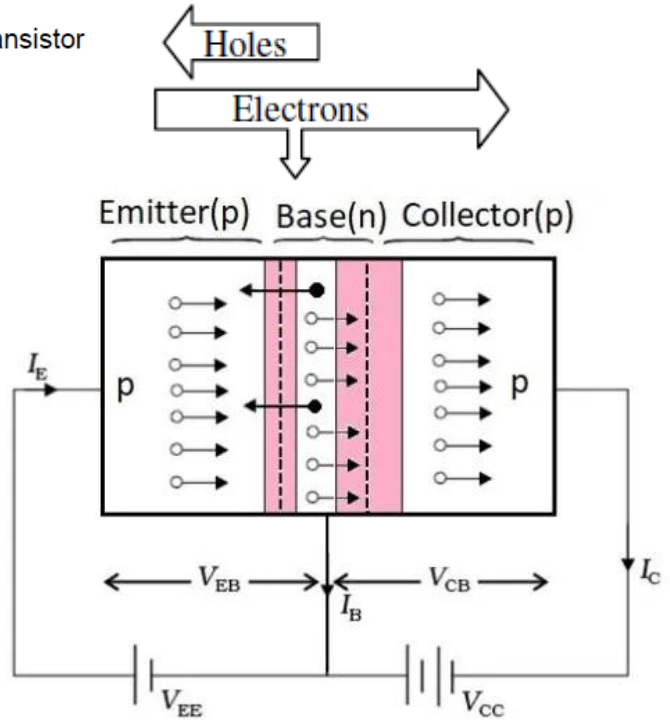
Bipolar Junction Transistor: BJT is a three terminal component, which is constructed with three doped semiconductor regions separated by two p-n junctions; the three regions are Emitter (E), Base (B) and collector(C). There are two types of BJT, such as a) NPN b) PNP

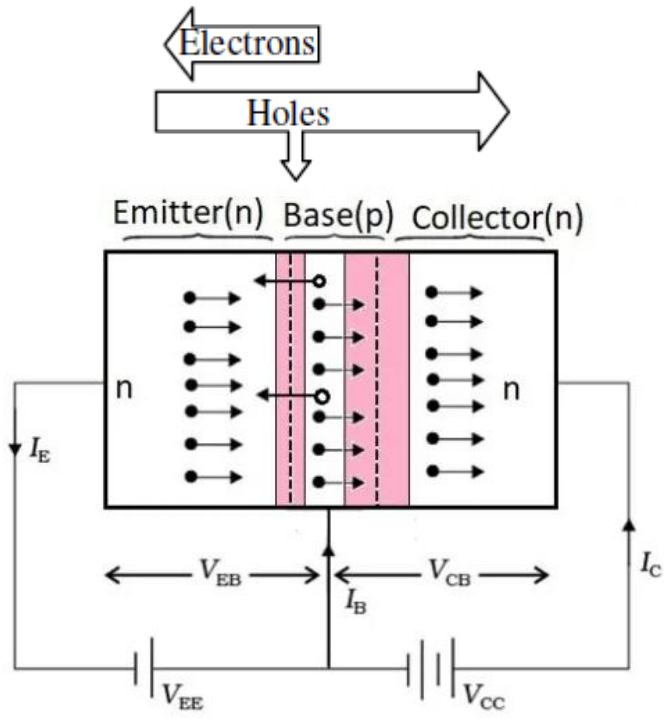
NPN transistor has N-type emitter & collector and a P-type base, while PNP has P-type emitter & collector and a N-type base as shown in figure 1(a) and (b).



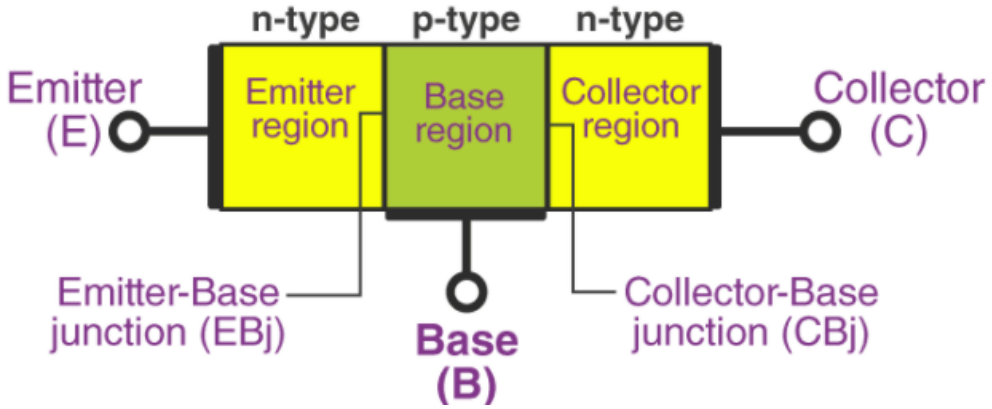


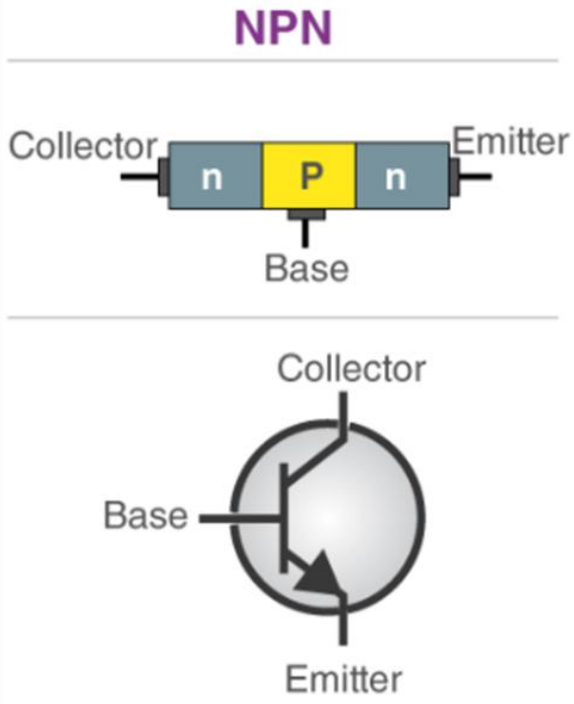


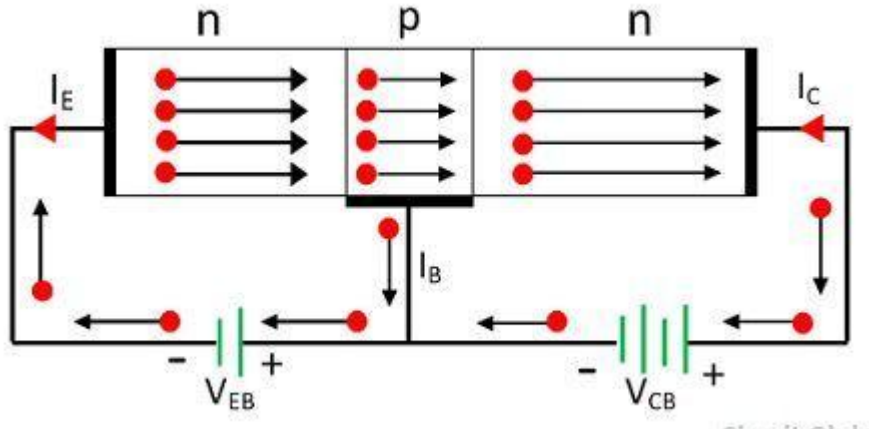


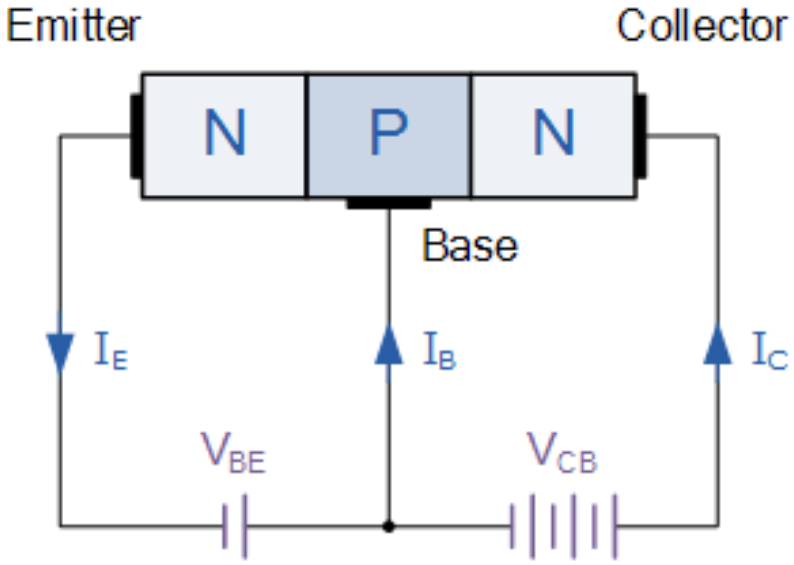


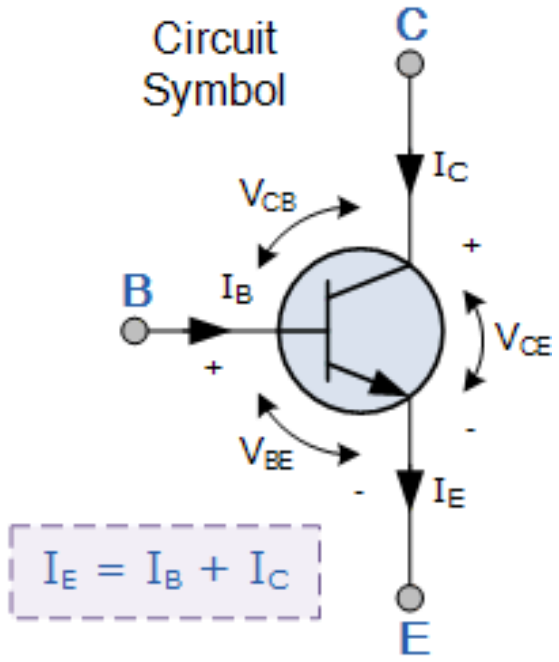
hole
electron











For a bipolar transistor to conduct correctly,

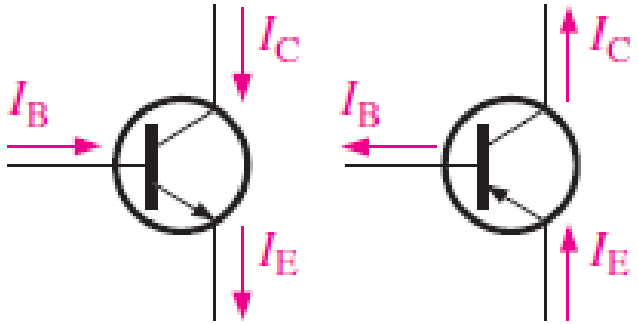
Base- Emitter Junction is to Forward Biased

Collector – Base Junction as to Reverse Biased

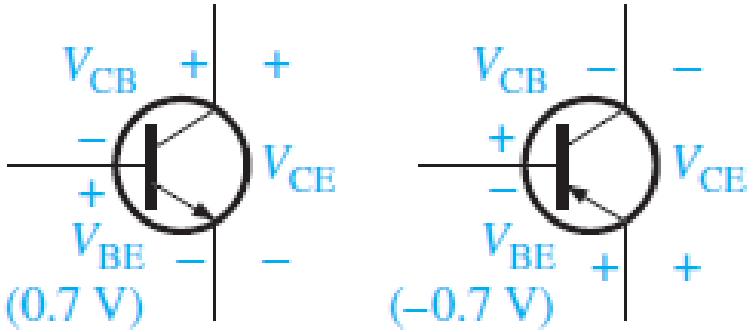
Bipolar NPN transistor the Collector must always more positive with respect to both the Base and the Emitter terminals

Ib provides the input and Ic provides the output

CURRENTS AND VOLTAGES



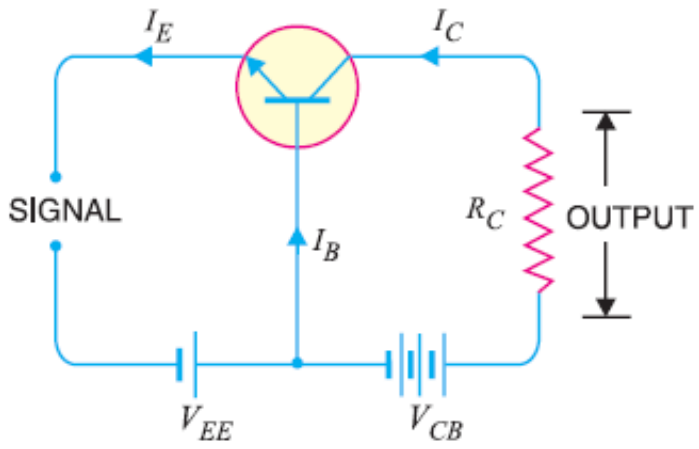
$$I_E = I_C + I_B$$



- Transistor has Three basic configurations:
  - Common Emitter Configuration – has both Current and Voltage Gain.
  - Common Base Configuration – has Voltage Gain but no Current Gain.
  - Common Collector Configuration – has Current Gain but no Voltage Gain.

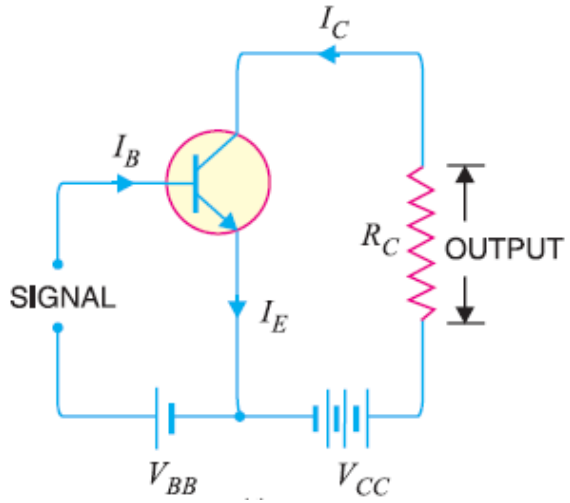
- Bipolar Transistors have the ability to operate within three different regions:
  - Active Region – the transistor operates as an amplifier and Ic = β.Ib
  - Saturation – the transistor is "Fully-ON" operating as a switch
  - Cut-off – the transistor is "Fully-OFF" operating as a switch

Common Base Connection



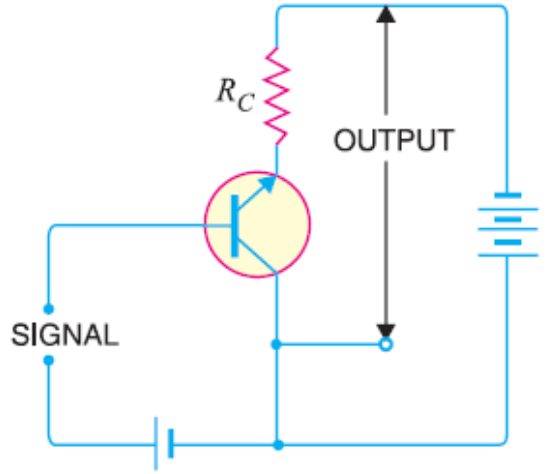
common base npn transistor circuit

Common Emitter Connection

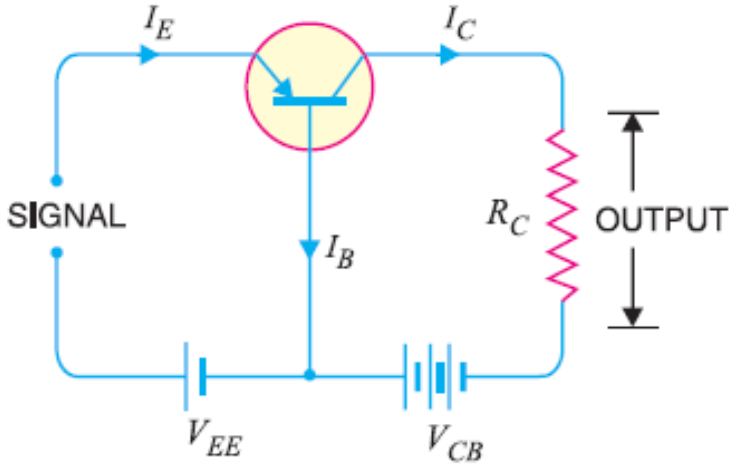


common emitter npn transistor circuit

Common Collector Connection

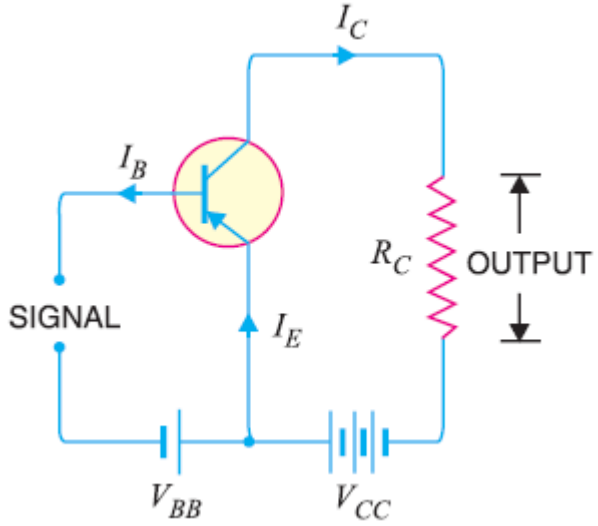


common collector npn transistor circuit



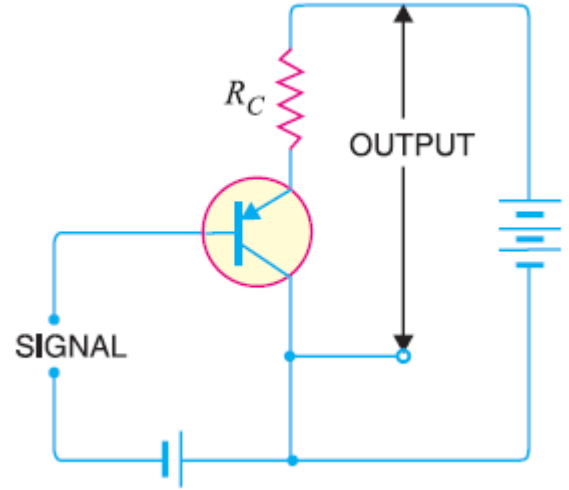
common base pnp transistor circuit

In a common base configuration, emitter current I_E is the input current and collector current I_C is the output current.



common emitter pnp transistor circuit

input is applied between base and emitter and output is taken between collector and emitter

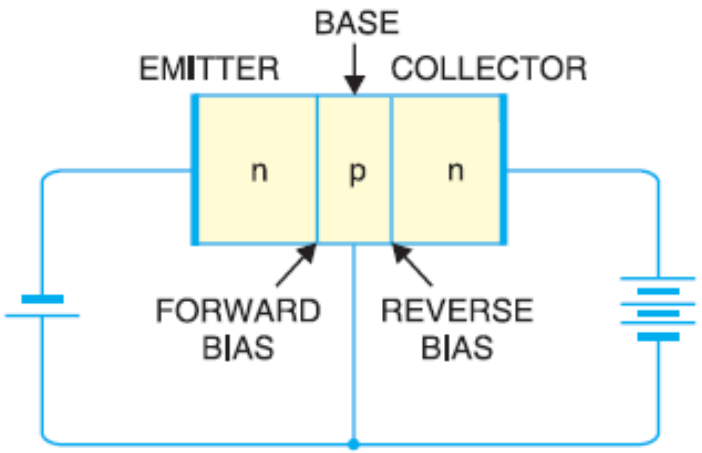


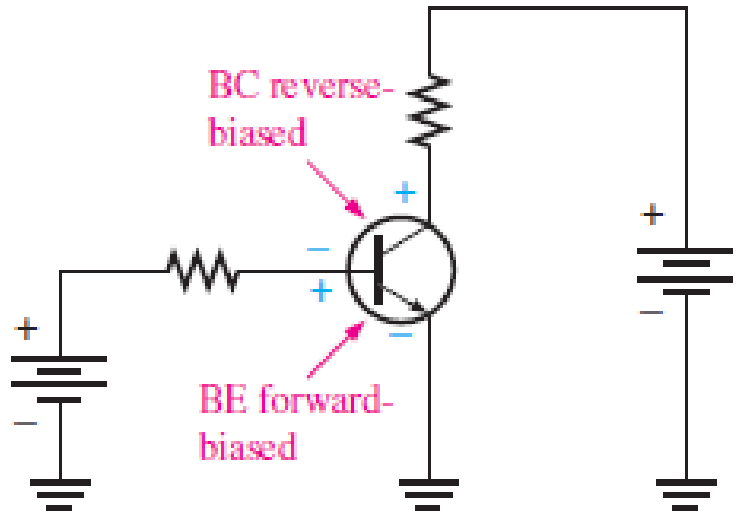
common collector pnp circuit

input is applied between the base and collector and the output is taken between the emitter and collector terminals

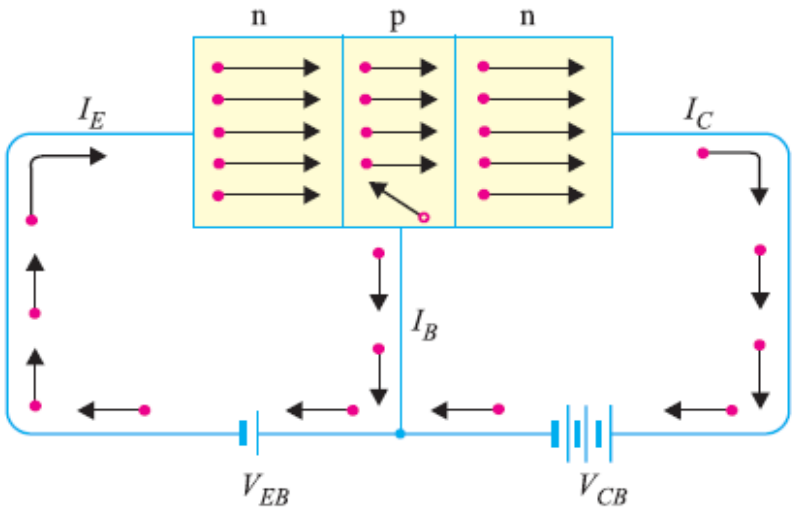
Biasing Arrangement

NPN Transistor Working

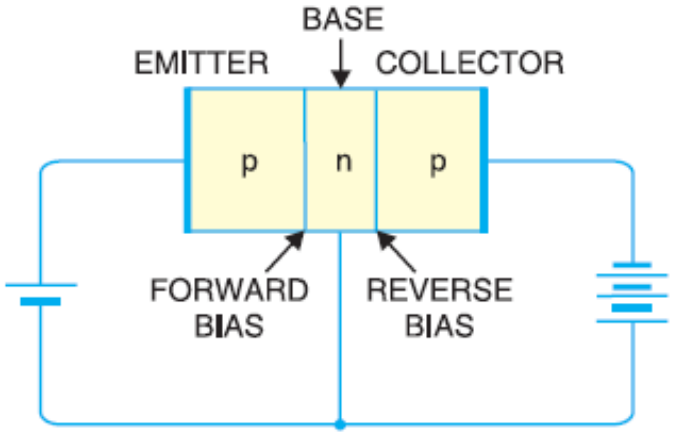


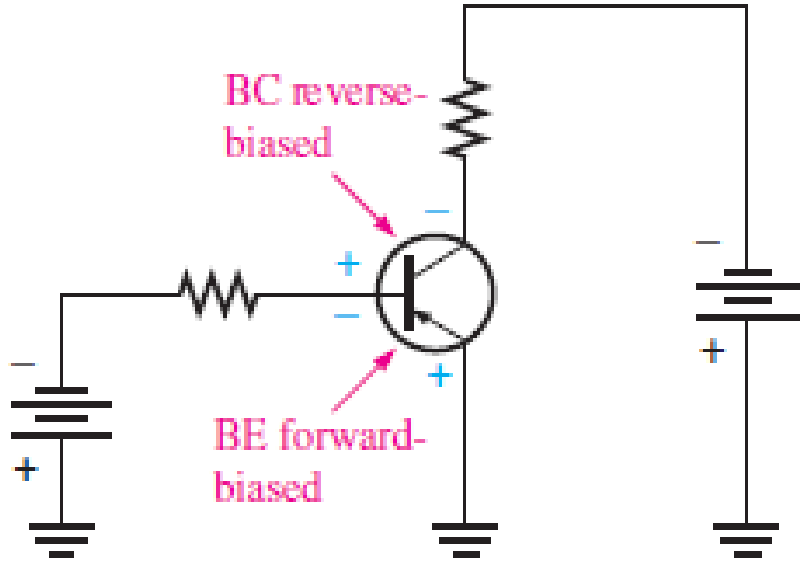


(a) *npn*

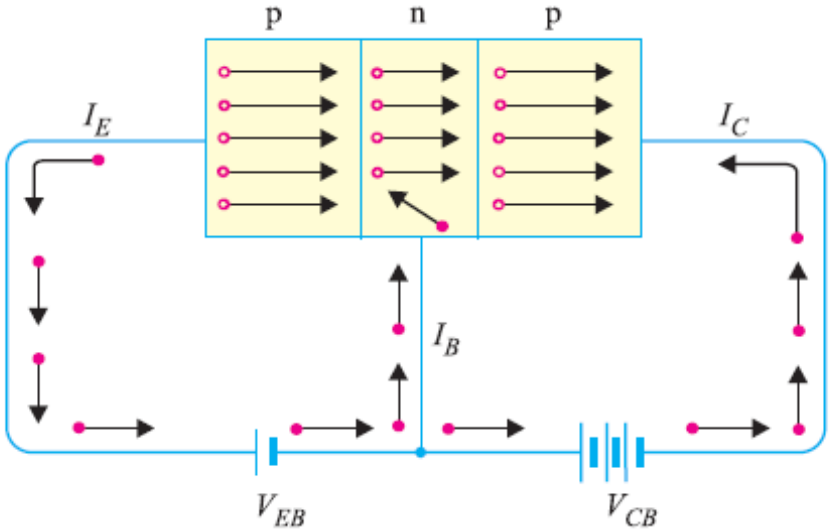


PNP Transistor Working





(b) *pnp*

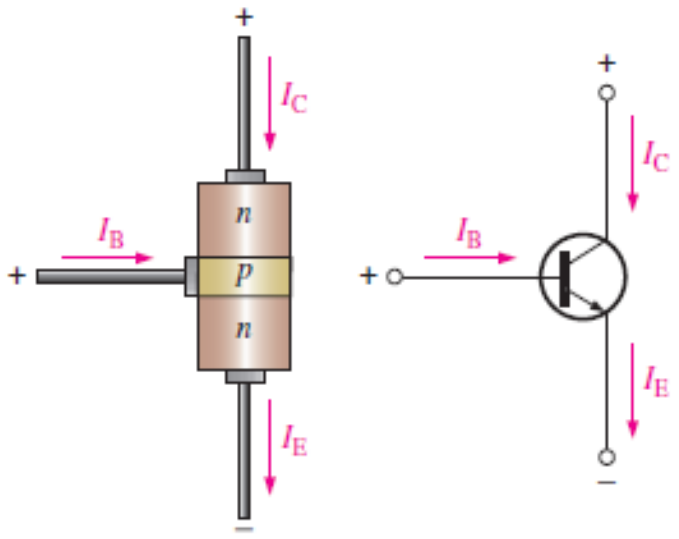


Biasing Arrangement & **Transistor Currents**

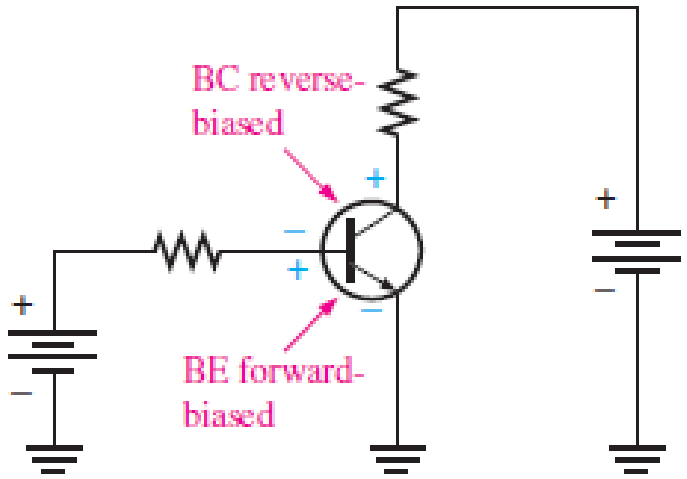
NPN Transistor Working

$I_E = I_C + I_B$

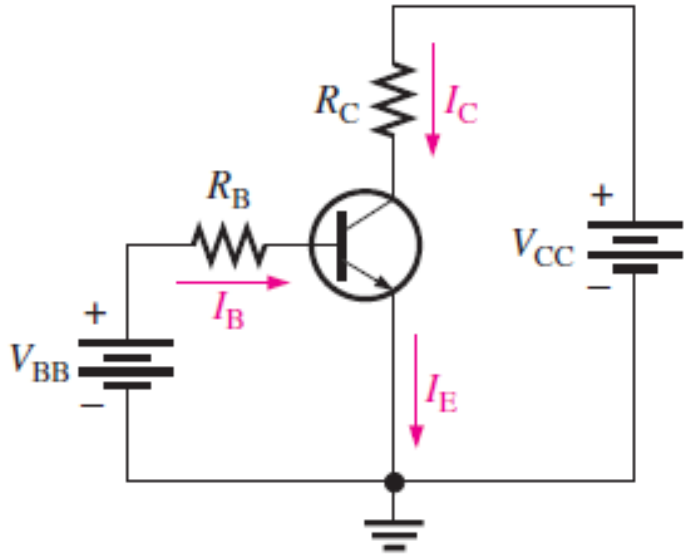
I_B is very small compared to I_E or I_C. The capital-letter subscripts indicate dc values. Lowercase italic subscript Indicate AC quantities *Ib, Ic, and Ie*



(a) *npn*

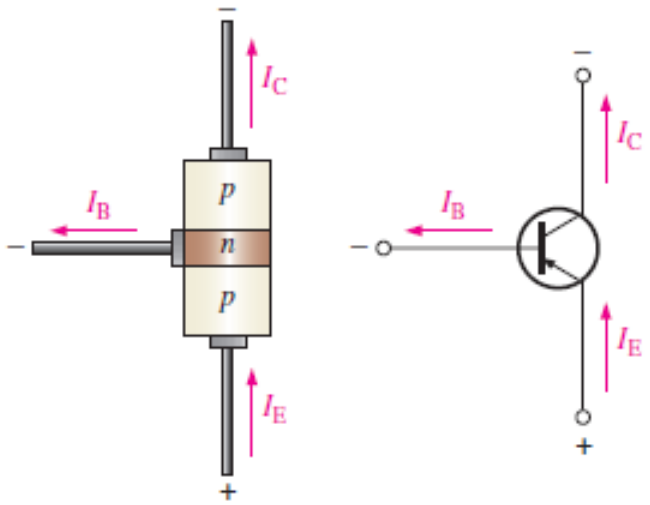


(a) *npn*

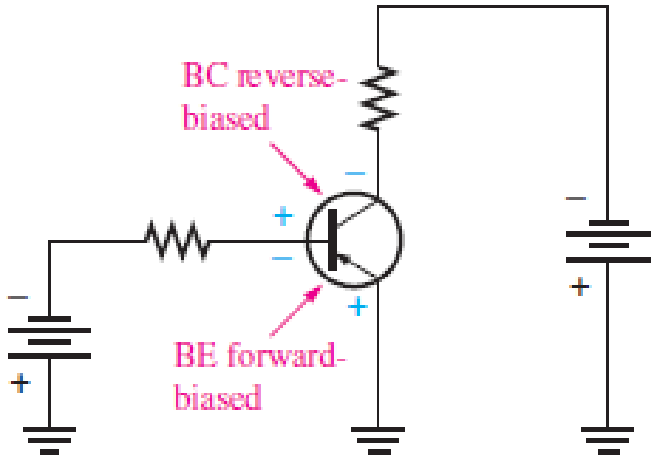


(a) *npn*

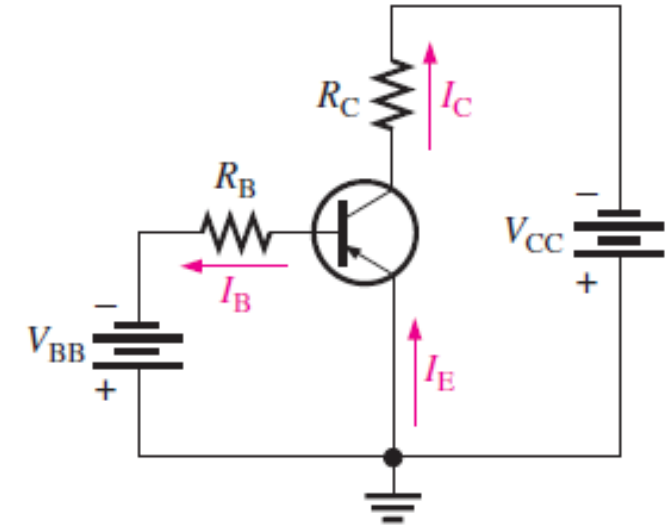
PNP Transistor Working



(b) *pnp*



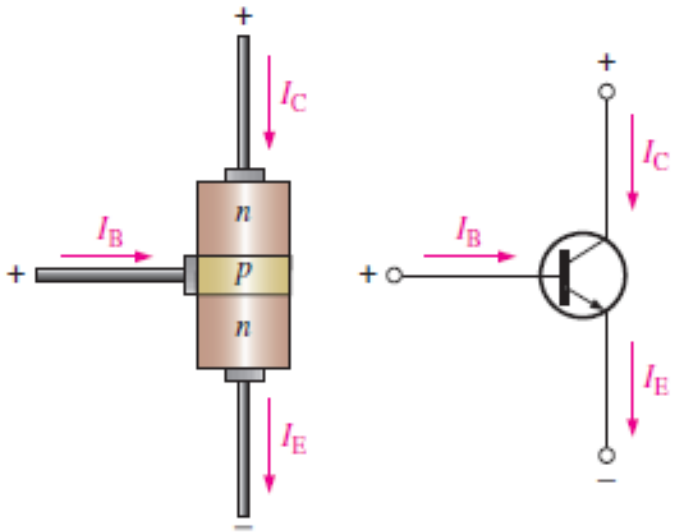
(b) *pnp*

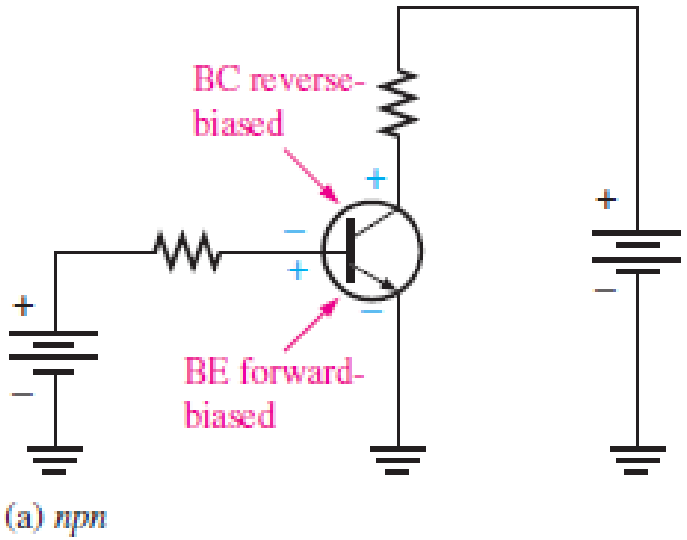


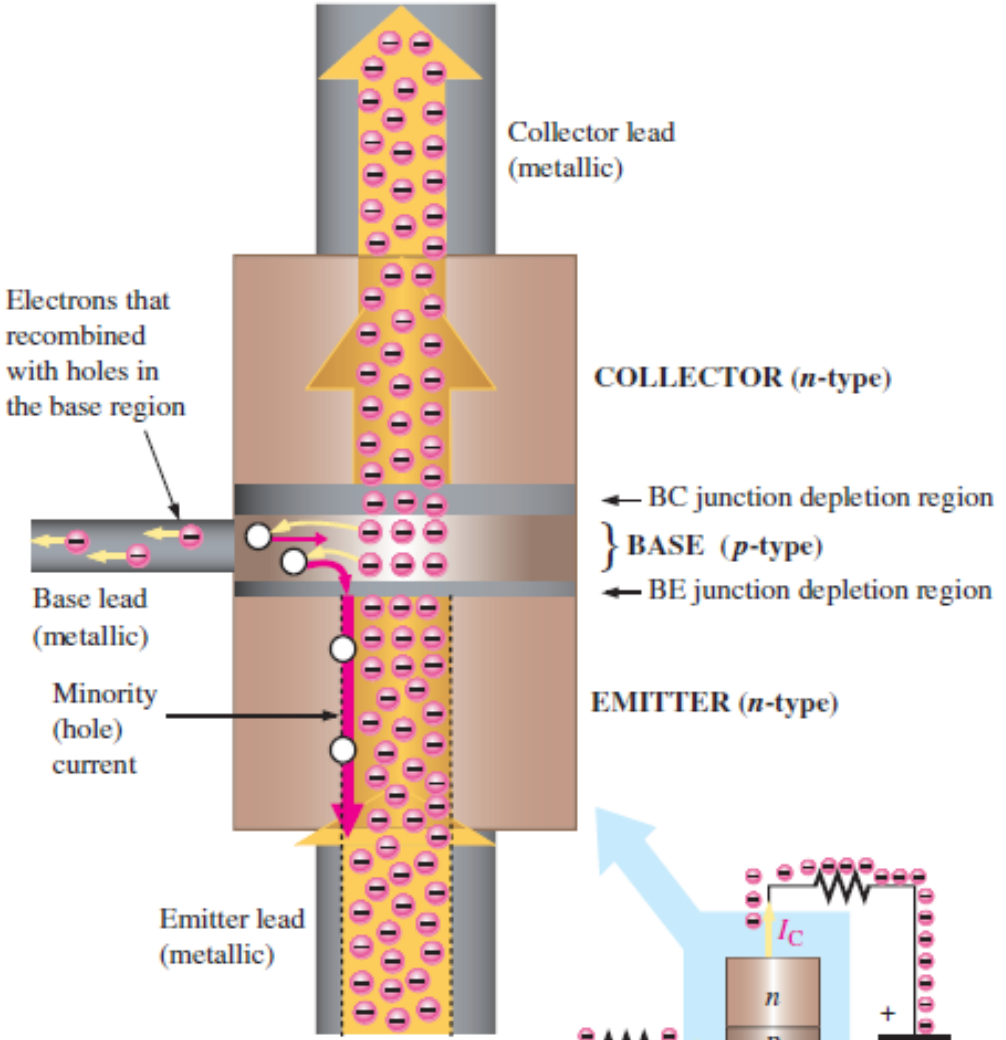
(b) *pnp*

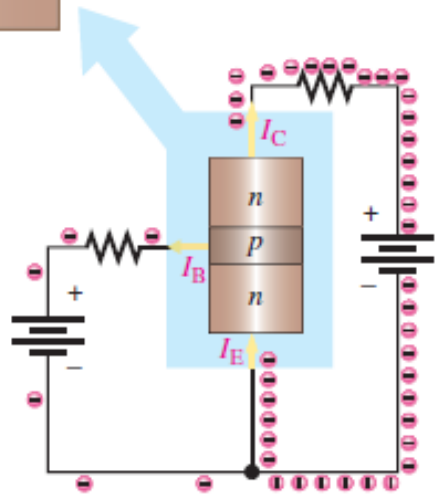
BJT operation showing electron flow

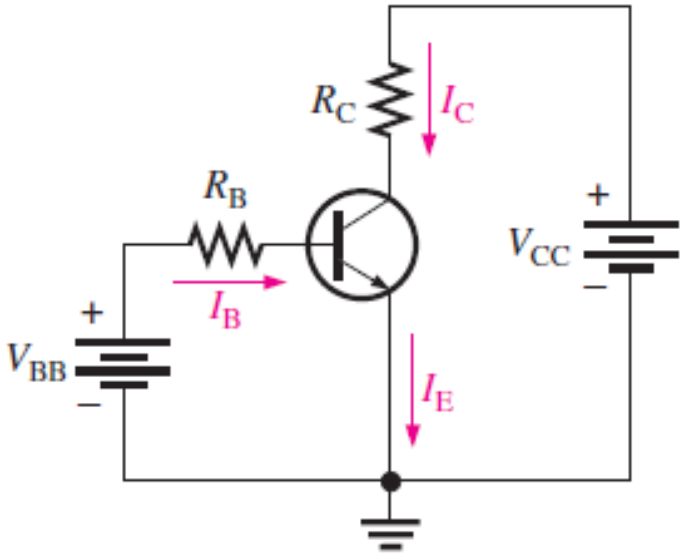
NPN Transistor Working











Transistor Biasing

Biasing Configurations of BJT

1. **Fixed bias configuration**
2. **Emitter stabilized bias configuration**
3. **Voltage divider bias configuration**

Parameters of BJT

1. **Gain**
2. **Input Impedance**
3. **Output Impedance**

DC current gain (B_{DC}) and DC Alpha (A_{DC})

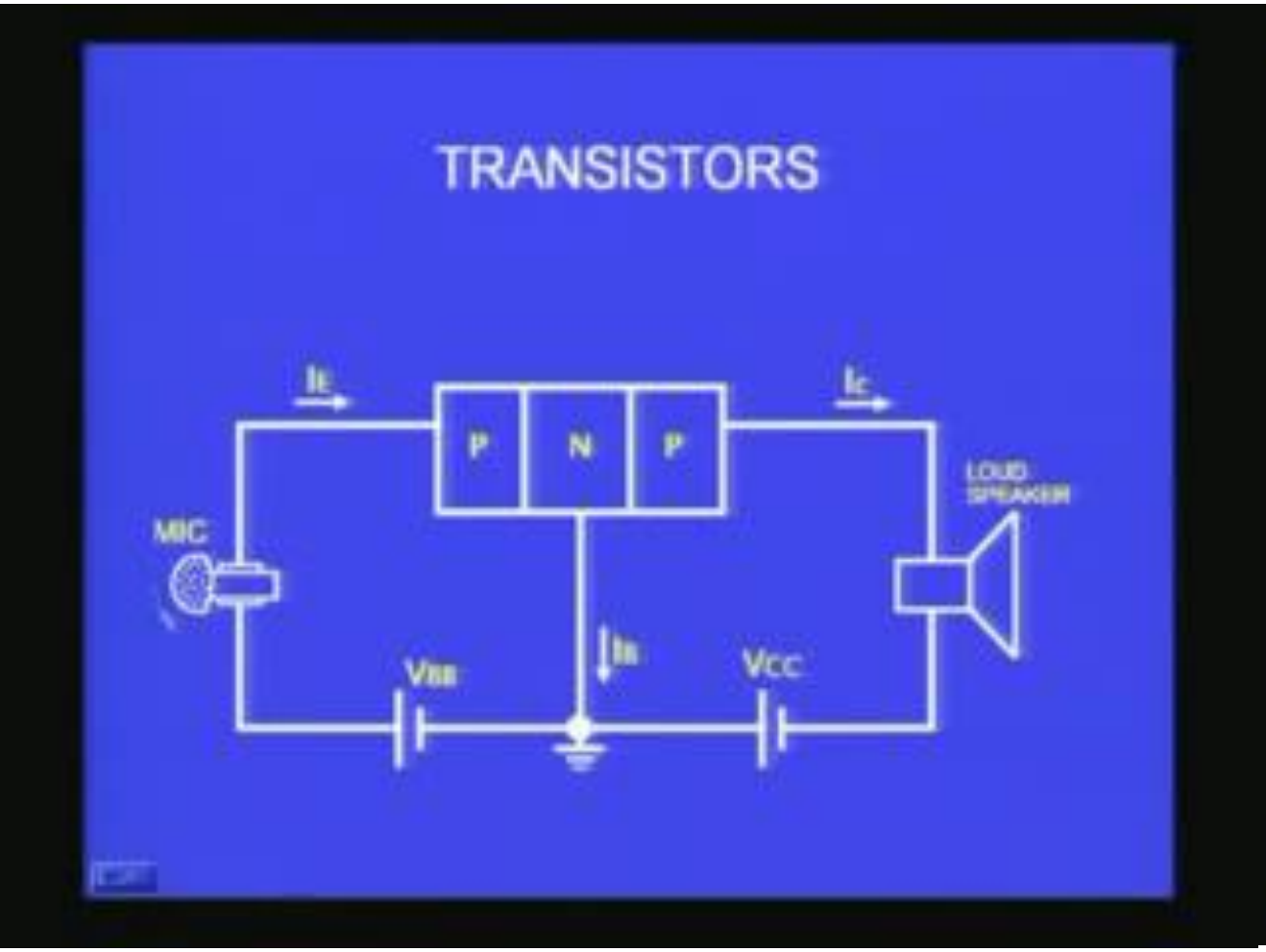
The dc current **gain** of a transistor is the ratio of the dc collector current (I_C) to the dc base current (I_B) and is designated dc **beta** (β_{DC}).

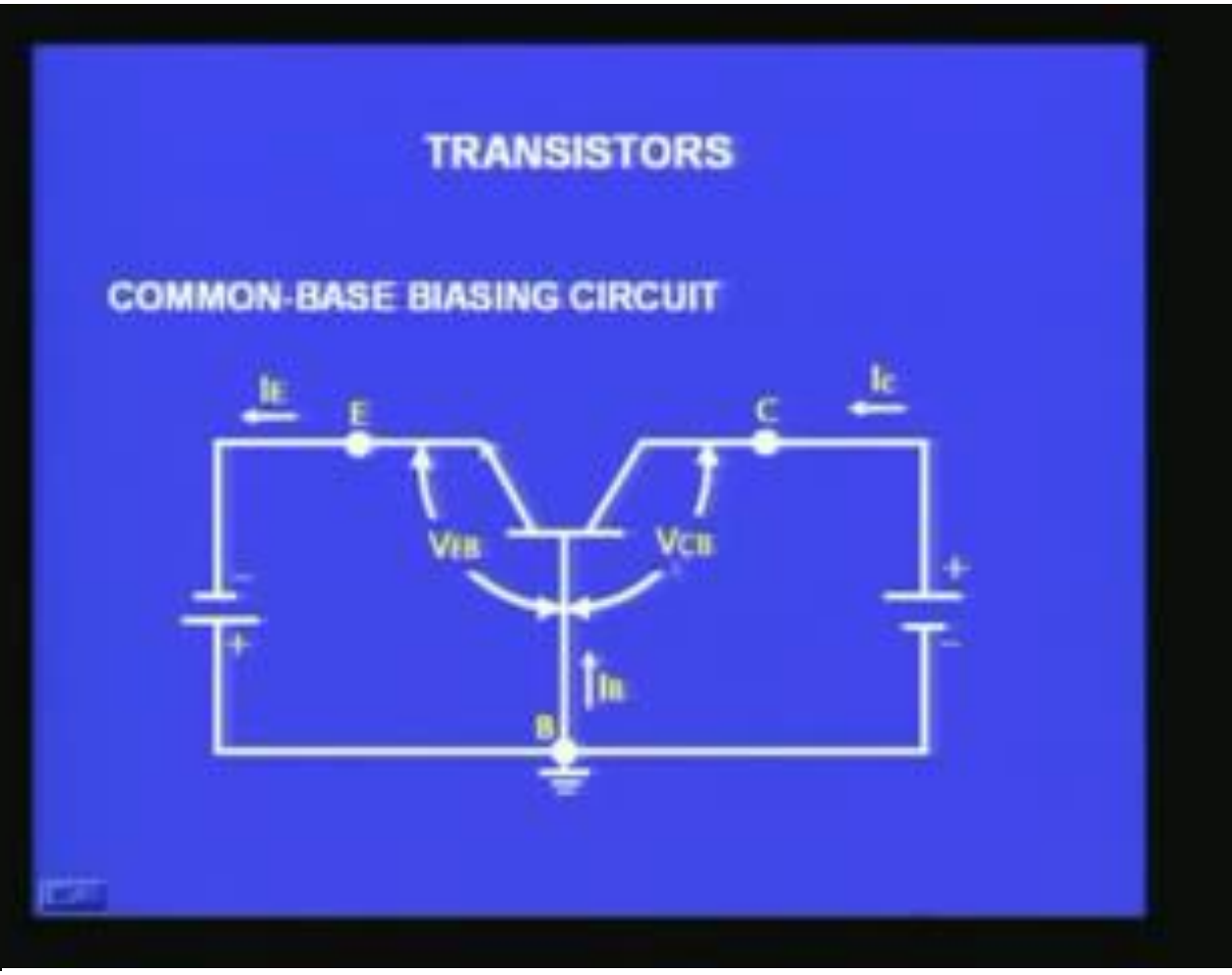
The ratio of the dc collector current (I_C) to the dc emitter current (I_E) is the dc **alpha** (α_{DC}). The alpha is a less-used parameter than beta in transistor circuits

The biasing of a bipolar junction transistor is to establish the desired value of collector to emitter voltage V_{CE} and Collector current I_C.

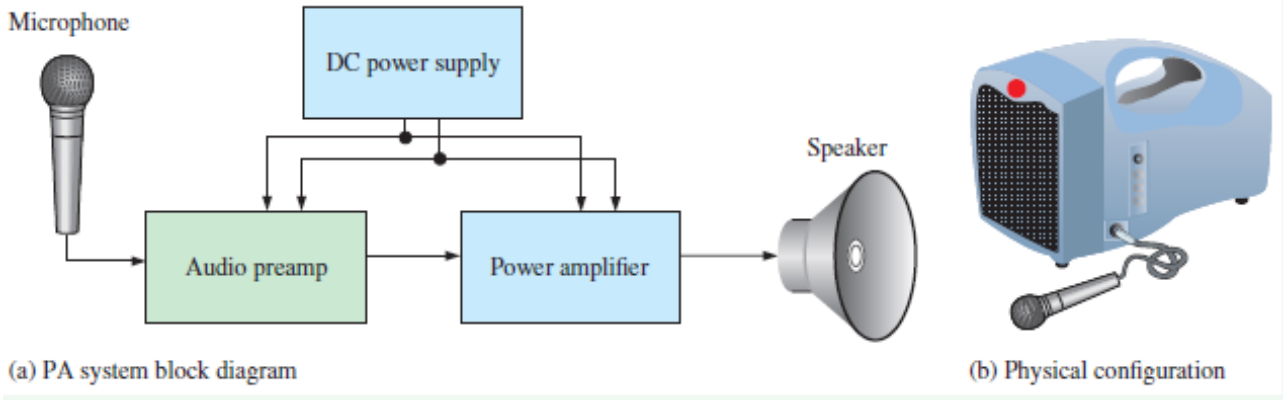
The values of V_{CE} and I_C together are known as operating point or quiescent point (Q-point)

AMPLIFICATION

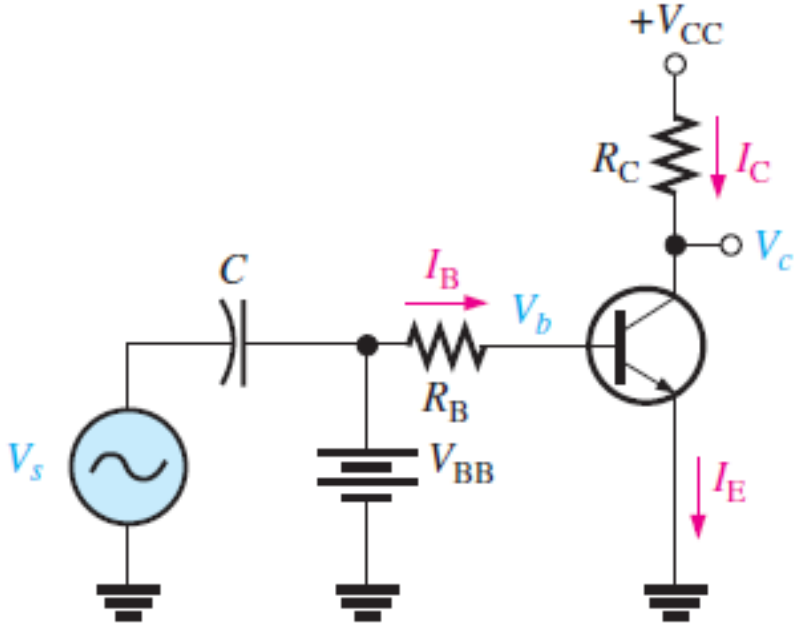




AMPLIFICATION



The public address system.



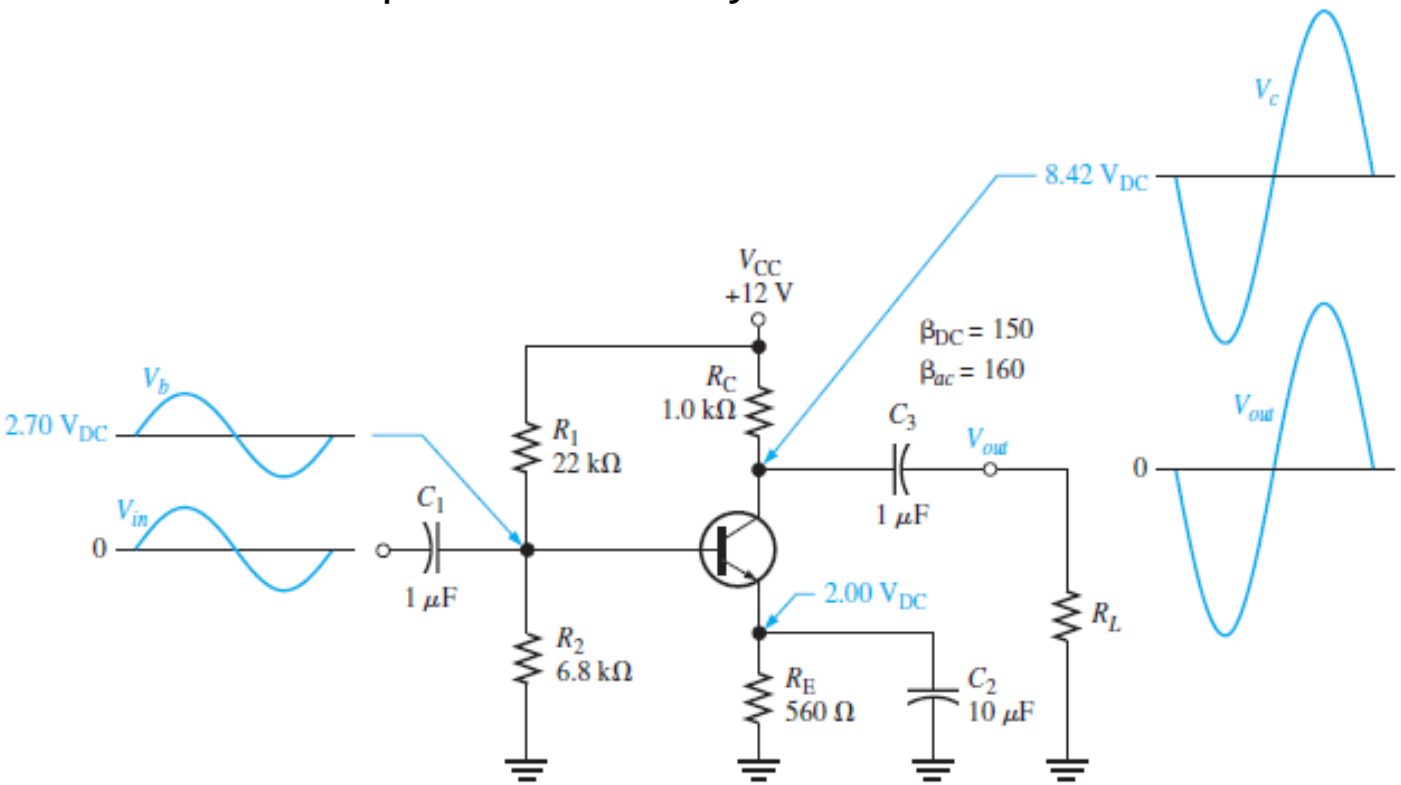
- DC current gain

$$I_C = \beta_{DC} I_B$$

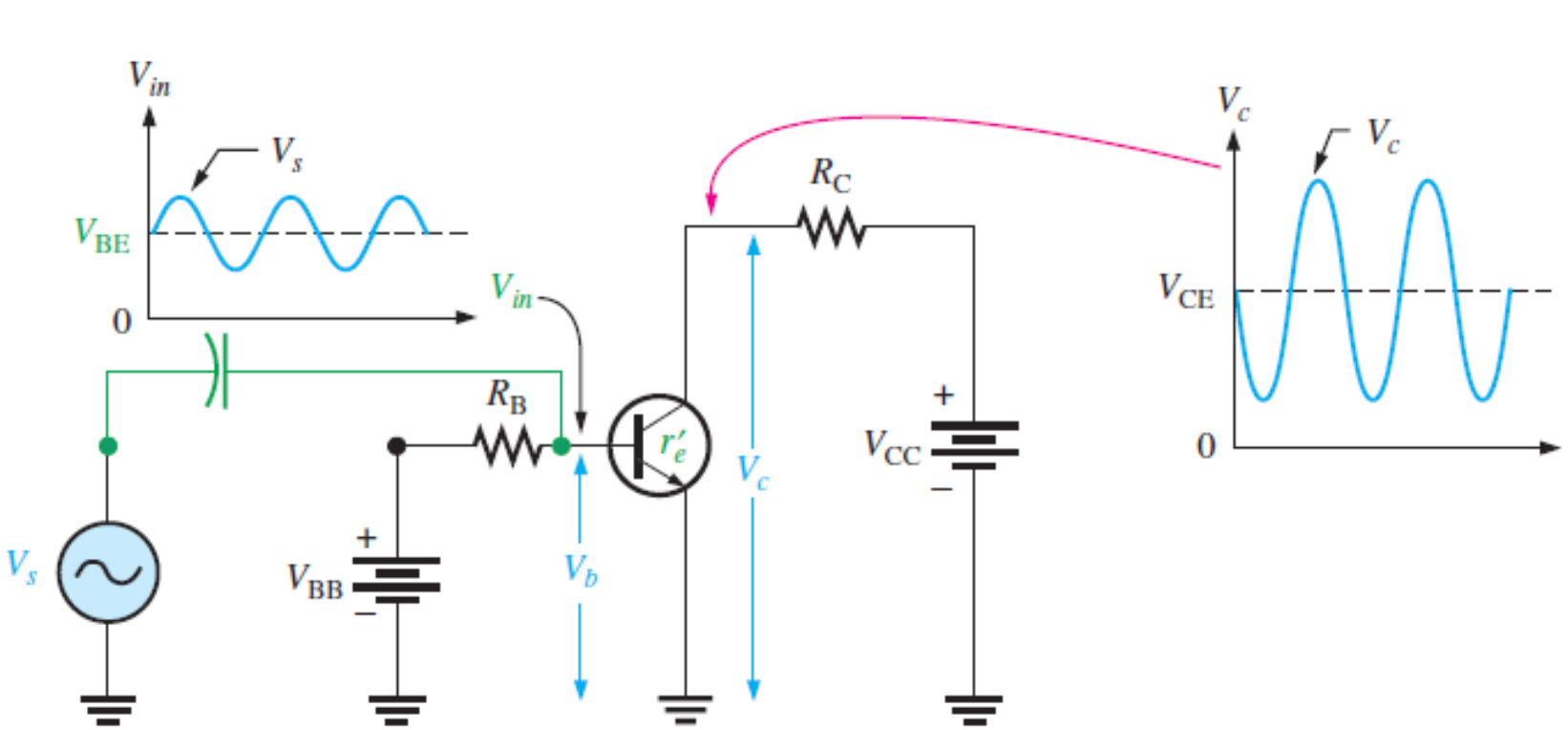
- AC voltage gain

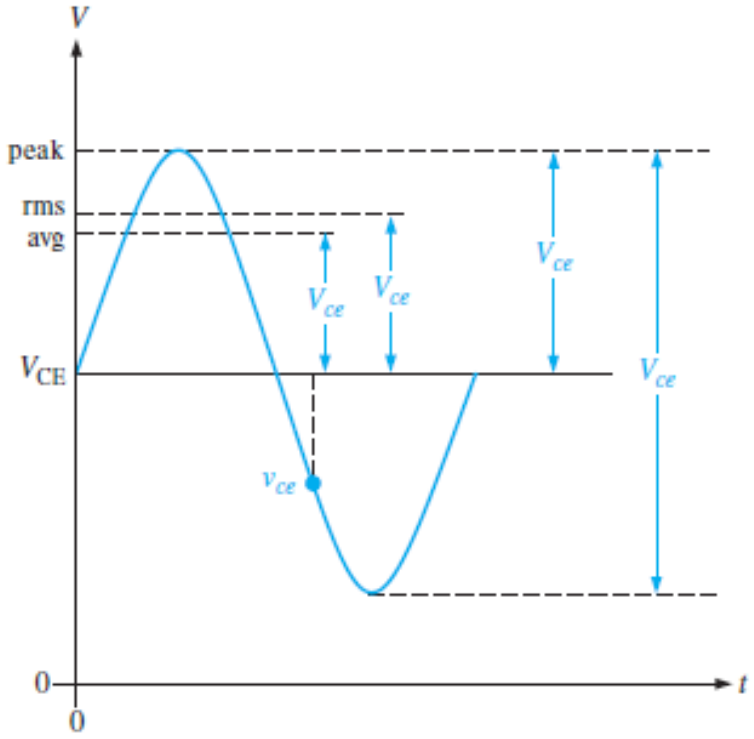
$$A_v = \frac{V_c}{V_b} = \frac{R_C}{r'_e}$$

BE junction forward-biased
BC junction reverse-biased



Voltage Amplification

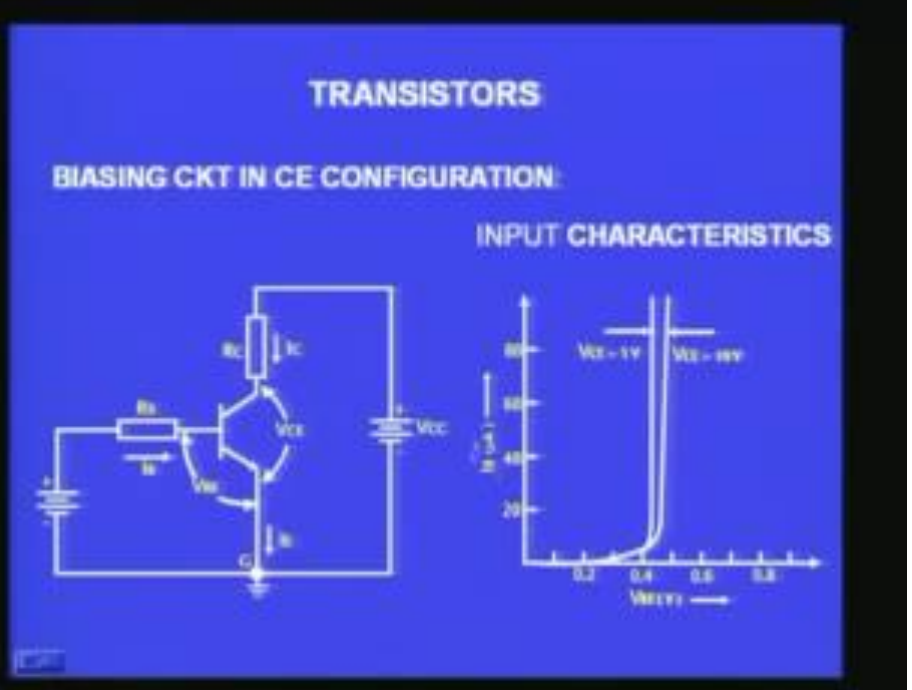


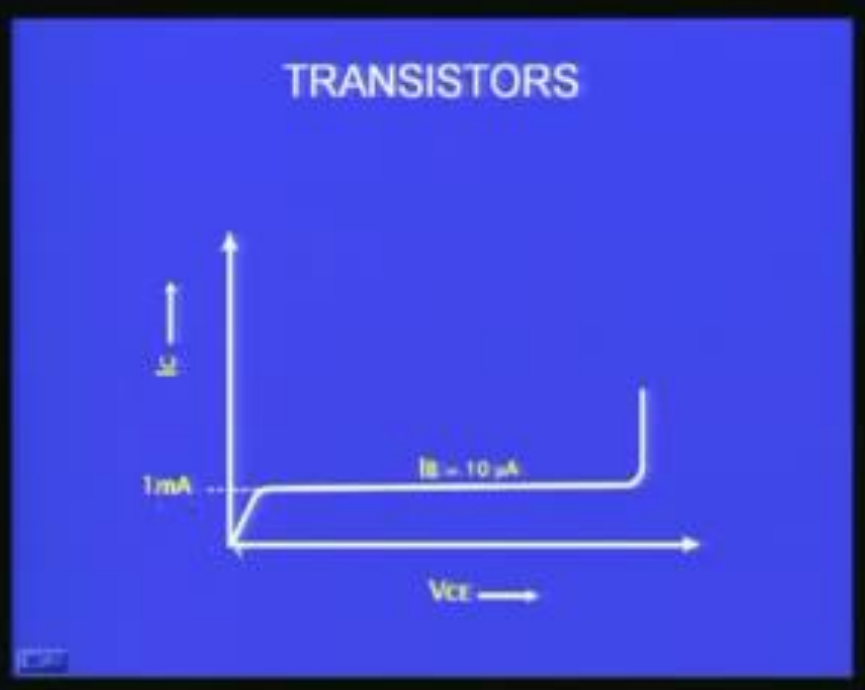


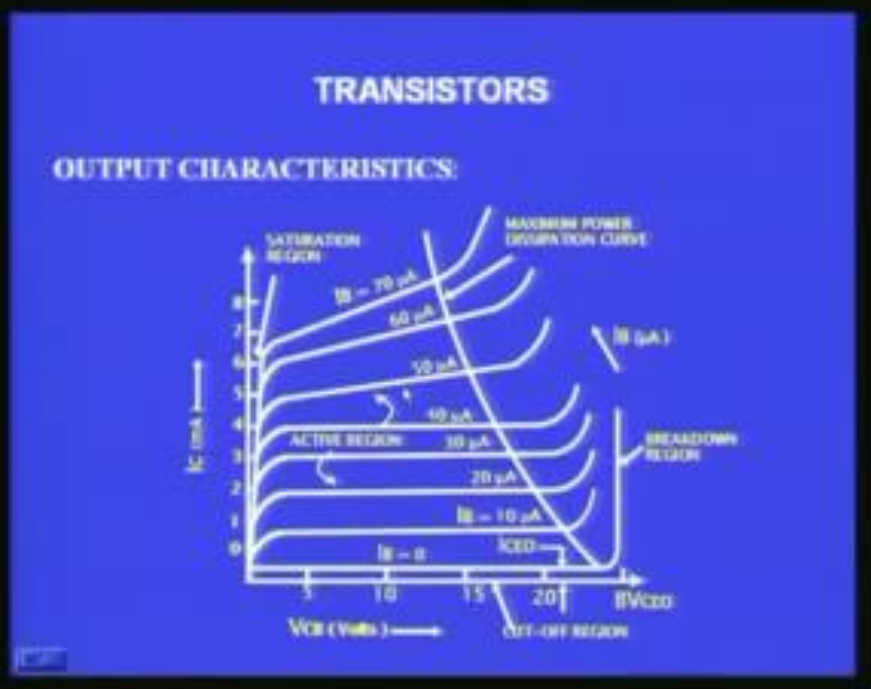
Basic transistor amplifier circuit with ac source voltage Vs and dc bias voltage VBB superimposed.

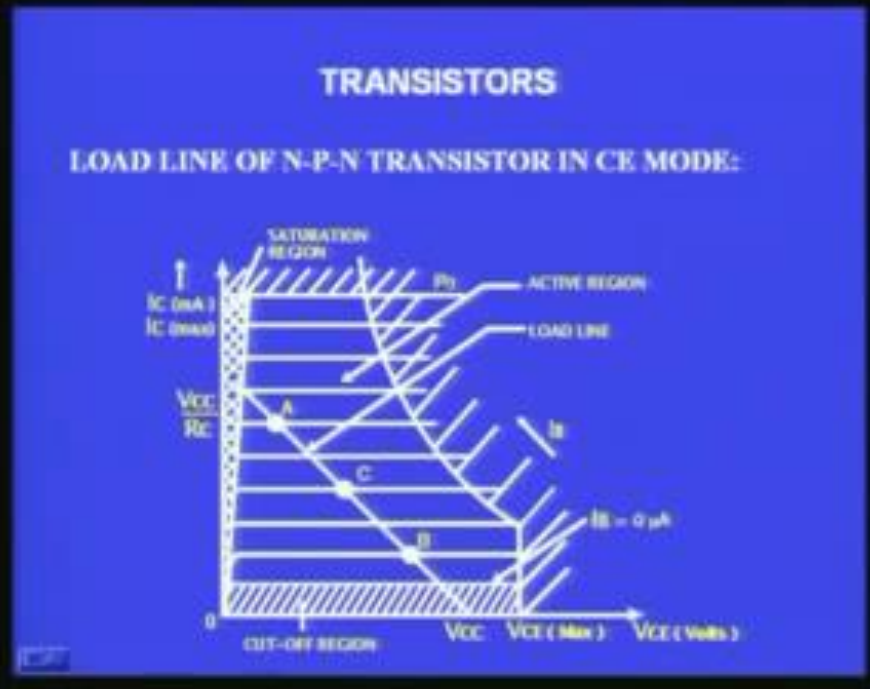
IB is very small compared to IE or IC. The capital-letter subscripts indicate dc values.
Lowercase italic subscript Indicate AC quantities *Ib, Ic, and Ie*

Input and Output Characteristics Curves of a Typical Bipolar Transistor

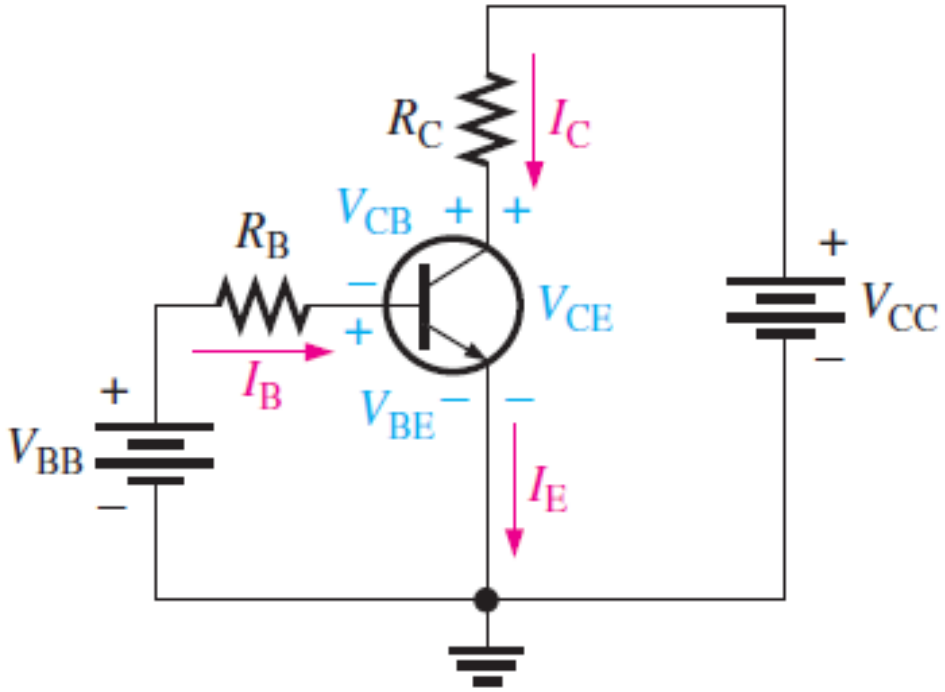








BJT Circuit Analysis



I_B: dc base current
I_E: dc emitter current
I_C: dc collector current
V_{BE}: dc voltage at base with respect to emitter
V_{CB}: dc voltage at collector with respect to base
V_{CE}: dc voltage at collector with respect to emitter
VBB : dc base-bias voltage source, forward-biases the base-emitter junction
VCC: collector-bias voltage source, reverse-biases the base-collector junction

Since the Emitter is at ground (0V), by Kirchhoff's voltage law, Apply KVL to the base circuit we get;

$$V_{BB} - I_B R_B - V_{BE} = 0 \; ; \quad V_{BB} = I_B R_B + V_{BE}$$

Also by Ohms Law, Voltage drop across R_B, $V_{RB} = I_B R_B$

$$V_{RB} = V_{BB} - V_{BE} \; ; \quad V_{BE} = 0.7V$$

Solving for I_B, $I_B = \frac{V_{BB} - V_{BE}}{R_B}$ **, $I_C = \beta I_B$, $I_E = I_C + I_B$**

β_{DC} = dc current gain

Apply KVL to the Collector circuit we get;

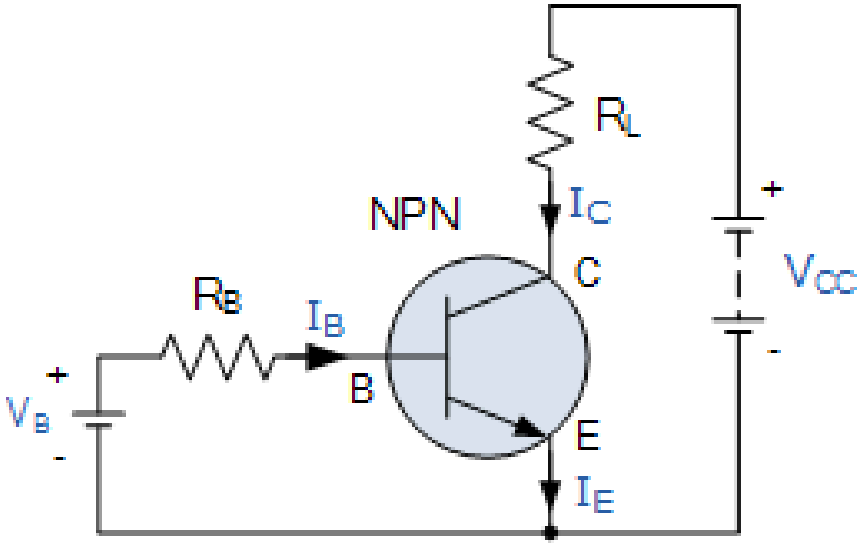
$$V_{CC} = I_C R_C + V_{CE}$$

The voltage at the collector with respect to the grounded emitter is $V_{CE} = V_{CC} - I_C R_C$

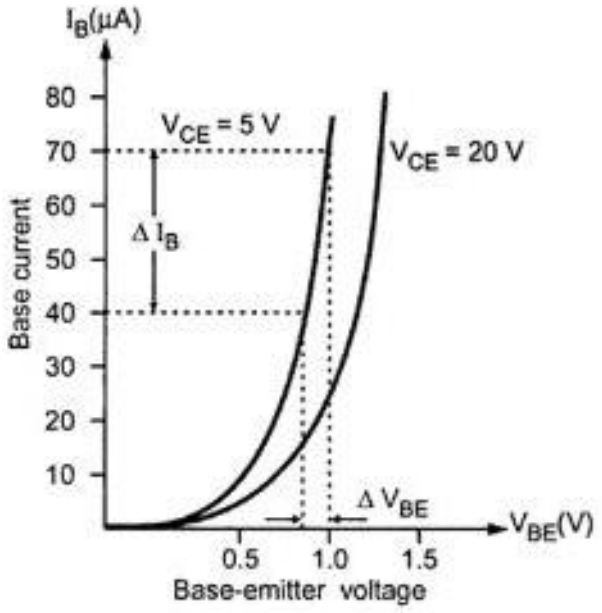
Voltage drop across R_C is $V_{RC} = I_C R_C$

The voltage across the reverse-biased collector-base junction is $V_{CB} = V_{CE} - V_{BE}$

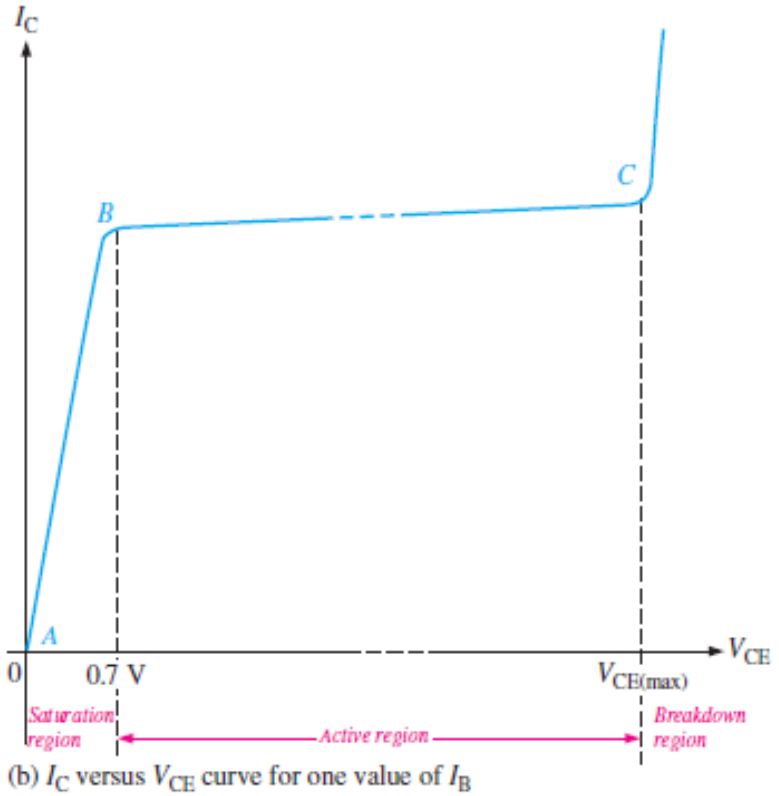
Input and Output Characteristics Curves of a Typical Bipolar Transistor



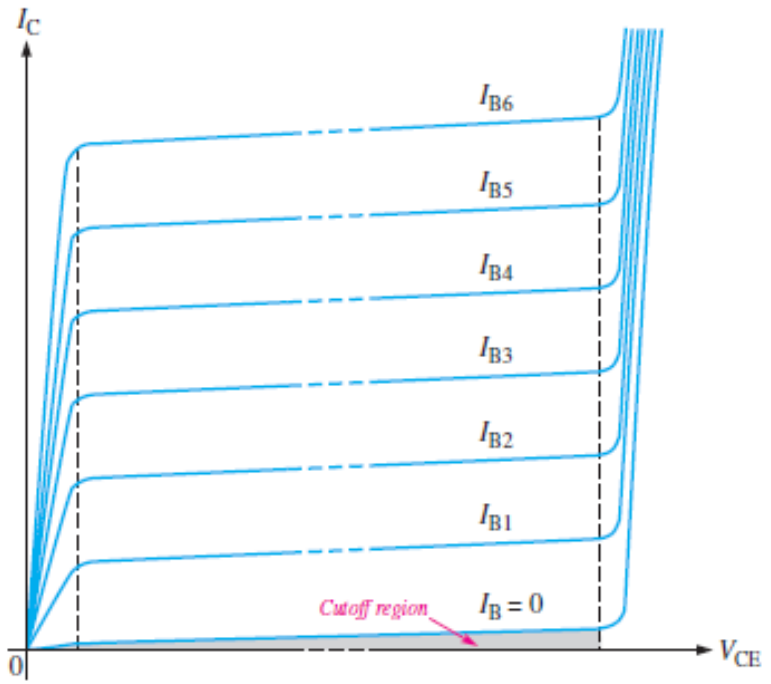
When dealing with the transistor configurations, characteristics curves are very important because they can predict the performance of a transistor. There are three curves, an input characteristic curve, a transfer characteristic curve and an output characteristic curve. Of these curves, the most useful for predicating the transistor performance is the output characteristics curve. The output characteristic curves for a BJT are a graph displaying the output voltages and currents for different input currents. It simply provides the V-I relationship at the output terminals, with either the input current or input voltage as parameters. For each transistor configuration CC, CE and CB (Common Base), the output curves are slightly



Input characteristics of the transistor in CE configuratior

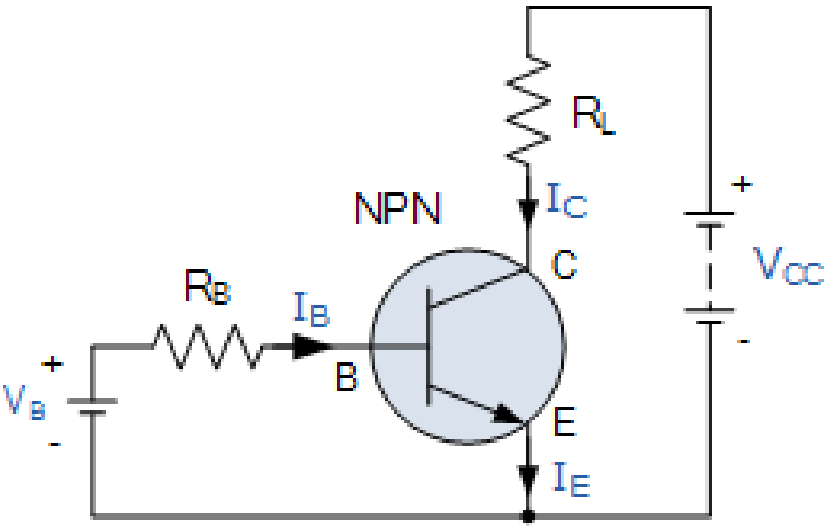


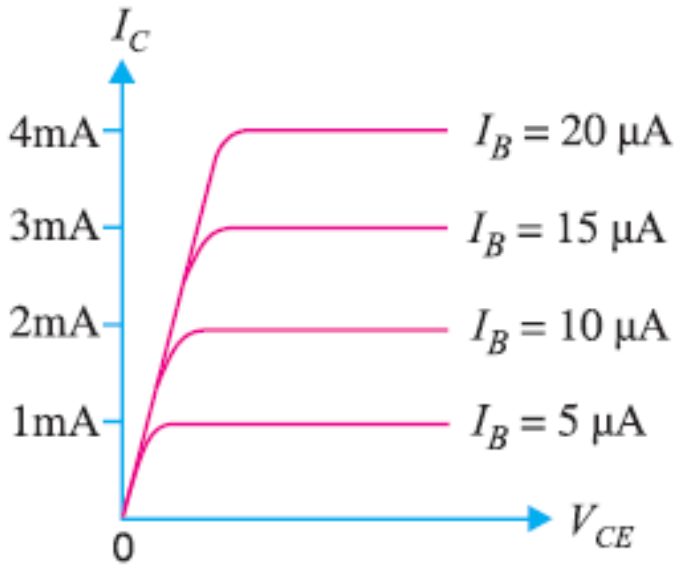
(b) I_C versus V_{CE} curve for one value of I_B

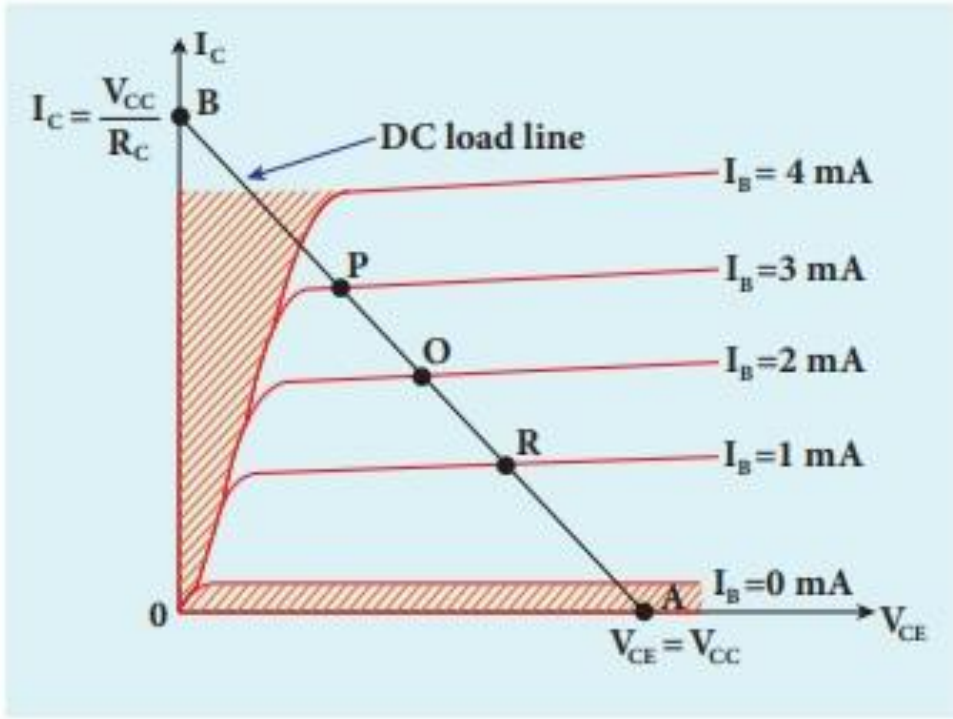


(c) Family of I_C versus V_{CE} curves for several values of I_B ($I_{B1} < I_{B2} < I_{B3}$, etc.)

Output Characteristics Curves of a Typical Bipolar Transistor







Apply KVL to the Collector circuit we get;

$$V_{CC} = I_C R_L + V_{CE}$$

Collector Current, $I_C = \dfrac{V_{CC} - V_{CE}}{R_L}$

When: $(V_{CE} = 0)$ $I_C = \dfrac{V_{CC} - 0}{R_L}$, $I_C = \dfrac{V_{CC}}{R_L}$

When: $(I_C = 0)$ $0 = \dfrac{V_{CC} - V_{CE}}{R_L}$, $V_{CC} = V_{CE}$

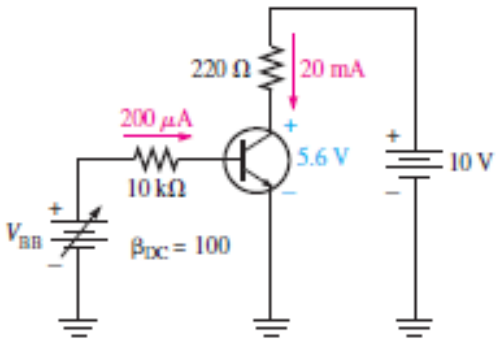
The **operating point** is a point where the transistor can be operated efficiently.

DC Load Line: The dc operation of a transistor circuit can be described graphically using a dc load line. This is a straight line drawn on the characteristic curves from the saturation value where $I_C = I_{C(sat)}$ on the y-axis to the cutoff value where VCE = VCC on the x-axis, The load line is determined by the external circuit(V_{CC} and R_C).

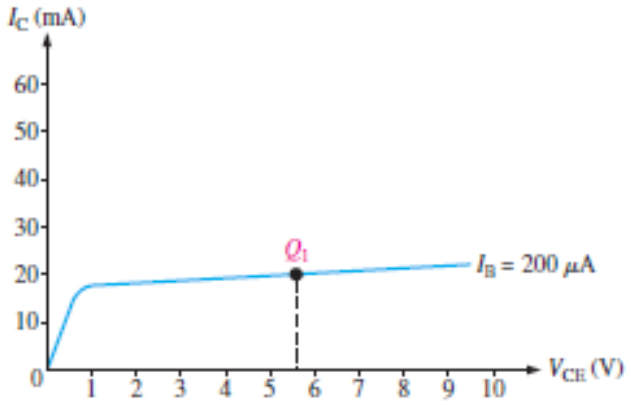
A line that is drawn with the values V_{CC} (when $I_C = 0$) and I_C (when $V_{CE} = 0$) is called the dc load line.

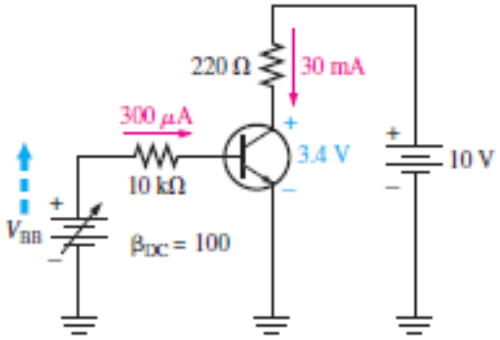
The dc load line superimposed on the output characteristics of a transistor is used to learn the operating point of the transistor

Illustration of Q-point adjustment

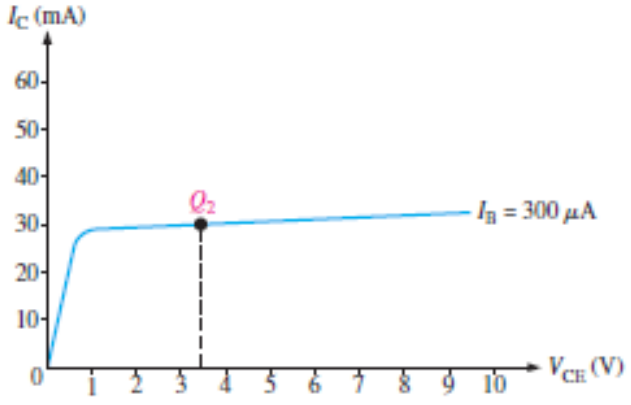


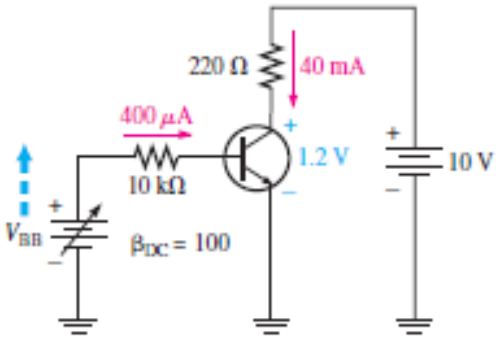
(a) $I_B = 200\,\mu A$



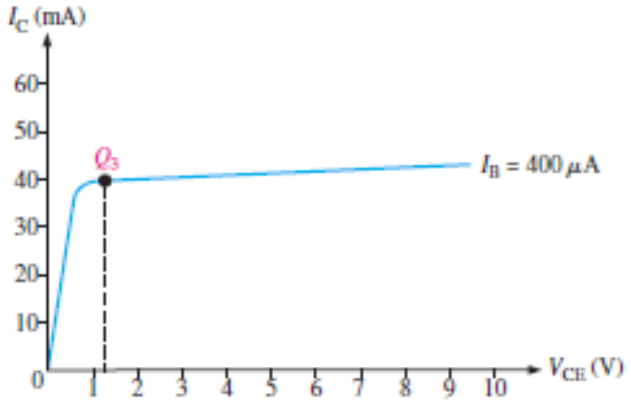


(b) Increase I_B to 300μ A by increasing V_{BB}

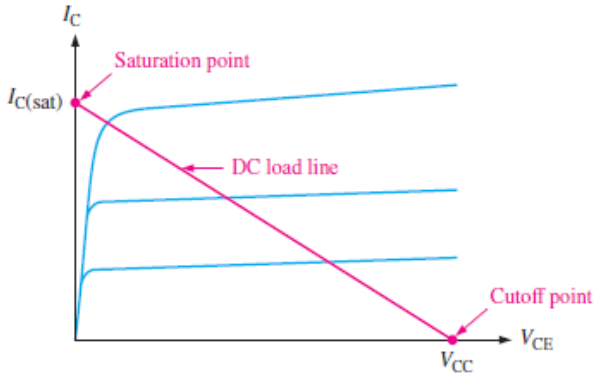




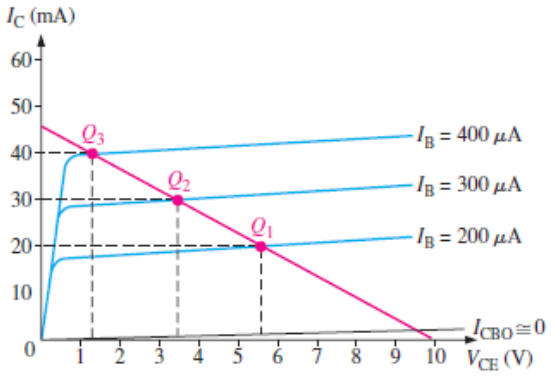
(c) Increase I_B to 400μ A by increasing V_{BB}



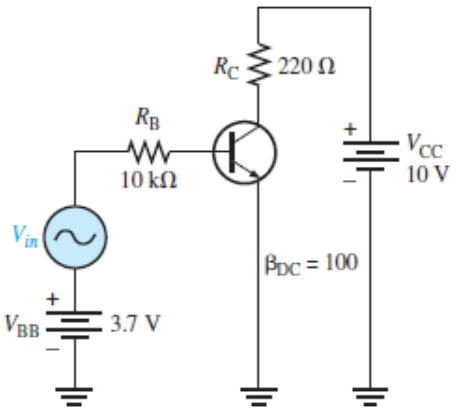
The dc load line



(a)



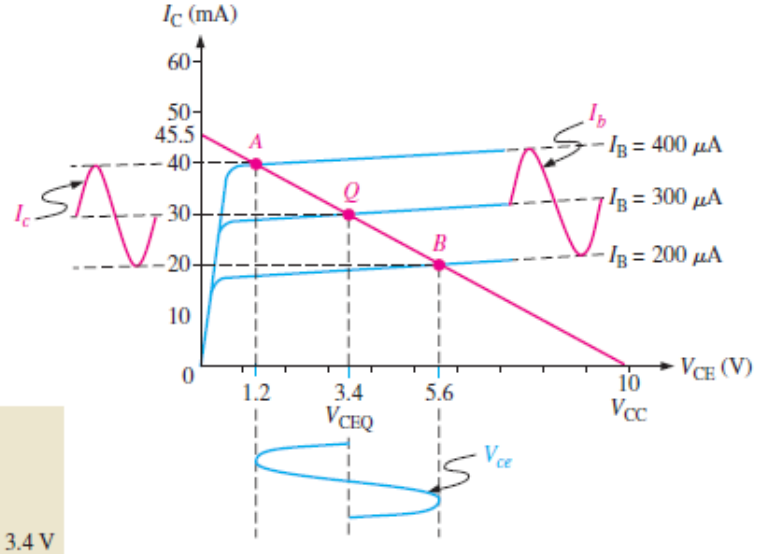
(b)



$$I_{BQ} = \frac{V_{BB} - 0.7\text{ V}}{R_B} = \frac{3.7\text{ V} - 0.7\text{ V}}{10\text{ k}\Omega} = 300\,\mu A$$

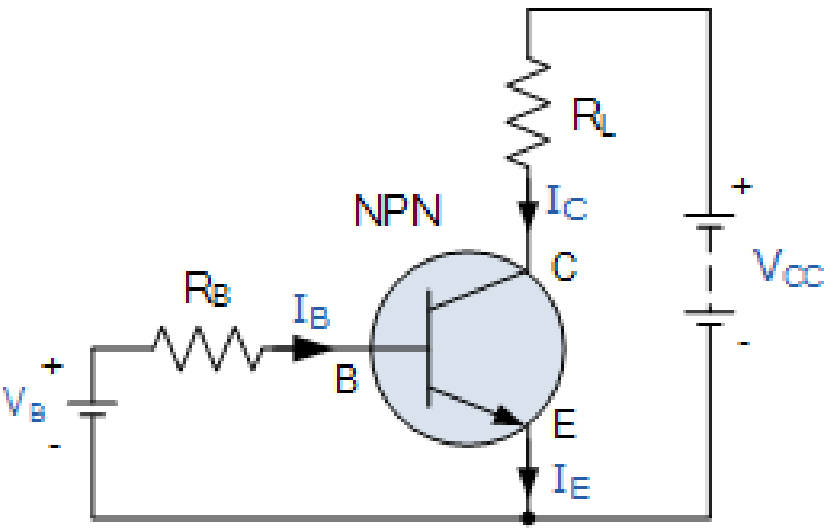
$$I_{CQ} = \beta_{DC} I_{BQ} = (100)(300\,\mu A) = 30\text{ mA}$$

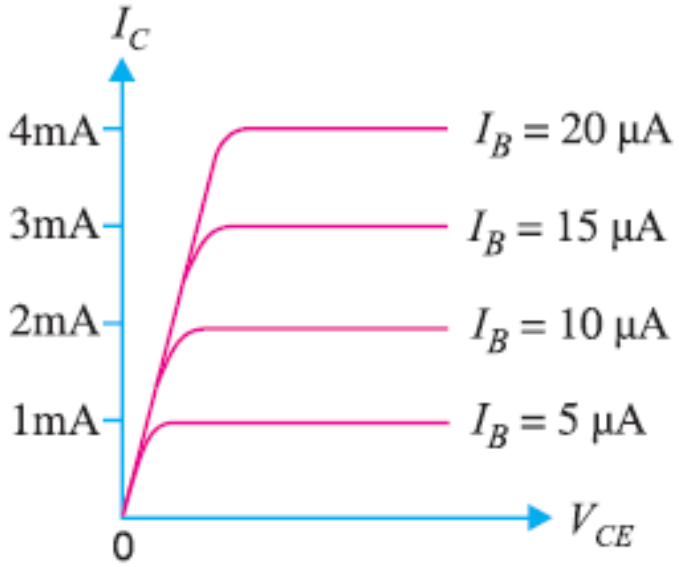
$$V_{CEQ} = V_{CC} - I_{CQ} R_C = 10\text{ V} - (30\text{ mA})(220\,\Omega) = 3.4\text{ V}$$

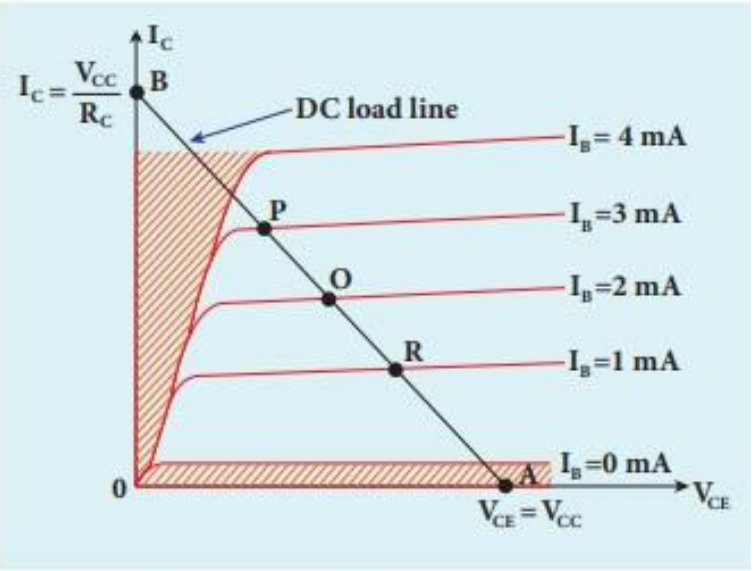


Variations in collector current and collector-to-emitter voltage as a result of a variation in base current

Output Characteristics Curves of a Typical Bipolar Transistor







Collector Current, $I_C = \frac{V_{CC} - V_{CE}}{R_L}$

When: $(V_{CE} = 0)$ $I_C = \frac{V_{CC} - 0}{R_L}$, $I_C = \frac{V_{CC}}{R_L}$

When: $(I_C = 0)$ $0 = \frac{V_{CC} - V_{CE}}{R_L}$, $V_{CC} = V_{CE}$

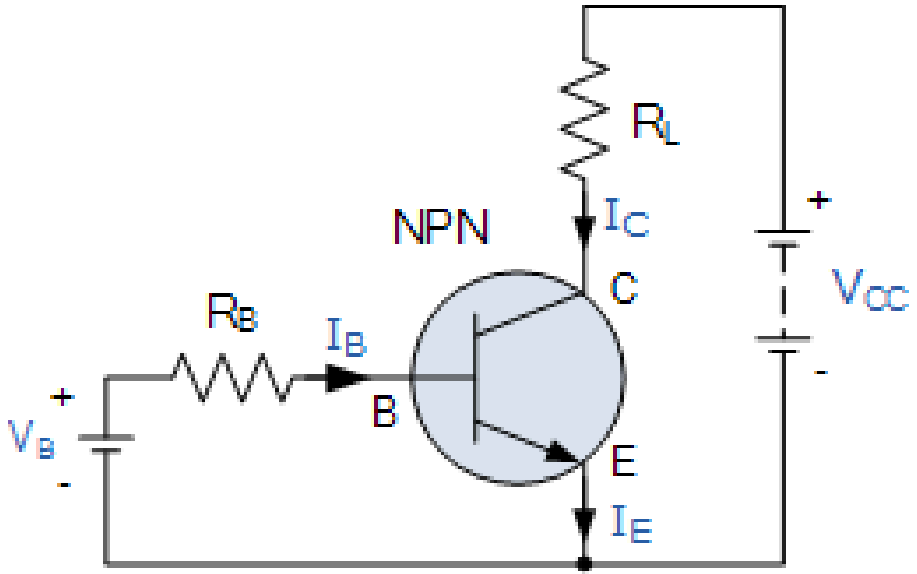
Points P, Q, R in Figure are called Q points or quiescent points which determine the operating point or the working point of a transistor.

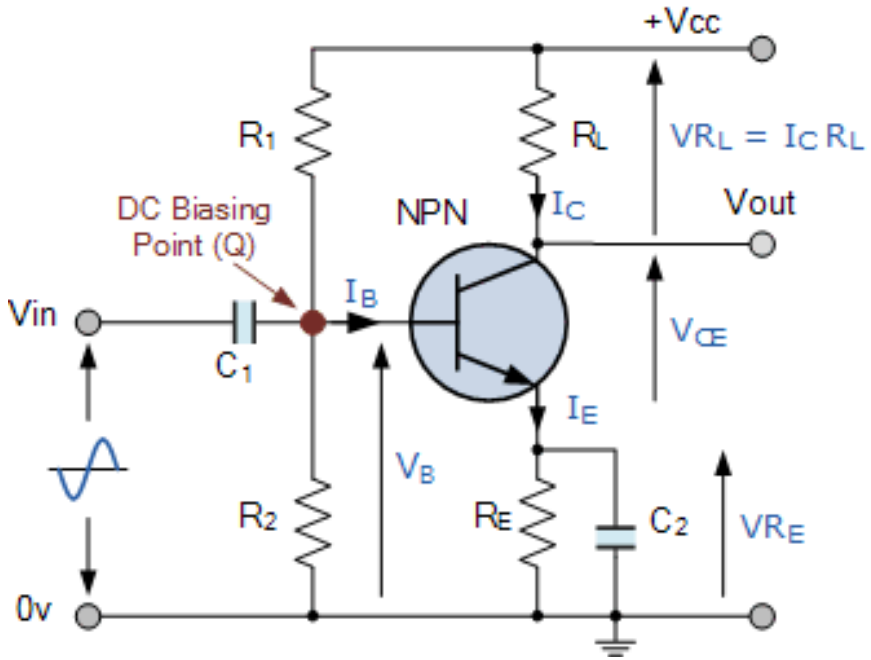
If the operating point is chosen at the middle of the dc load line (point Q), the transistor can effectively work as an amplifier.

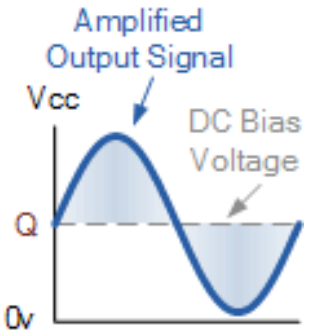
The operating point determines the maximum signal that can be obtained without being distorted.

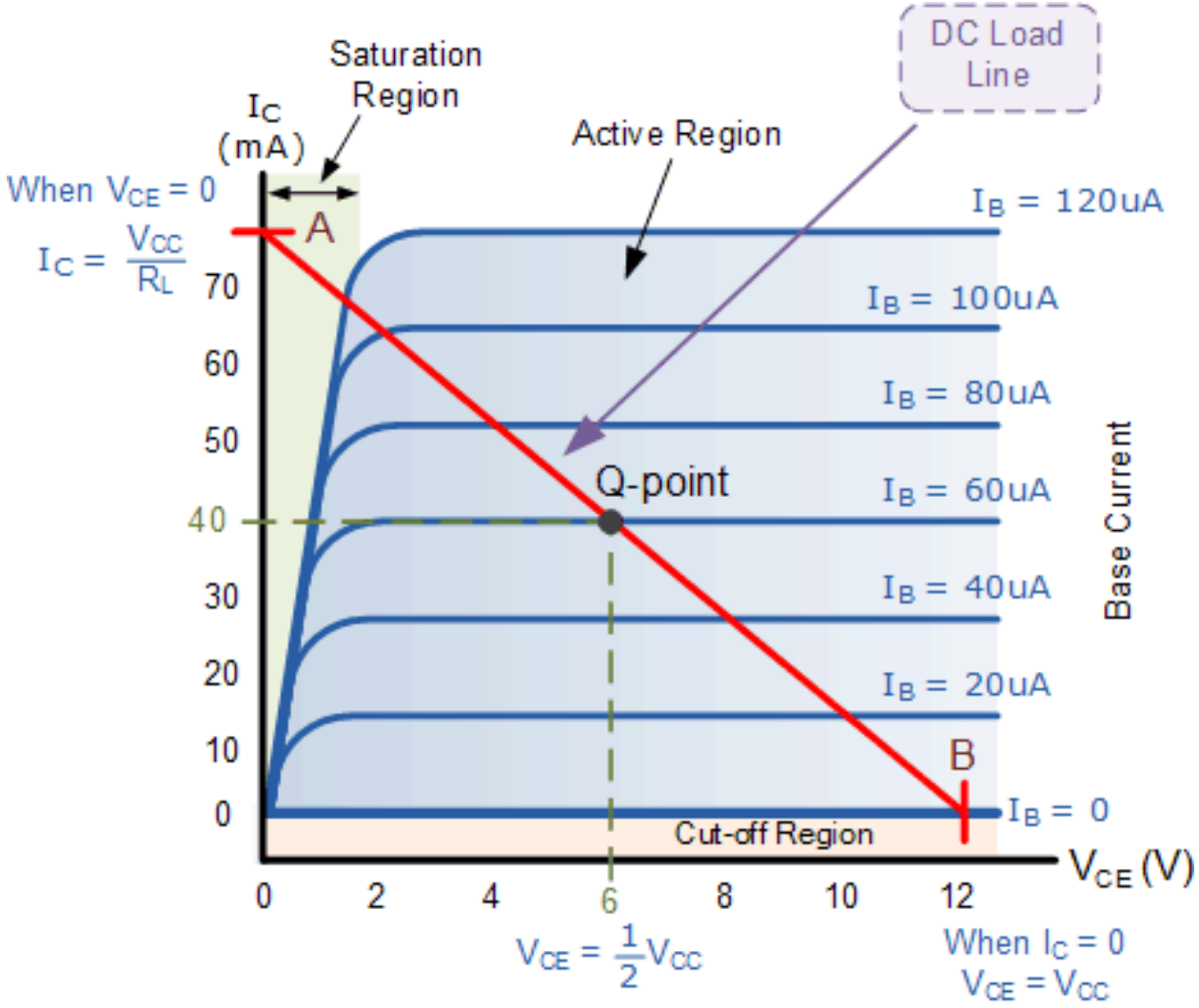
For a transistor to work as a open switch, the Q point OR quiescent points can be chosen at the cut-off region and to work as a closed switch, the Q point can be chosen in the saturation region.

Output Characteristics Curves of a Typical Bipolar Transistor

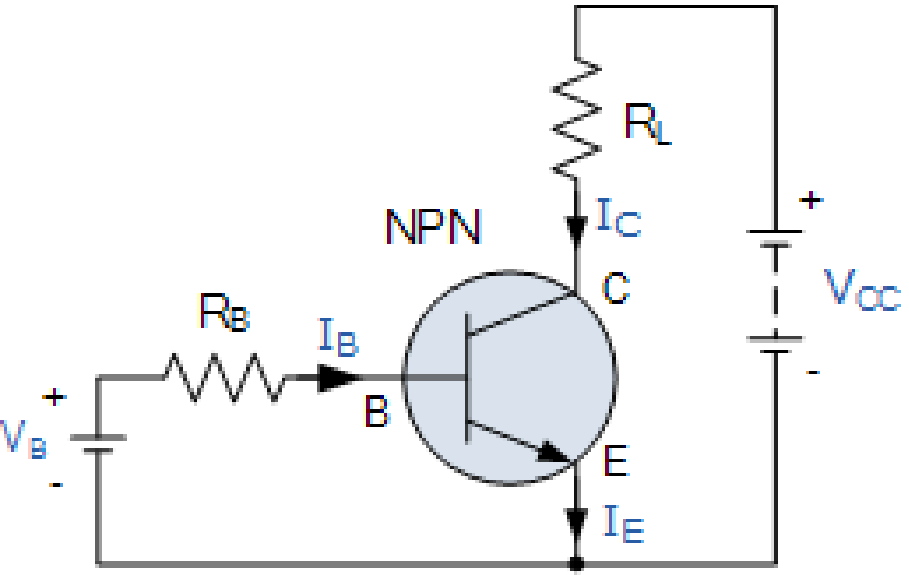


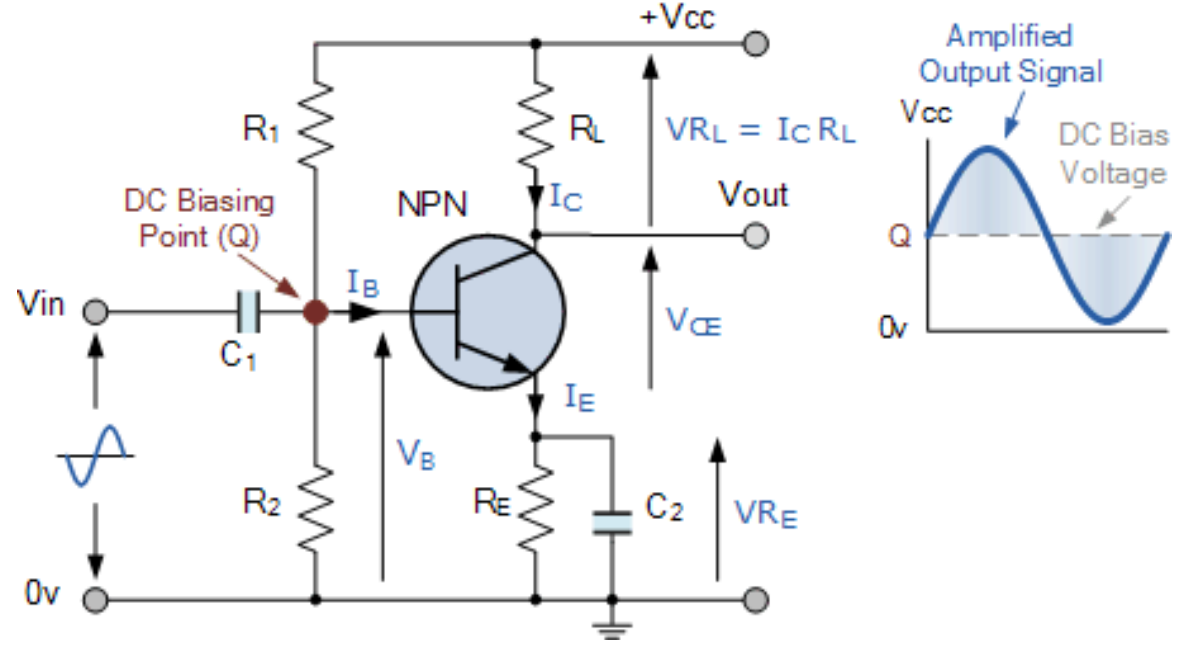


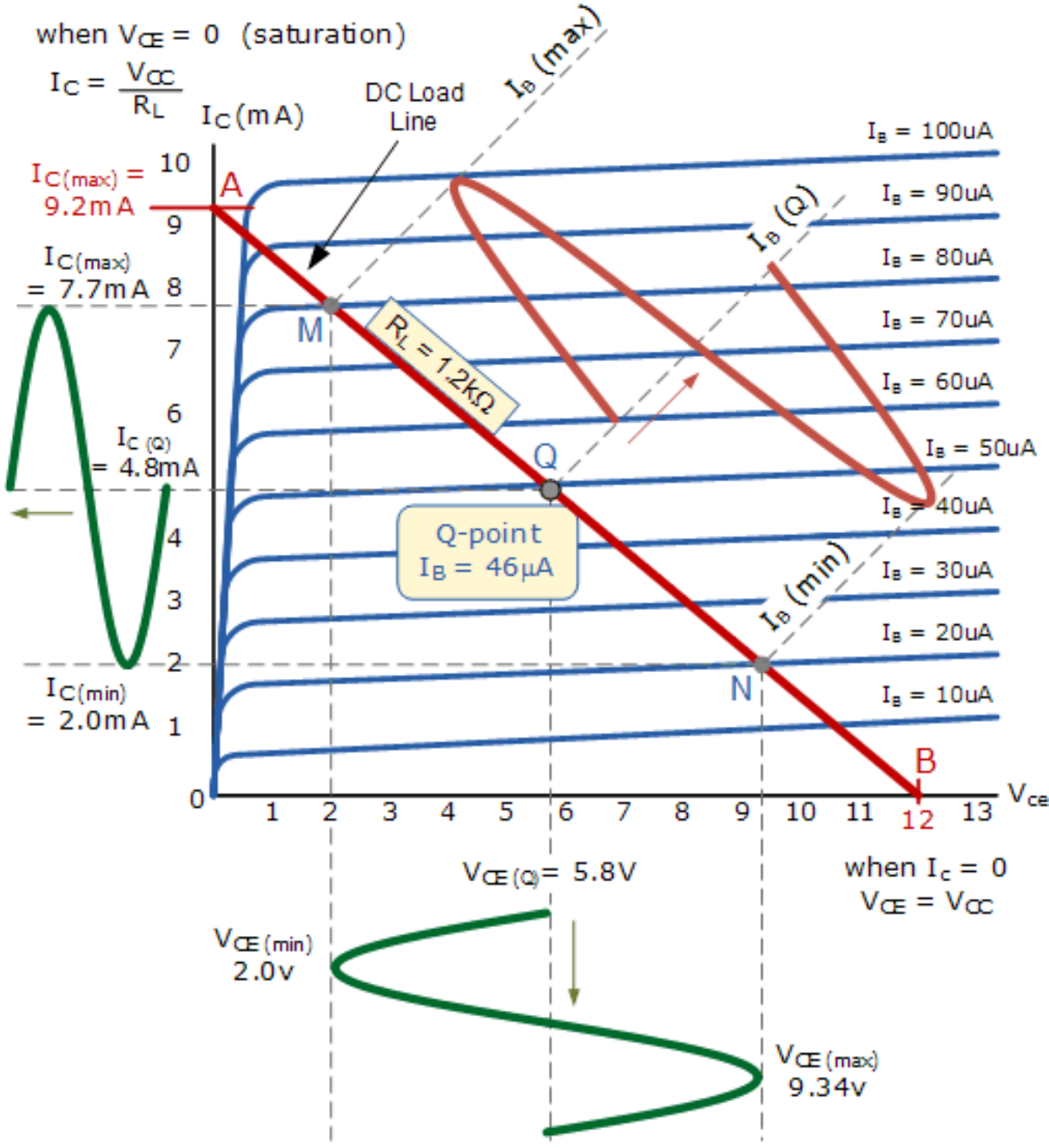




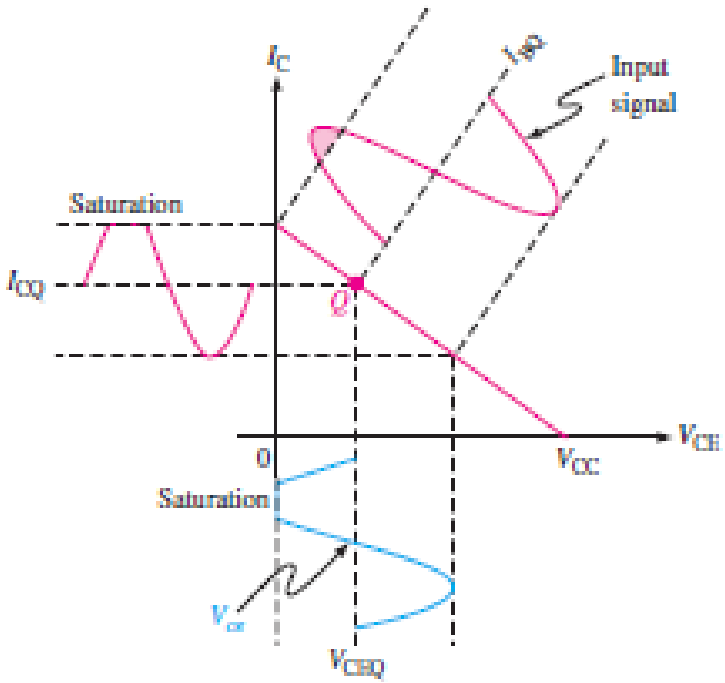
Output Characteristics Curves of a Typical Bipolar Transistor



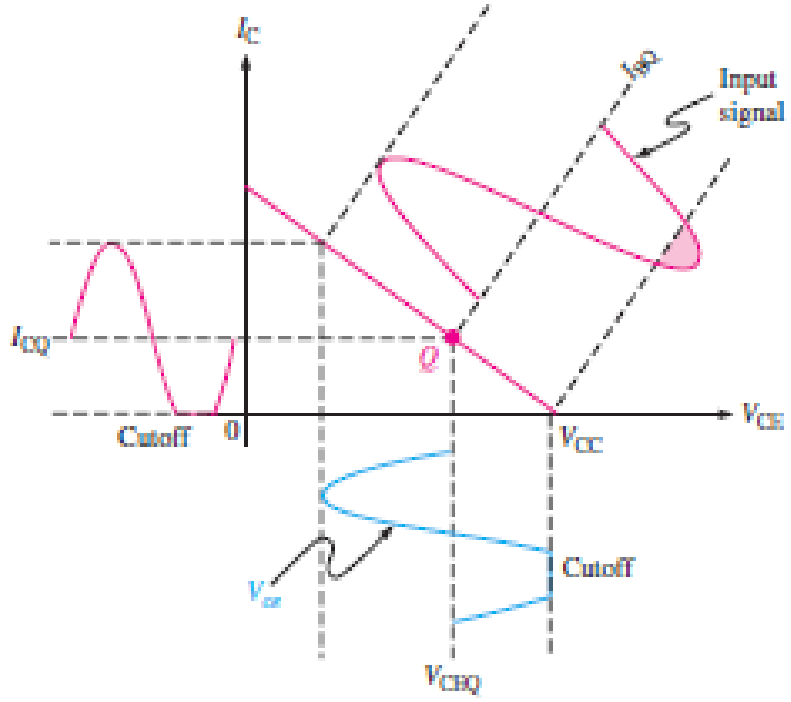




Waveform Distortion Graphical load line illustration of a transistor being driven into saturation and/or cutoff

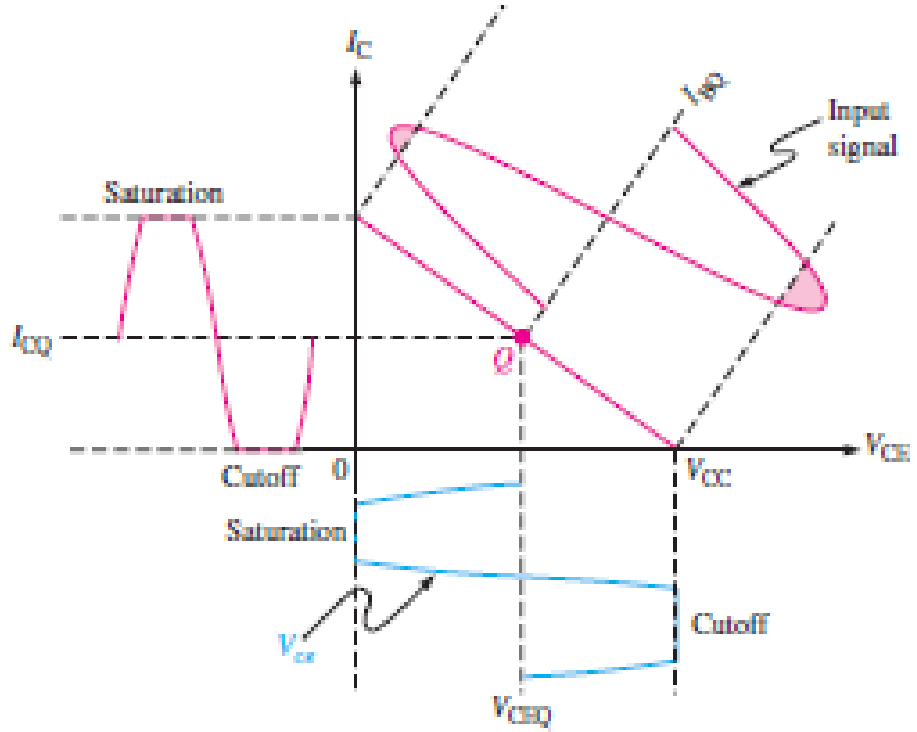


(a) Transistor is driven into saturation because the Q-point is too close to saturation for the given input signal.



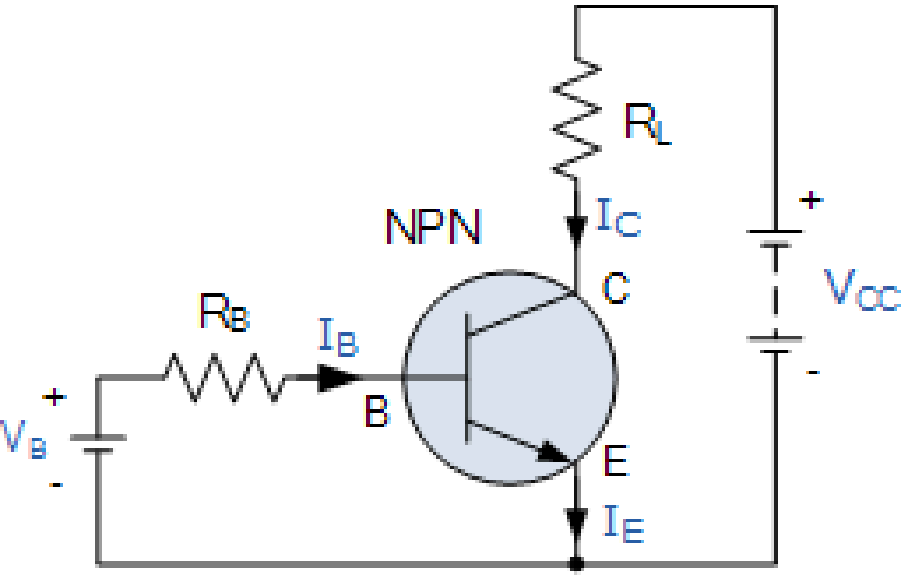
(b) Transistor is driven into cutoff because the Q-point is too close to cutoff for the given input signal.

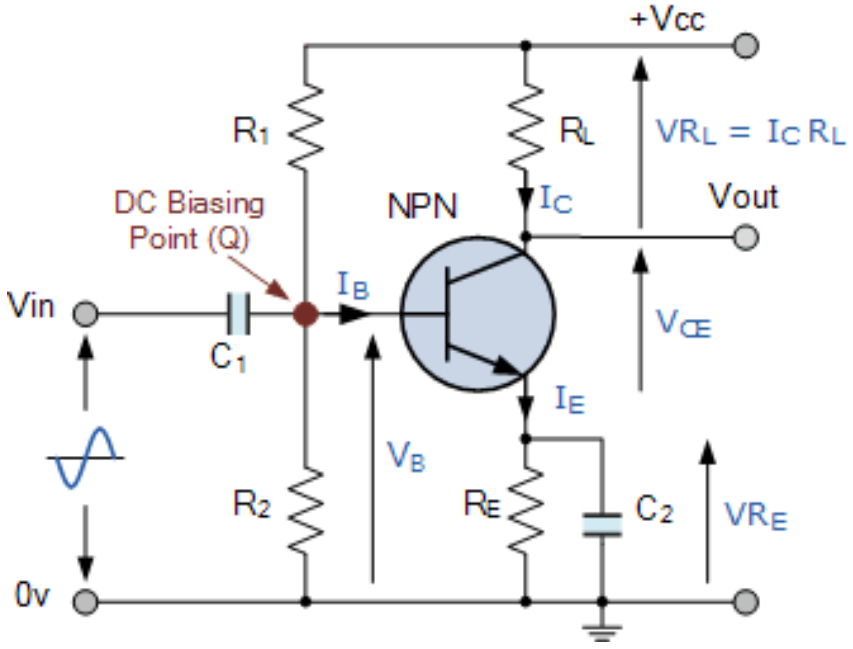
under certain input signal conditions the location of the Q-point on the load line can cause one peak of the Vce waveform to be limited or clipped, as shown in parts Fig (a) and (b). In each case the input signal is too large for the Q-point location and is driving the transistor into cutoff or saturation during a portion of the input cycle.

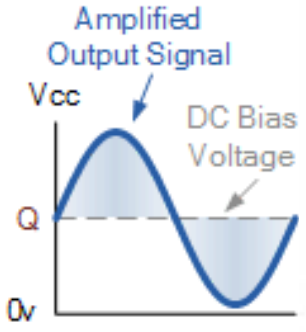


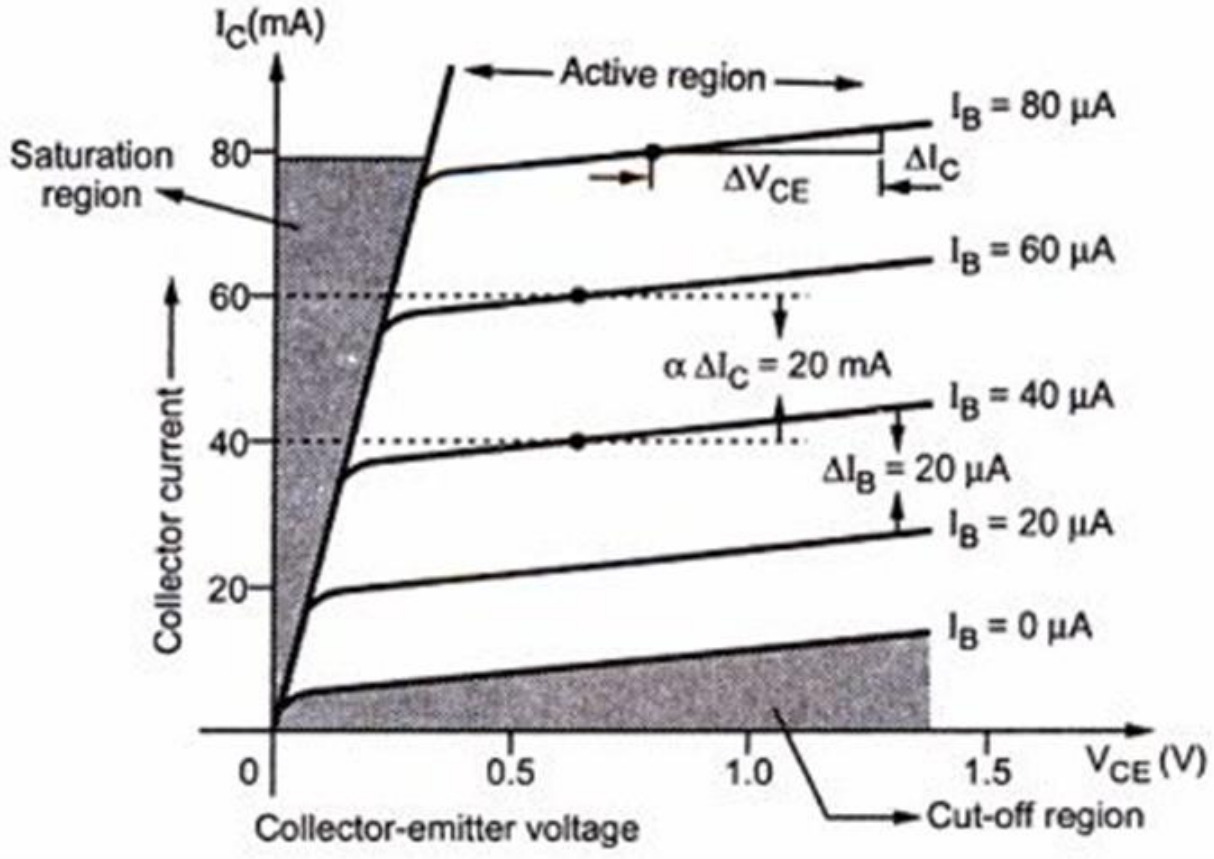
(c) Transistor is driven into both saturation and cutoff because the input signal is too large.

Output Characteristics Curves of a Typical Bipolar Transistor





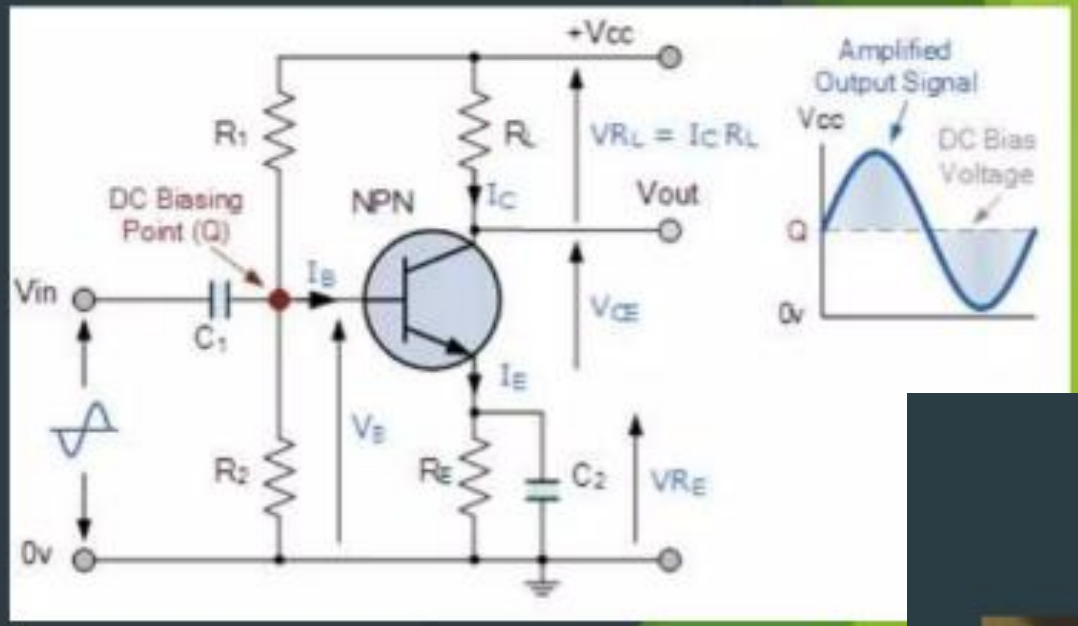




Output characteristics of the transistor in CE configuration

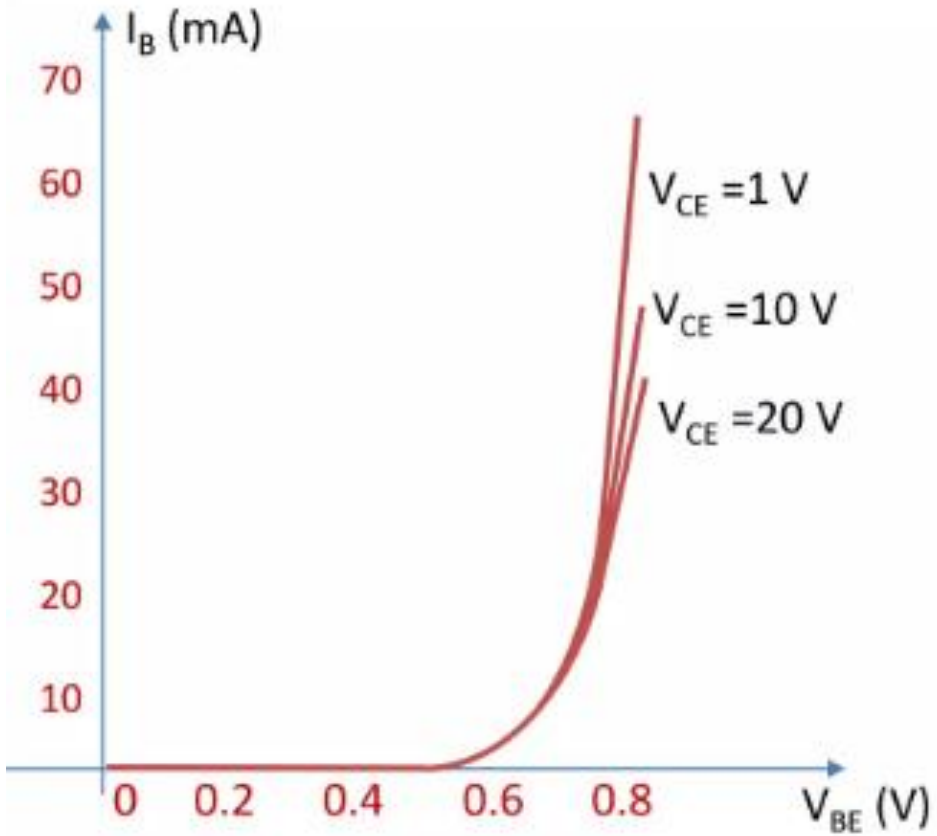
Common Emitter Amplifier

- a common emitter amplifier is typically used as a voltage amplifier
- Input is applied to base ,output is taken across collector and the emitter is grounded.
- Features:
  - Moderate /high input impedance.
  - Moderate output impedance.
  - High Voltage Gain
  - High Currant Gain.
  - Output is Inverted

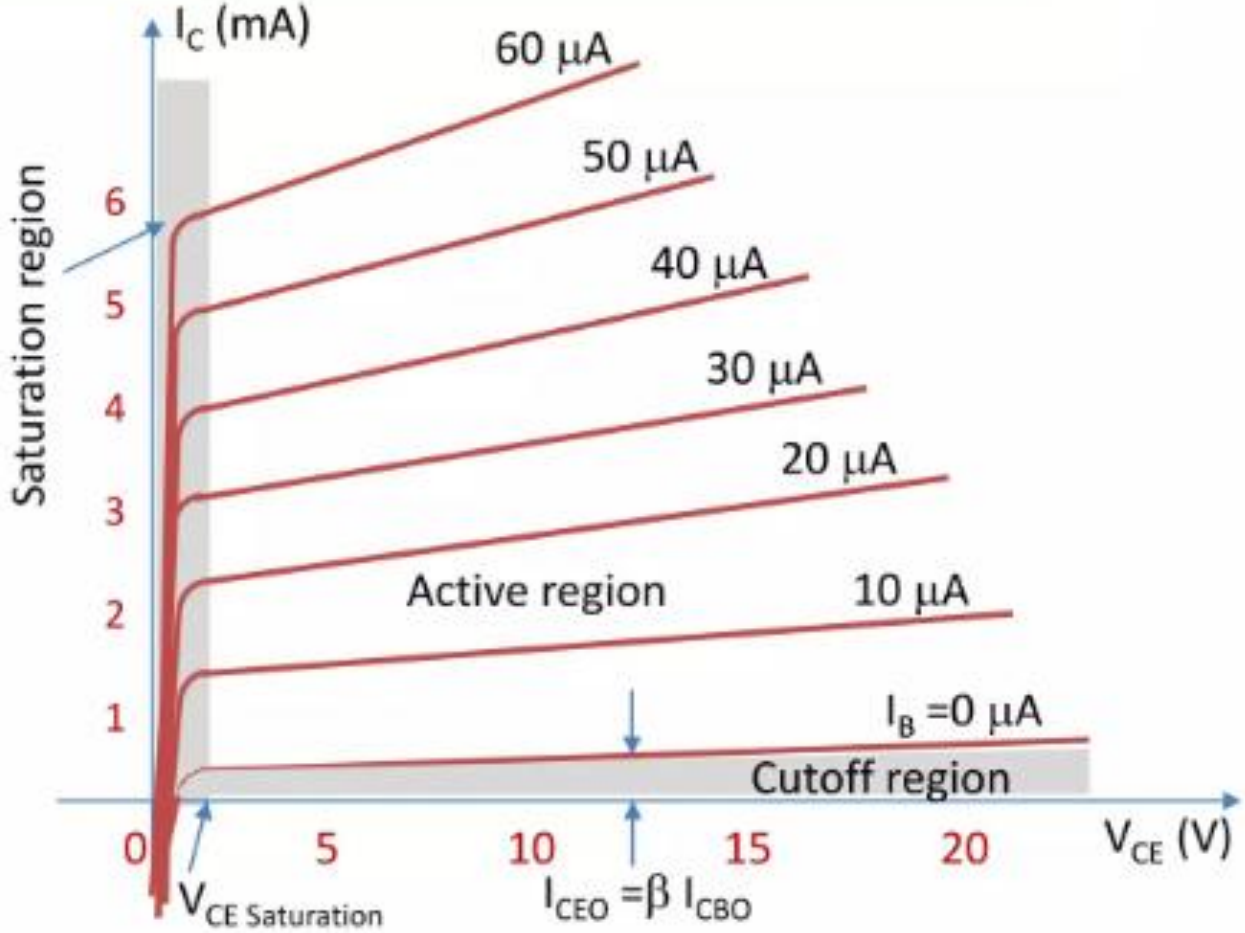


Experimental Output of CE

BJT: Common Emitter Configuration



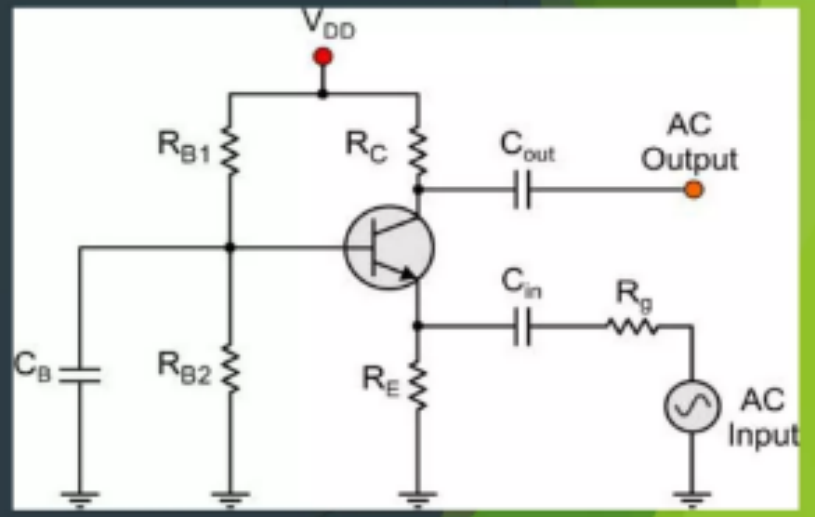
Input characteristics of CE configuration



Output characteristics of CE configuration

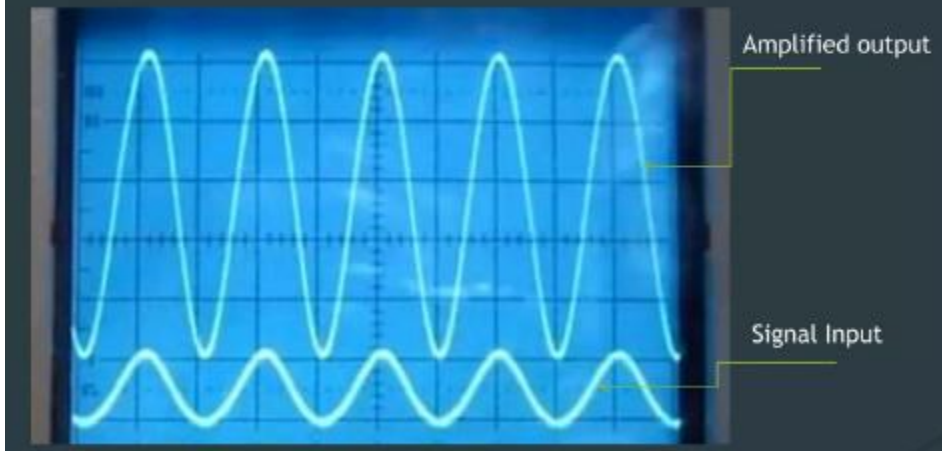
Common base amplifier

- A **common base** also known as **grounded-base** amplifier is typically used as a voltage amplifier.
- In this circuit
  - The emitter terminal serves as the input
  - The collector as the output
  - The base is connected to ground, or "common".
- Features:
  - Low input impedance.
  - Moderate/High output impedance.
  - High Voltage Gain
  - Unity Current Gain.
  - Non-inverting amplifier.

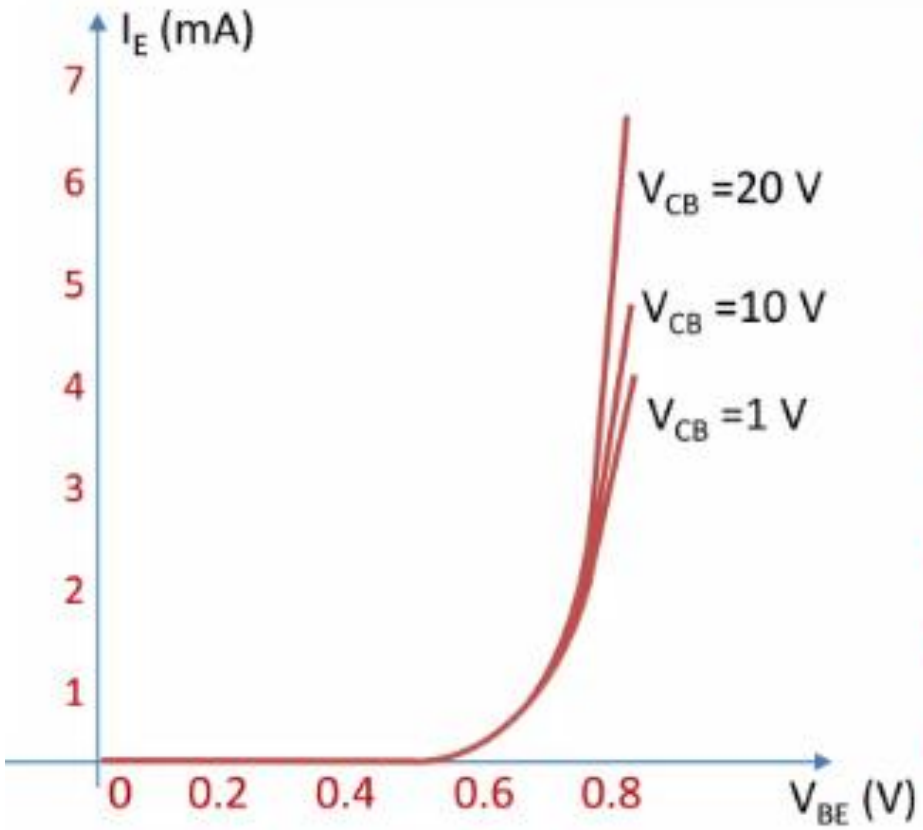


The Common base amplifier circuit

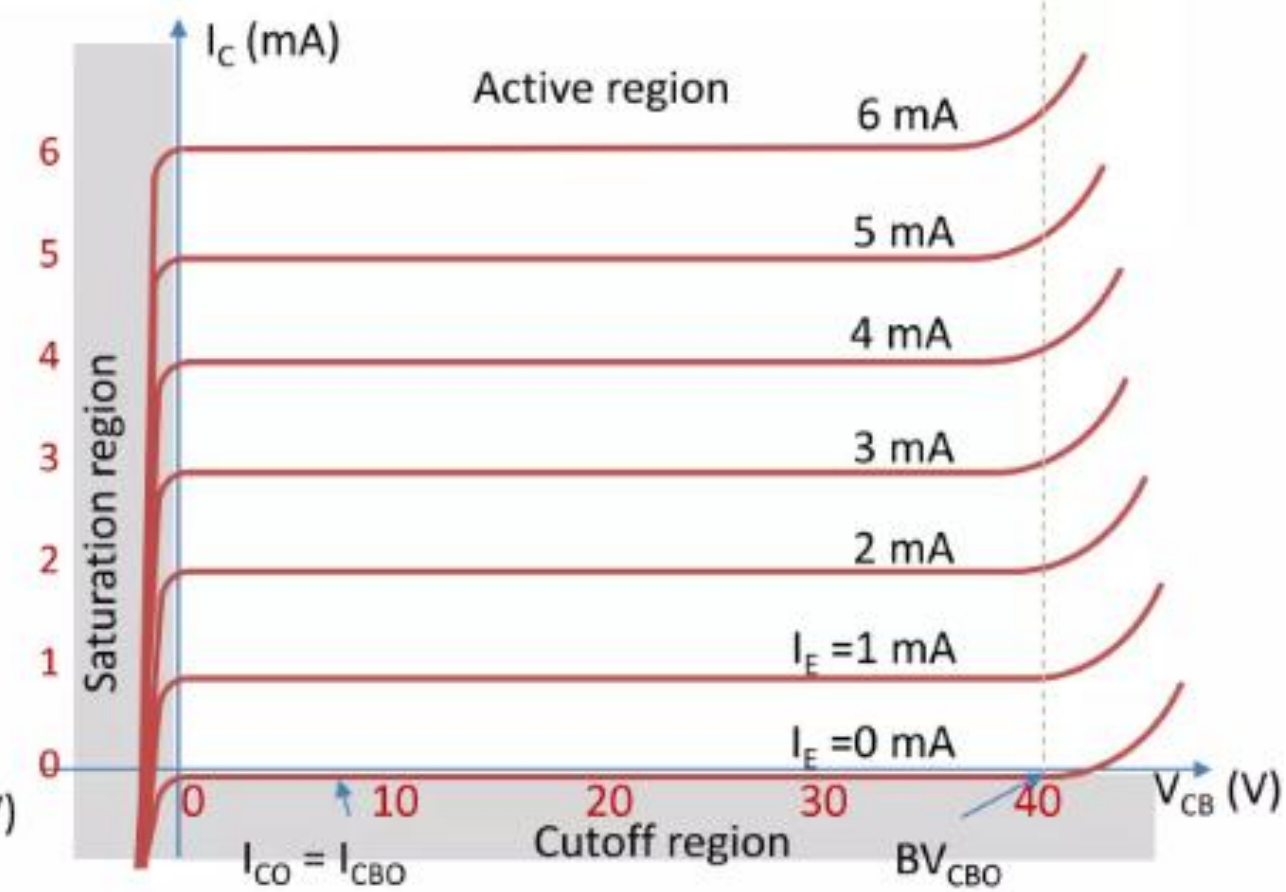
Experimental Output of CB Amplifier



BJT: Common Base configuration



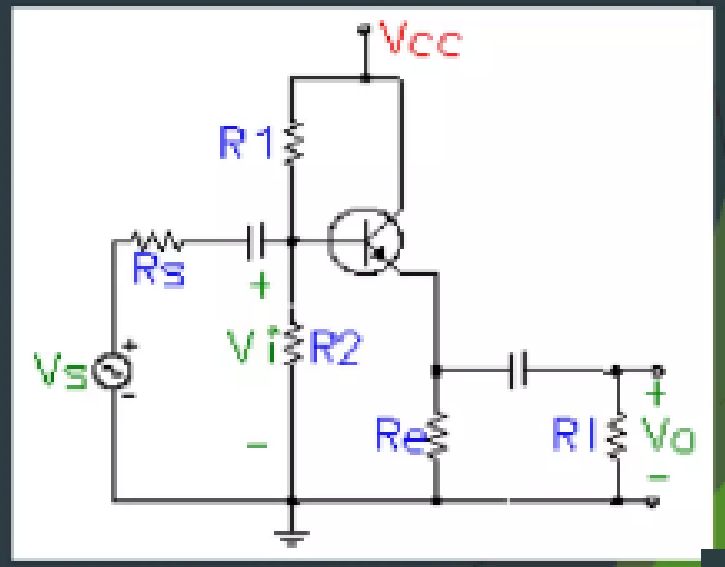
Input characteristics of CB configuration



Output characteristics of CB configuration

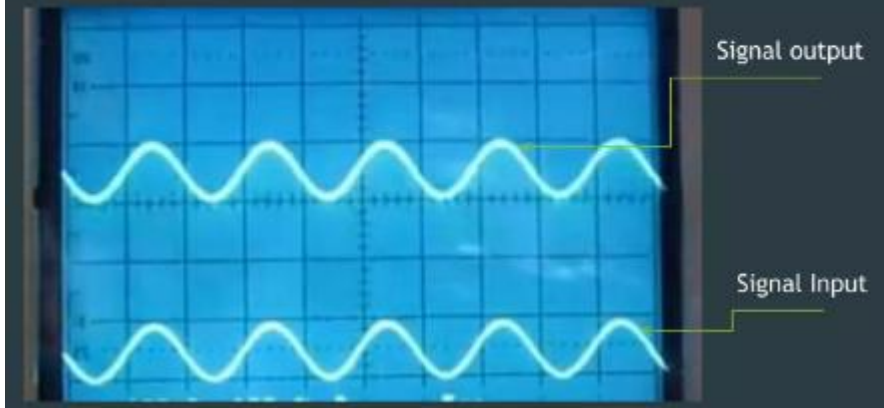
Common collector

- Common collector amplifier also known as an **emitter follower** typically used as a voltage buffer.
- In this circuit
  - The base terminal serves as the input,
  - The emitter is the output
  - The collector is common.
- Features:
  - Moderate/high input impedance.
  - Low output impedance.
  - Low (unity) voltage gain.
  - High Current Gain.

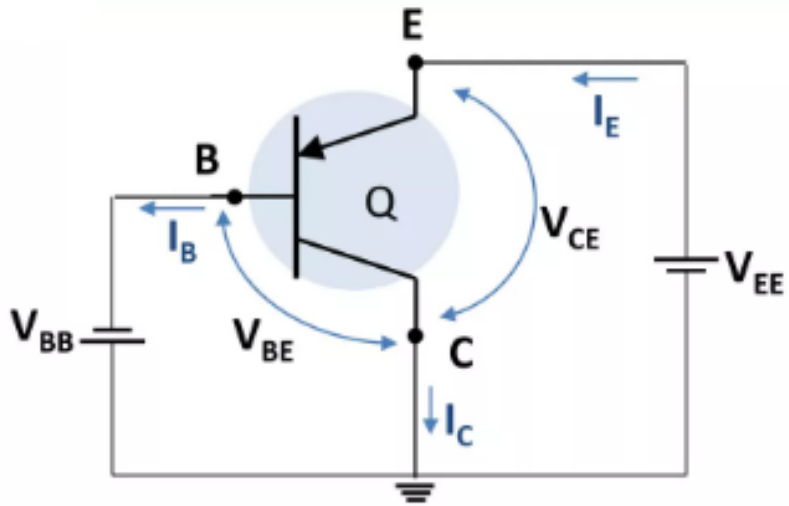


The CC amplifier circuit

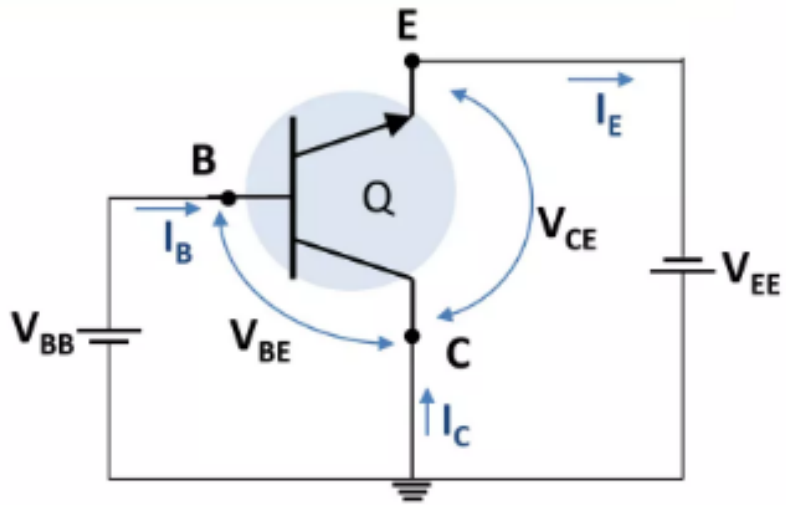
Experimental Output of CC Amplifier.



BJT: Common Collector Configuration



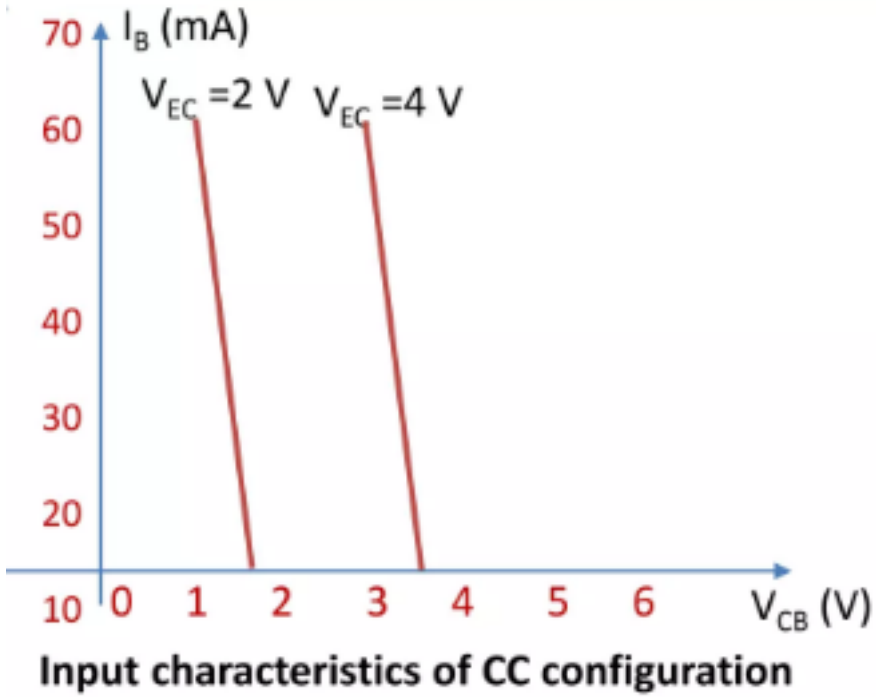
Common emitter configuration pnp transistor



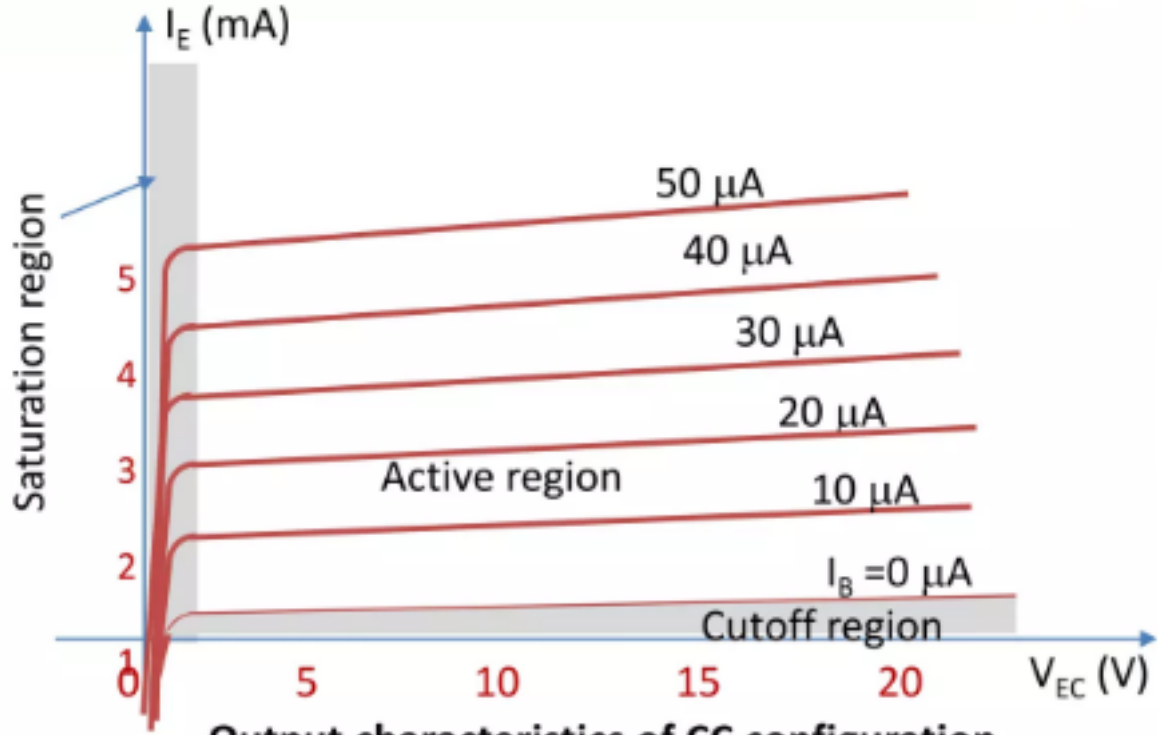
Common emitter configuration npn transistor

- CC configuration is also known as emitter follower configuration as the emitter voltage follows the base voltage.
- This configuration is mostly used as a buffer.
- CC configuration is used mainly for impedance-matching, as it has high-input & low-output impedance, opposite to CB/CE Configuration

BJT: Common collector Configuration



Input characteristics of CC configuration

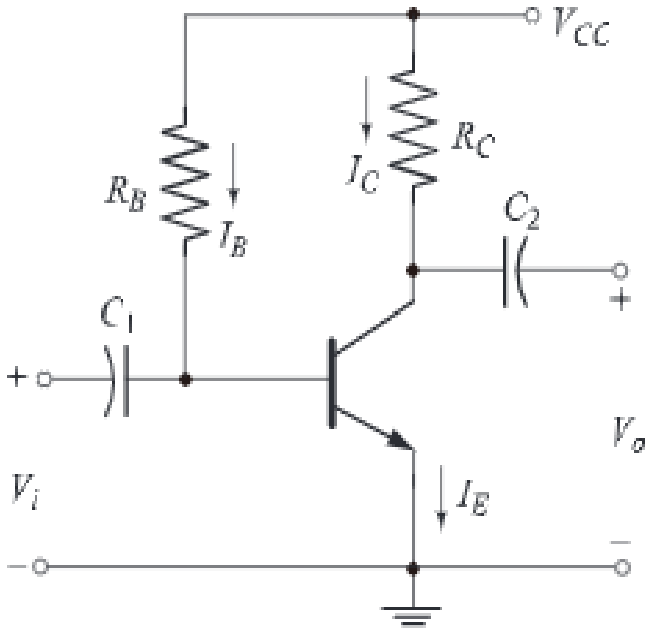


Output characteristics of CC configuration

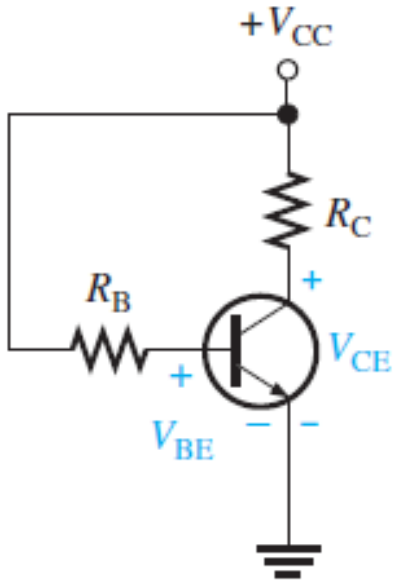
- Input characteristics of the CC configuration is different as current I_B decreases with increase in base collector voltage
- Output characteristics of the CC configuration are the same as of CE configuration.

Fixed Bias Configuration

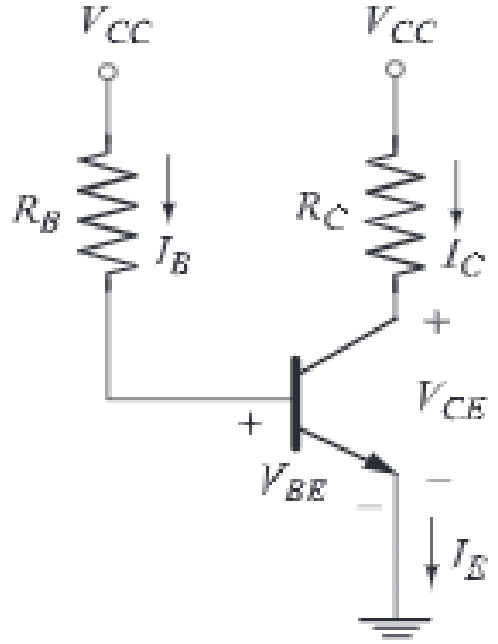
For the dc analysis we can replace capacitor with an open circuit (since capacitor blocks dc) because the reactance of capacitor is infinity



Circuit Diagram

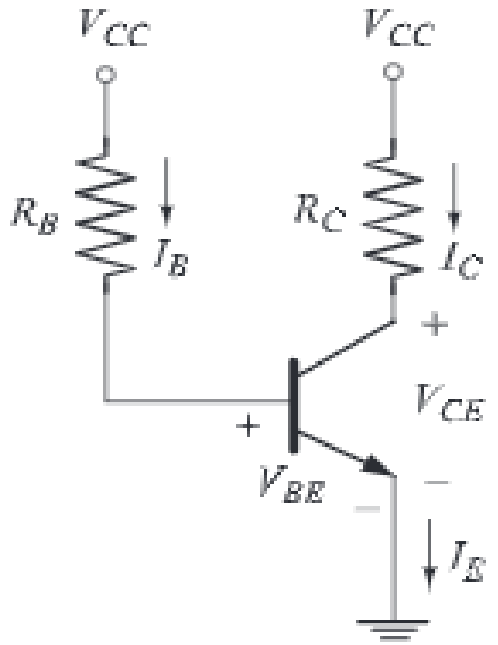


C_1 & C_2 = Coupling Capacitors
V_{CC} = Supply voltage
R_B = Base Resistance
R_C = Collector Resistance



DC equivalent circuit of fixed bias

Fixed Bias Configuration



DC equivalent circuit of fixed bias

Apply KVL to the base circuit we get;

$$V_{CC} - I_B R_B - V_{BE} = 0$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

Apply KVL to the Collector circuit we get;

$$V_{CC} = I_C R_C + V_{CE}$$

$$V_{CE} = V_{CC} - I_C R_C$$

$$I_C = \frac{V_{CC} - V_{CE}}{R_C}$$

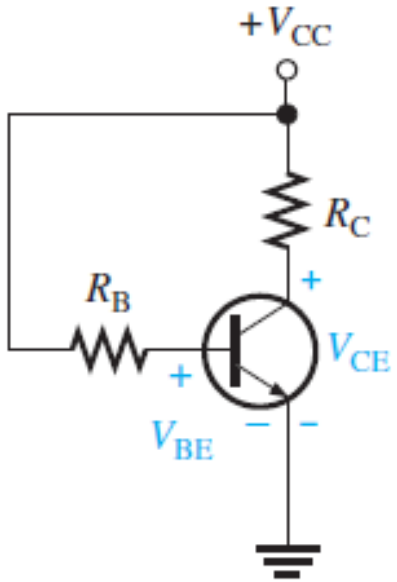
$I_C = \beta I_B$ **Where** β_{DC} **= dc current gain and** $I_E = I_C + I_B$

Also $V_{CE} = V_C - V_E$; $V_{BE} = V_B - V_E$

Since the Emitter is at ground (0V), $V_E = 0$

$V_{BE} = V_B$; $V_{CE} = V_C$

Fixed Bias Configuration



$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

$$I_C = \frac{V_{CC} - V_{CE}}{R_C}$$

$$I_C = \beta I_B \qquad I_E \sim I_C$$

$$I_C = \beta \frac{V_{CC} - V_{BE}}{R_B}$$

Base bias.

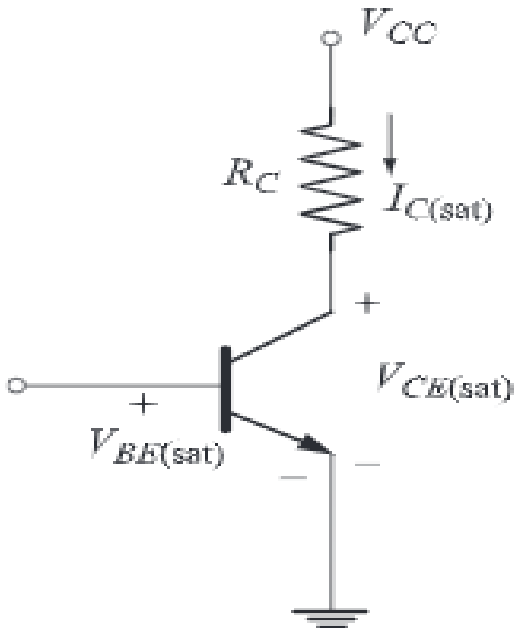
Q-Point Stability of Base Bias

- Notice that Equation I_C shows that I_C is dependent on β_{DC}. The disadvantage of this is that a variation in β_{DC} causes I_C and, as a result, V_{CE} to change, thus changing the Q-point of the transistor. This makes the base-bias circuit extremely beta-dependent and unpredictable.

- Recall that β_{DC} varies with temperature and collector current. In addition, there is a large spread of β_{DC} values from one transistor to another of the same type due to manufacturing variations.

- For these reasons, base bias is used in switching circuits where the transistor is either in saturation or cutoff but is rarely used in linear circuits

Fixed Bias Configuration



Transistor operating in Saturation region

Apply KVL to the Collector circuit we get;

$$V_{CC} - I_{C(sat)}R_C - V_{CE(sat)} = 0$$

$$I_{C(sat)} = \frac{V_{CC} - V_{CE(sat)}}{R_C}$$

But $V_{CE(sat)} \approx 0$

$$I_{C(sat)} \approx \frac{V_{CC}}{R_C}$$

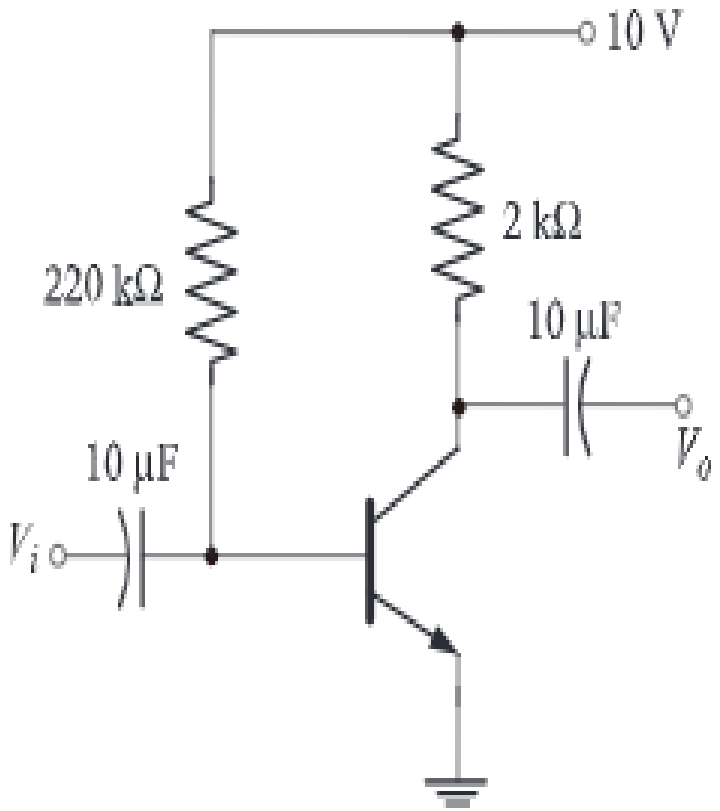
Fixed Bias Configuration: Numericals

1. For the fixed bias circuit shown, assuming VBE = 0.7V and β = 60 find:

a. Quiescent values of base and collector currents.
b. Quiescent value of V_{CE}.
c. Base-ground and collector-ground voltages.
d. Base-collector voltage
e. Quiescent values of I_C and V_{CE} for β = 110.

Given Data:

$V_{CC} = 10V$
$R_B = 220k\Omega$
$R_C = 2k\Omega$
$C_1 = C_2 = 10\mu F$



Circuit Diagram

Fixed Bias Configuration: Numericals

Coupling Capacitors acts as open circuit.

a. Quiescent values of base current and collector current.

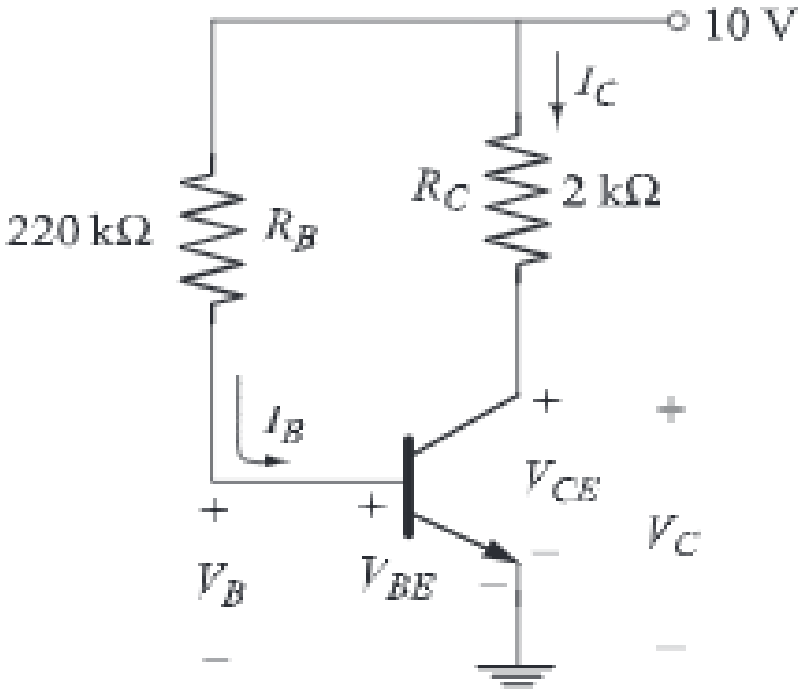
$$I_{BQ} = \frac{V_{CC} - V_{BE}}{R_B} = \frac{10\,\text{V} - 0.7\,\text{V}}{220\,\text{kW}} = 42.27\ \mu\text{A}$$

$$I_{CQ} = \beta I_{BQ} = 60 \times 42.27\ \mu\text{A} = 2.54\ \text{mA}$$

b. Quiescent value of V_{CE}.

$$V_{CC} = I_C R_C + V_{CE}$$

$$V_{CEQ} = V_{CC} - I_{CQ} R_C = 10 - (2.54\ \text{mA})(2\ \text{k}\Omega) = 4.92\ \text{V}$$



DC equivalent circuit of fixed bias

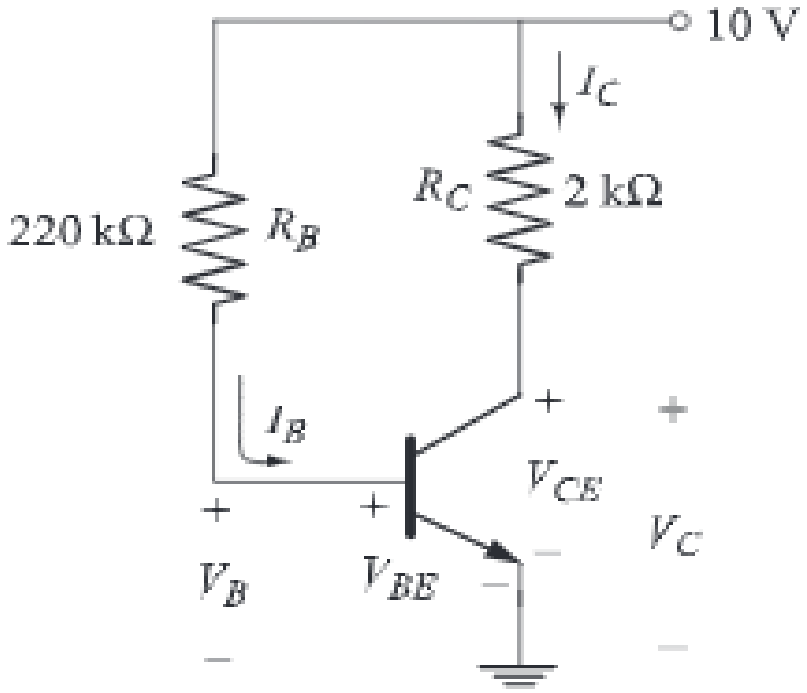
Fixed Bias Configuration: Numericals

c. Base and collector voltages with respect to ground.

$$V_B = V_{BE} = 0.7\ \text{V}$$
$$V_C = V_{CE} = 4.92\ \text{V}$$

d. Base-collector voltage.

$$V_{BC} = V_B - V_C = 0.7\ \text{V} - 4.92\ \text{V} = -4.22\ \text{V}$$



DC equivalent circuit of fixed bias

Fixed Bias Configuration: Numericals

e. When β = 110.

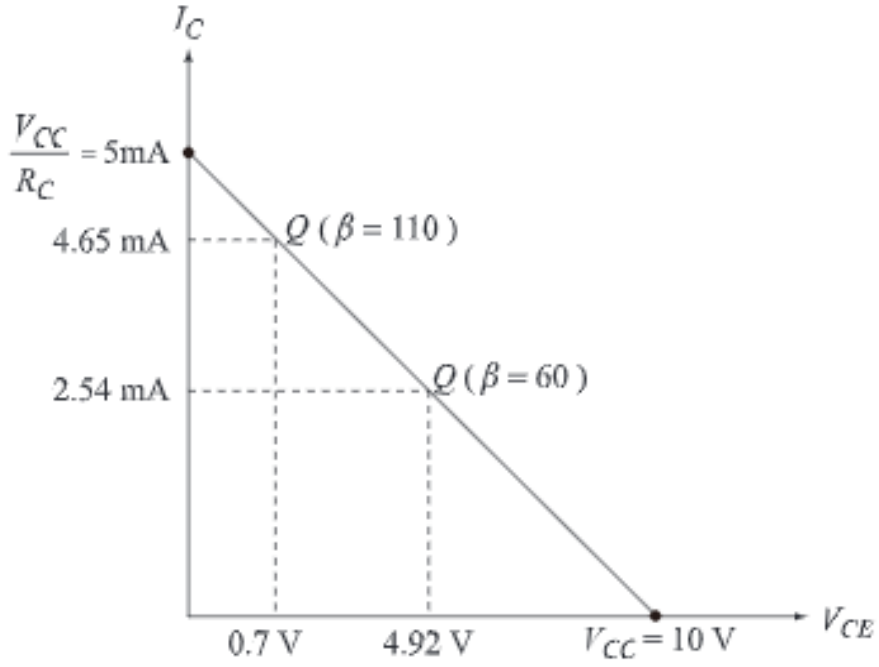
I_{BQ} is not affected by change in β.

$$I_{BQ} = 42.27\ \mu A \quad \text{[as obtained in part (a)]}$$

$$I_{CQ} = \beta I_{BQ} = 110 \times 42.27\ \mu A = 4.65\ mA$$

$$V_{CEQ} = V_{CC} - I_{CQ} R_C = 10\ V - (4.65\ mA \times 2\ k\Omega) = 0.7\ V$$

β	I_{BQ}	I_{CQ}	V_{CEQ}
60	42.27 μA	2.54 mA	4.92 V
110	42.27 μA	4.65 mA	0.7 V



Fixed Bias Configuration: Numericals

2. For the fixed bias circuit shown, find collector current, collector resistance, base resistance and V_{CE}. Assume β = 80 and V_{BE} = 0.7V

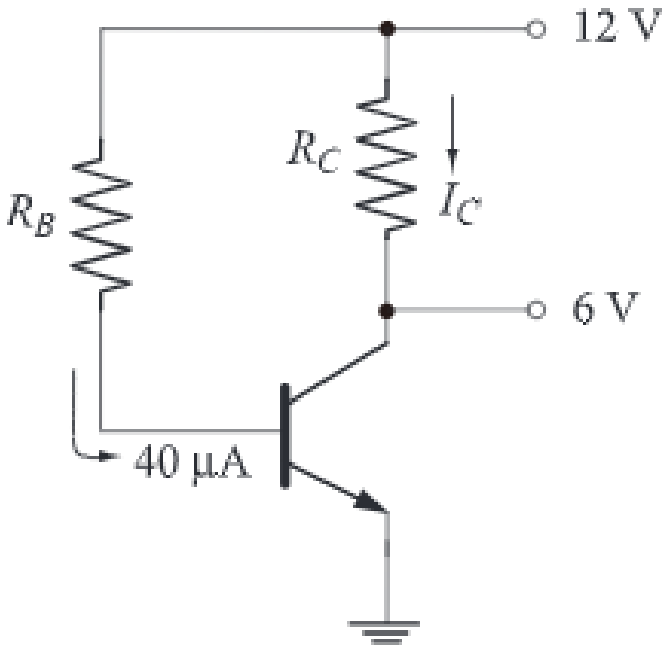
Given Data:

V_{CC} = 12V, I_B = 40 µA, V_C = 6V

a. Collector Current

$$I_C = \beta * I_B$$

$$I_C = (80)*(40\ \mu A) = 3.2\ mA$$



Circuit Diagram

Fixed Bias Configuration: Numericals

Given Data:

$V_{CC} = 12V,\ I_B = 40\ \mu A,\ V_C = 6V = V_{CE}$

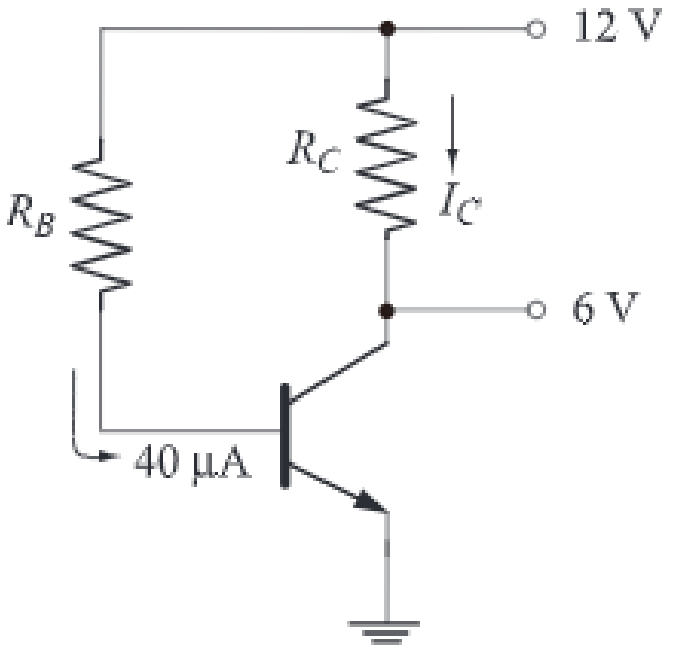
b. Collector Resistance

$$V_{CC} - I_C R_C - V_{CE} = 0$$

$$I_C R_C = V_{CC} - V_{CE}$$

$$R_C = \frac{V_{CC} - V_{CE}}{I_C}$$

$$R_C = \frac{12 - 6}{3.2mA} = 1.875k\Omega$$



Circuit Diagram

Fixed Bias Configuration: Numericals

Given Data:

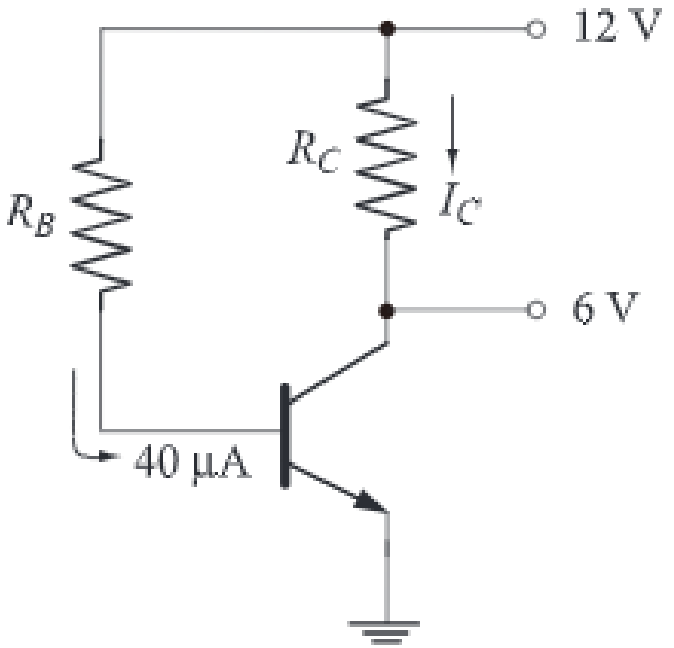
$V_{CC} = 12V,\ I_B = 40\ \mu A,\ V_C = 6V = V_{CE}$

c. Base Resistance

$$V_{CC} - I_B R_B - V_{BE} = 0$$

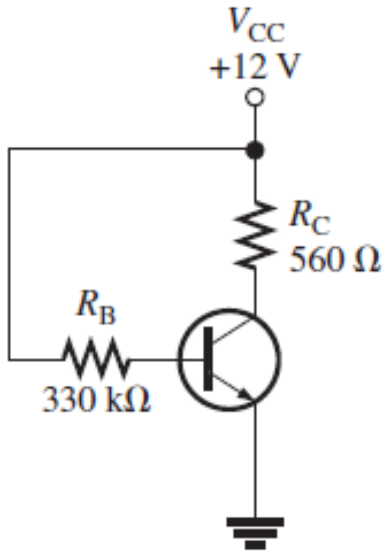
$$R_B = \frac{V_{CC} - V_{BE}}{I_B}$$

$$R_B = \frac{12 - 0.7}{40\mu A} = 282.5k\Omega$$



Circuit Diagram

Determine how much the Q-point (I_C, V_{CE}) for the circuit in Figure 5–20 will change over a temperature range where β_{DC} increases from 100 to 200.



For $\beta_{DC} = 100$,

$$I_{C(1)} = \beta_{DC}\left(\frac{V_{CC} - V_{BE}}{R_B}\right) = 100\left(\frac{12\text{ V} - 0.7\text{ V}}{330\text{ k}\Omega}\right) = 3.42\text{ mA}$$

$$V_{CE(1)} = V_{CC} - I_{C(1)}R_C = 12\text{ V} - (3.42\text{ mA})(560\ \Omega) = 10.1\text{ V}$$

For $\beta_{DC} = 200$,

$$I_{C(2)} = \beta_{DC}\left(\frac{V_{CC} - V_{BE}}{R_B}\right) = 200\left(\frac{12\text{ V} - 0.7\text{ V}}{330\text{ k}\Omega}\right) = 6.84\text{ mA}$$

$$V_{CE(2)} = V_{CC} - I_{C(2)}R_C = 12\text{ V} - (6.84\text{ mA})(560\ \Omega) = 8.17\text{ V}$$

The percent change in I_C as β_{DC} changes from 100 to 200 is

$$\%\Delta I_C = \left(\frac{I_{C(2)} - I_{C(1)}}{I_{C(1)}}\right)100\%$$

$$= \left(\frac{6.84\text{ mA} - 3.42\text{ mA}}{3.42\text{ mA}}\right)100\% = \mathbf{100\%}\text{ (an increase)}$$

The percent change in V_{CE} is

$$\%\Delta V_{CE} = \left(\frac{V_{CE(2)} - V_{CE(1)}}{V_{CE(1)}}\right)100\%$$

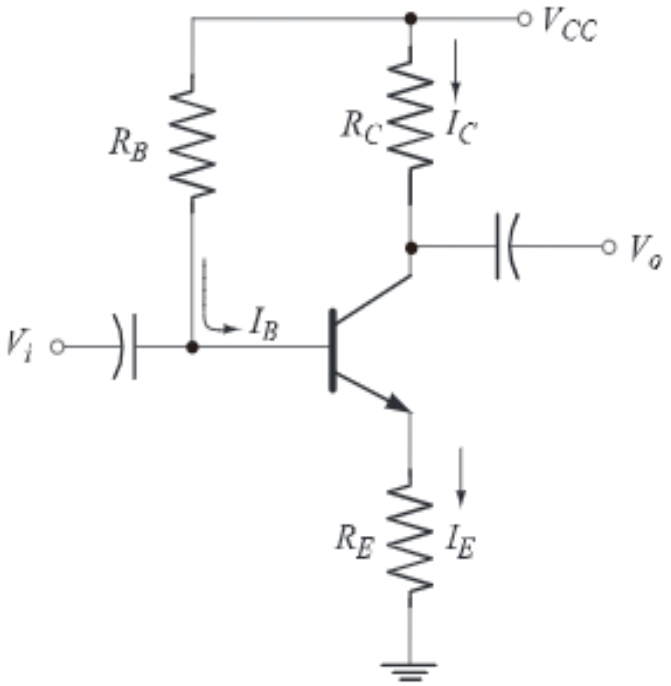
$$= \left(\frac{8.17\text{ V} - 10.1\text{ V}}{10.1\text{ V}}\right)100\% = \mathbf{-19.1\%}\text{ (a decrease)}$$

As you can see, the Q-point is very dependent on β_{DC} in this circuit and therefore makes the base-bias arrangement very unreliable for linear circuits,

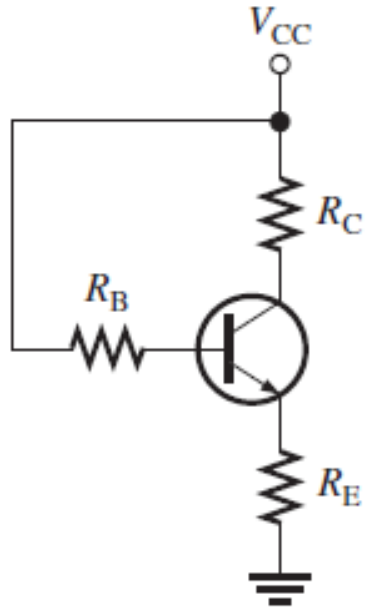
but it can be used in switching applications.

Emitter Stabilized Bias Configuration

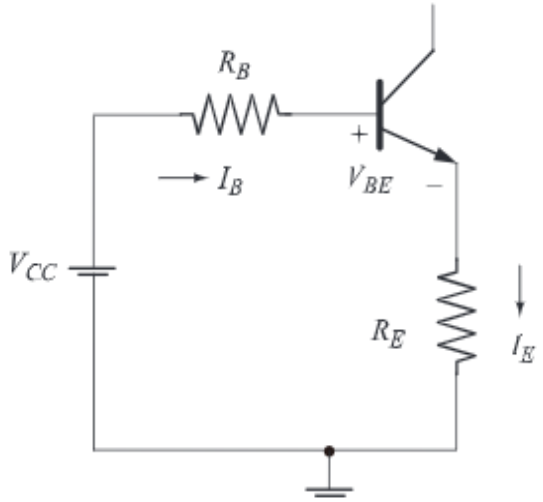
For the dc analysis we can replace capacitor with an open circuit (since capacitor blocks dc) because the reactance of capacitor is infinity



Emitter-feedback bias Circuit Diagram



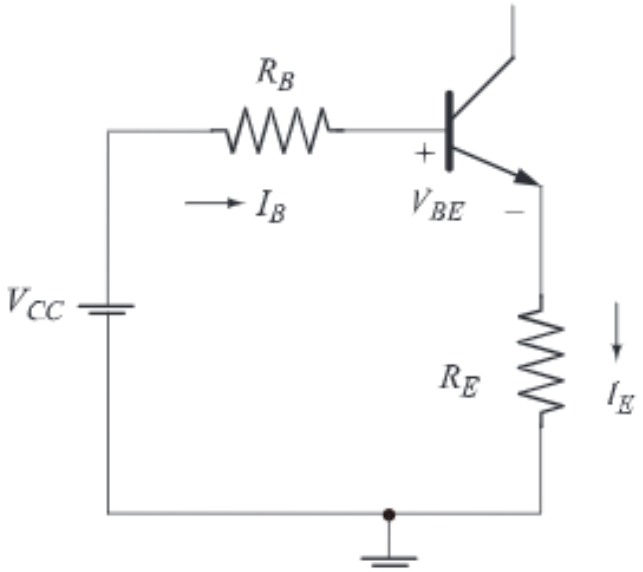
DC equivalent circuit of Emitter-feedback bias



Base-Emitter circuit

C_1 & C_2 = Coupling Capacitors
V_{CC} = Supply voltage
R_B = Base Resistance
R_C = Collector Resistance
R_E = Emitter Resistance

Emitter Stabilized Bias Configuration



Base-Emitter circuit

Apply KVL to the base circuit we get;

$$V_{CC} = I_B R_B + V_{BE} + I_E R_E$$

$$I_E = I_C + I_B$$

$$I_C = \beta I_B$$

$$I_E = \beta I_B + I_B = (1+\beta) I_B$$

$$V_{CC} = I_B R_B + V_{BE} + (1+\beta) I_B R_E$$

$$V_{CC} - V_{BE} = I_B [R_B + (1+\beta) R_E]$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (1+\beta) R_E}$$

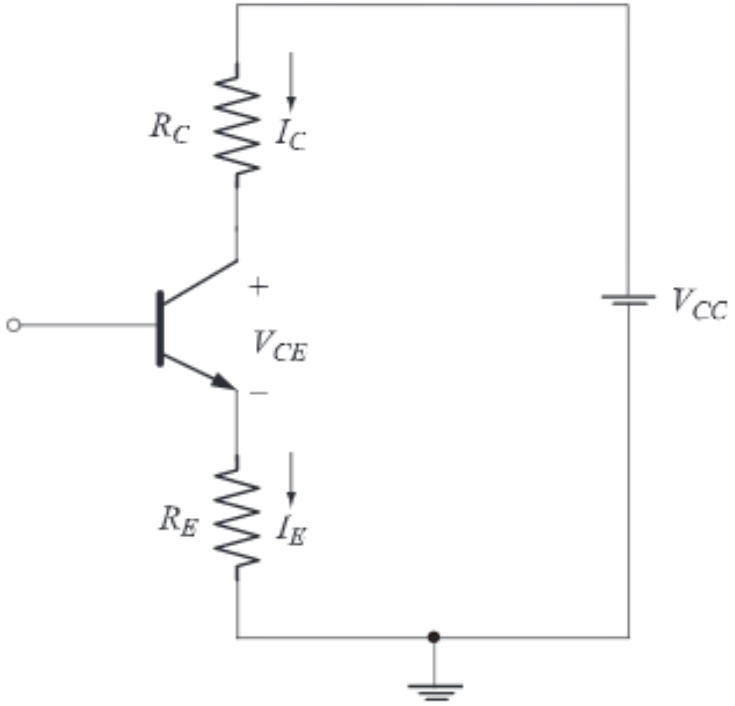
As $I_C = \beta I_B$ and $I_E \sim = I_C$

Substituting I_E/β_{DC} for I_B, you can see that I_E is still dependent on β_{DC}.

$$V_{CC} = I_B R_B + V_{BE} + I_E R_E$$

$$I_E = \frac{V_{CC} - V_{BE}}{R_E + R_B/\beta}$$

Emitter Stabilized Bias Configuration



Collector-Emitter circuit

Apply KVL to the Collector circuit we get;

$$V_{CC} = I_C R_C + V_{CE} + I_E R_E$$

$$I_E \sim = I_C$$

$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$

Voltage across emitter:

$$V_E = I_E R_E$$

$$V_C = V_{CE} + I_E R_E$$

$$V_C = V_{CE} + V_E$$

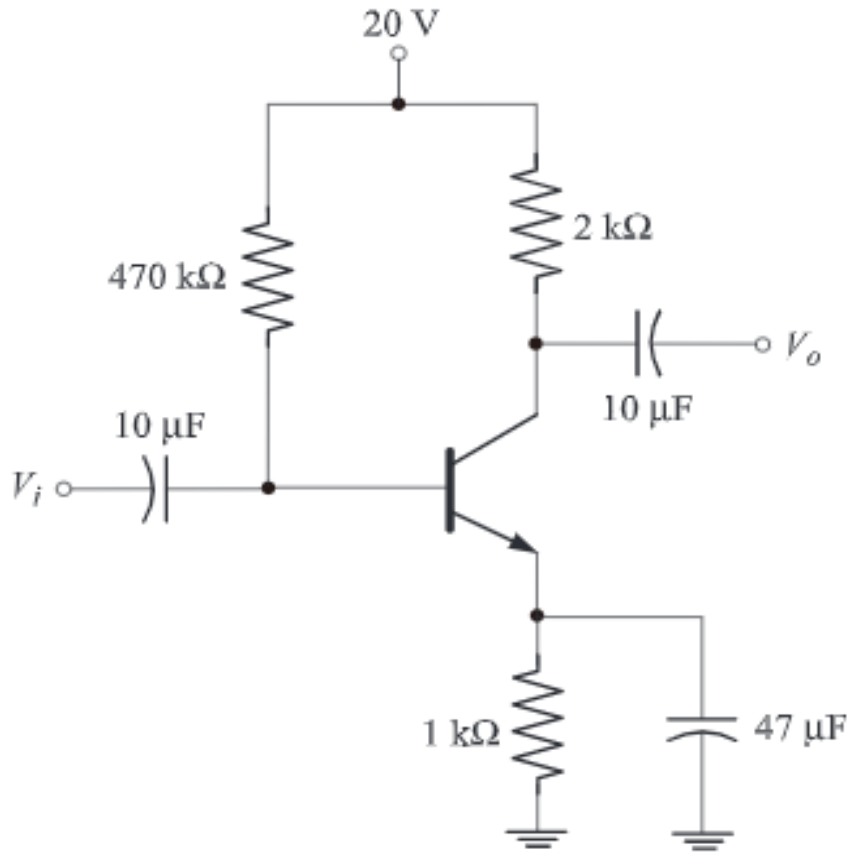
Emitter Stabilized Bias Configuration

1. For the emitter-bias shown using silicon transistor with V_{BE} = 0.7 V and β = 60, find;

a. Base current and collector current
b. Collector-Emitter voltage
c. Collector, emitter and base voltages to ground
d. Base-collector voltage

Given Data:

V_{CC} = 20V
R_B = 470kΩ
R_C = 2kΩ
$C_1 = C_2$ = 10μF
R_E = 1kΩ
C_E = 47μF



Circuit Diagram

Emitter Stabilized Bias Configuration

For the dc analysis we can replace capacitor with an open circuit (since capacitor blocks dc) because the reactance of capacitor is infinity

Given Data:

V_{CC} = 20V, R_B = 470kΩ, R_C = 2kΩ, C_1 = C_2 = 10μF

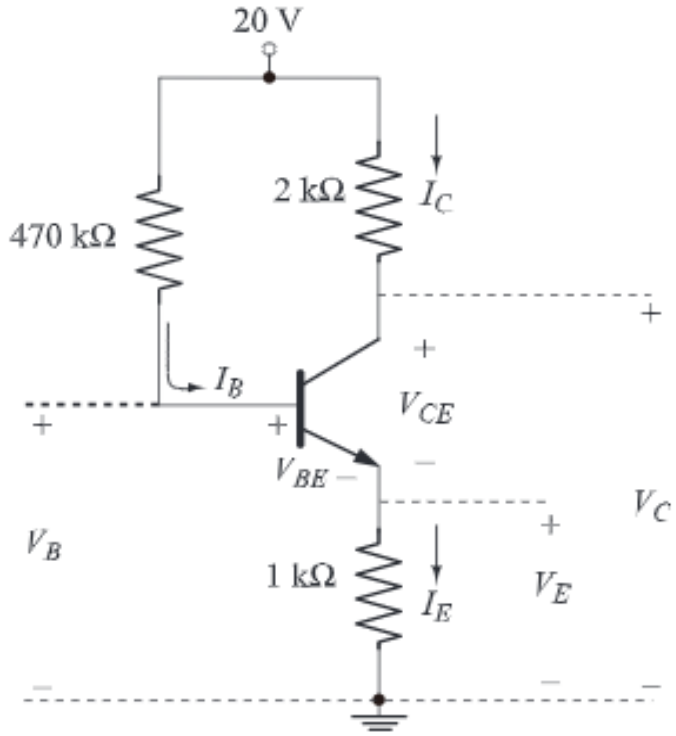
R_E = 1kΩ, C_E = 47μF

a. Base current and collector current

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (1+\beta)R_E}$$

$$I_B = \frac{20 - 0.7}{470k + (1+60)1k} = 36.34\mu A$$

$I_C = \beta * I_B = 60 * 36.34\mu = 2.18mA$



DC Equivalent Circuit Diagram

Emitter Stabilized Bias Configuration

Given Data:

$V_{CC} = 20V, R_B = 470k\Omega, R_C = 2k\Omega, C_1 = C_2 = 10\mu F, R_E = 1k\Omega, C_E = 47\mu F$

b. Collector-emitter voltage

$$V_{CE} = V_{CC} - I_C(R_C+R_E)$$

$$V_{CE} = 20 - 2.18m(2k+1k) = 13.46V$$

c. Collector, emitter and base voltages to ground

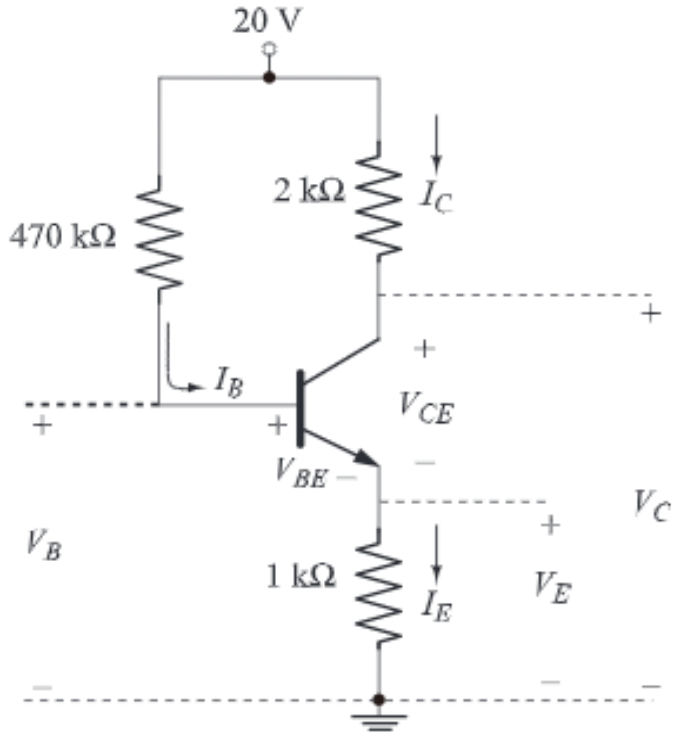
$$V_C = V_{CC} - I_C R_C = 20 - (2.18m*2k) = 15.64V$$

$$V_E = V_C - V_{CE} = 15.64 - 13.46 = 2.18V$$

$$V_B = V_{BE} + V_E = 0.7 + 2.18 = 2.88V$$

d. Base-collector voltage

$$V_{BC} = V_B - V_C = 2.88 - 15.64 = -12.76V$$



DC Equivalent Circuit Diagram

Emitter Stabilized Bias Configuration

2. For the emitter bias circuit shown using silicon transistor V_{BE} = 0.7 V and β = 100. Find;

a. Quiescent values of base current, collector current and collector to emitter voltage.

b. Voltage at collector, base and emitter with respect to ground.

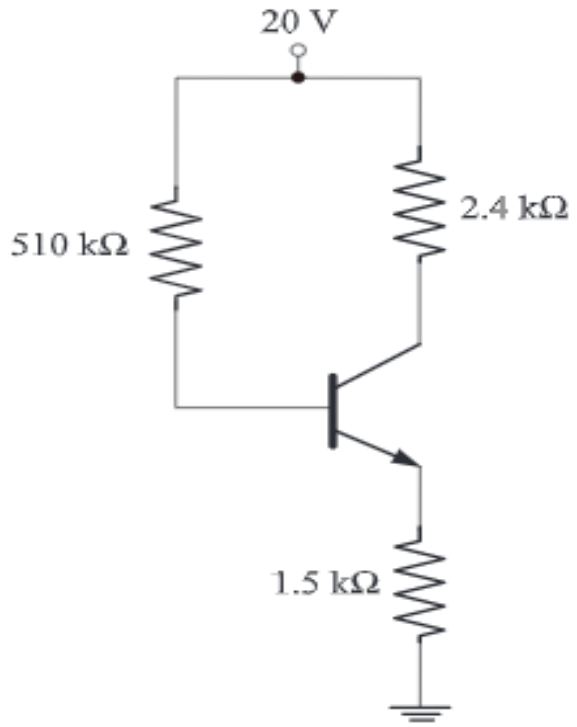
Given Data:

V_{CC} = 20V

R_B = 510kΩ

R_C = 2.4kΩ

R_E = 1.5kΩ



Circuit Diagram

Emitter Stabilized Bias Configuration

Given Data:

V_{CC} = 20V, R_B = 510kΩ, R_C = 2.4kΩ, R_E = 1.5kΩ

a. Base current, collector current and V_{CE}.

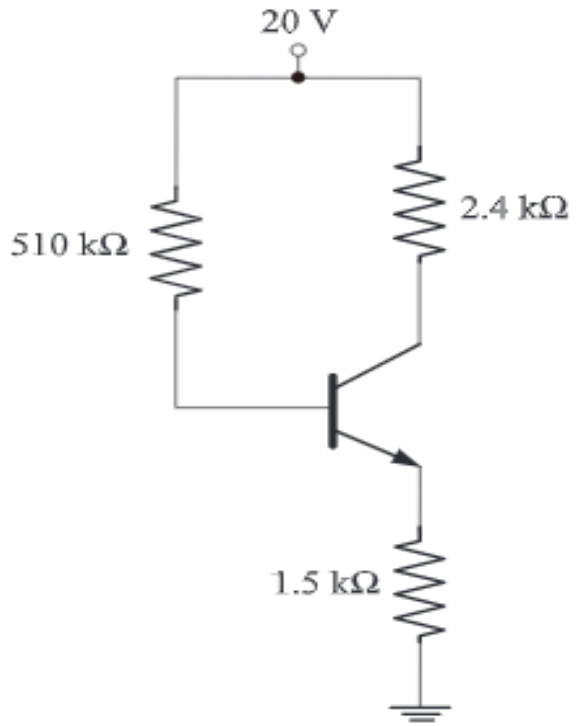
$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (1+\beta)R_E}$$

$$I_B = \frac{20 - 0.7}{510k + (1+100)1.5k} = 29.18\mu A$$

$I_C = \beta * I_B = 100 * 29.18\mu = 2.92mA$

$V_{CE} = V_{CC} - I_C(R_C + R_E)$

$V_{CE} = 20 - 2.92m(2.4k + 1.5k) = 8.61V$



Circuit Diagram

Emitter Stabilized Bias Configuration

Given Data:

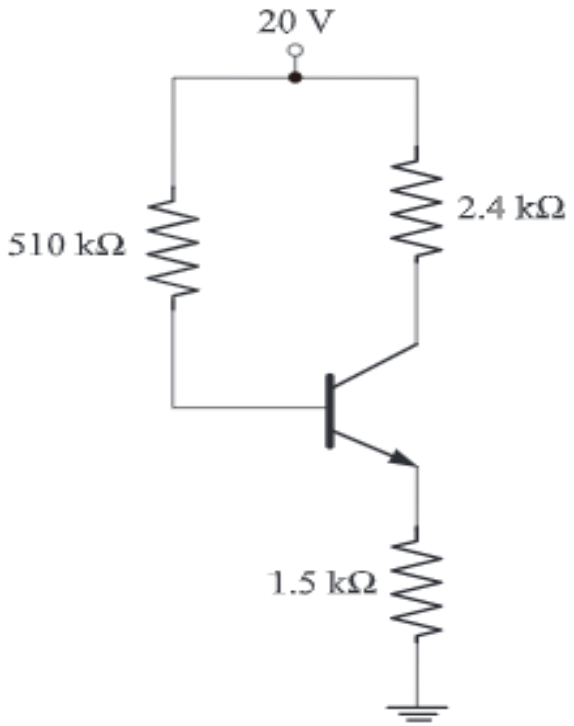
$V_{CC} = 20V, R_B = 510k\Omega, R_C = 2.4k\Omega, R_E = 1.5k\Omega$

b. Collector, emitter and base voltages to ground

$$V_C = V_{CC} - I_C R_C = 20 - (2.92m * 2.4k) = 13V$$

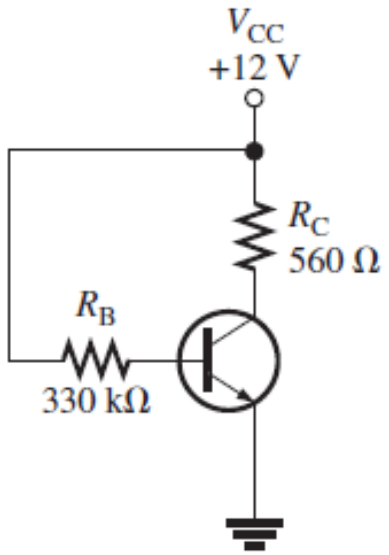
$$V_E = V_C - V_{CE} = 13 - 8.61 = 4.39V$$

$$V_B = V_{BE} + V_E = 0.7 + 4.39 = 5.09V$$



Circuit Diagram

Determine how much the Q-point (I_C, V_{CE}) for the circuit in Figure 5–20 will change over a temperature range where β_{DC} increases from 100 to 200.



The base-bias circuit from Example 5–8 is converted to emitter-feedback bias by the addition of a 1 kΩ emitter resistor. All other values are the same, and a transistor with a $\beta_{DC} = 100$ is used. Determine how much the Q-point will change if the first transistor is replaced with one having a $\beta_{DC} = 200$. Compare the results to those of the base-bias circuit.

For $\beta_{DC} = 100$,

$$I_{C(1)} = I_E = \frac{V_{CC} - V_{BE}}{R_E + R_B/\beta_{DC}} = \frac{12\text{ V} - 0.7\text{ V}}{1\text{ k}\Omega + 330\text{ k}\Omega/100} = 2.63\text{ mA}$$

$$V_{CE(1)} = V_{CC} - I_{C(1)}(R_C + R_E) = 12\text{ V} - (2.63\text{ mA})(560\ \Omega + 1\text{ k}\Omega) = 7.90\text{ V}$$

For $\beta_{DC} = 200$,

$$I_{C(2)} = I_E = \frac{V_{CC} - V_{BE}}{R_E + R_B/\beta_{DC}} = \frac{12\text{ V} - 0.7\text{ V}}{1\text{ k}\Omega + 330\text{ k}\Omega/200} = 4.26\text{ mA}$$

$$V_{CE(2)} = V_{CC} - I_{C(2)}(R_C + R_E) = 12\text{ V} - (4.26\text{ mA})(560\ \Omega + 1\text{ k}\Omega) = 5.35\text{ V}$$

The percent change in I_C is

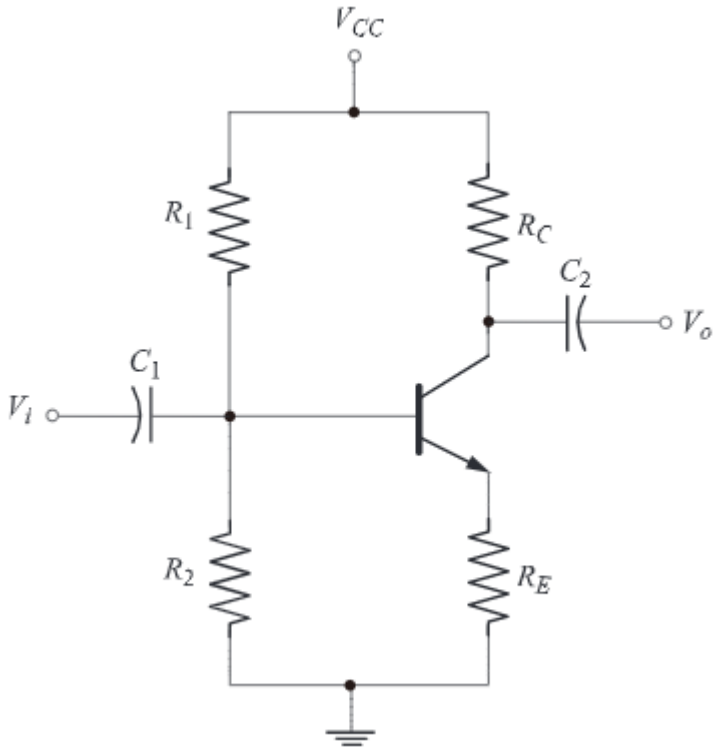
$$\%\Delta I_C = \left(\frac{I_{C(2)} - I_{C(1)}}{I_{C(1)}}\right)100\% = \left(\frac{4.26\text{ mA} - 2.63\text{ mA}}{2.63\text{ mA}}\right)100\% = \mathbf{62.0\%}$$

$$\%\Delta V_{CE} = \left(\frac{V_{CE(2)} - V_{CE(1)}}{V_{CE(1)}}\right)100\% = \left(\frac{5.35\text{ V} - 7.90\text{ V}}{7.90\text{ V}}\right)100\% = \mathbf{-32.3\%}$$

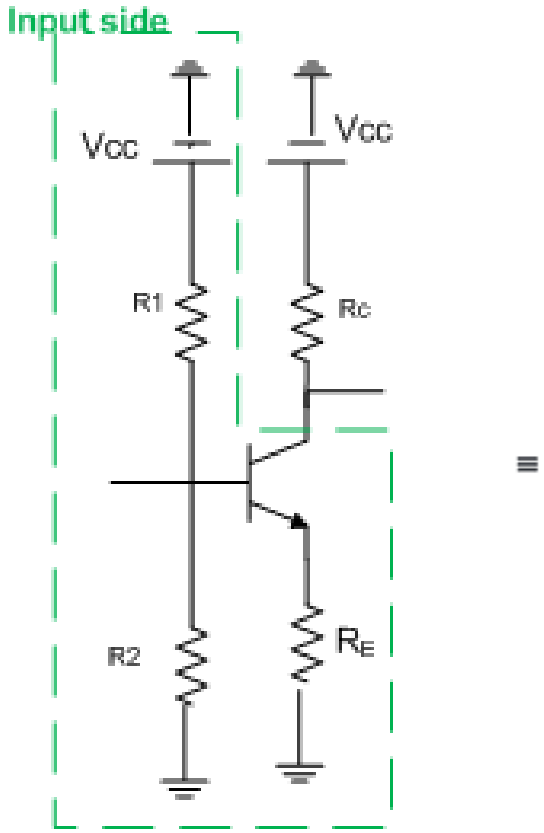
Although the emitter-feedback bias significantly improved the stability of the bias for a change in β_{DC} compared to base bias, it still does not provide a reliable Q-point.

Voltage Divider Bias Configuration

For the dc analysis we can replace capacitor with an open circuit (since capacitor blocks dc) because the reactance of capacitor is infinity



Circuit Diagram

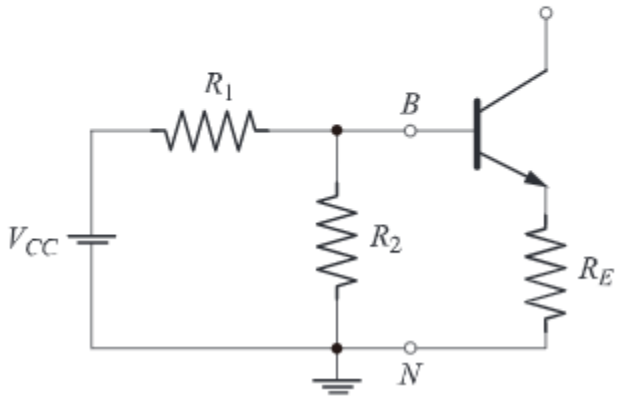


DC equivalent circuit of fixed bias

The two methods of Analysis:

1. **Exact Analysis Method**
2. **Approximate Analysis Method**

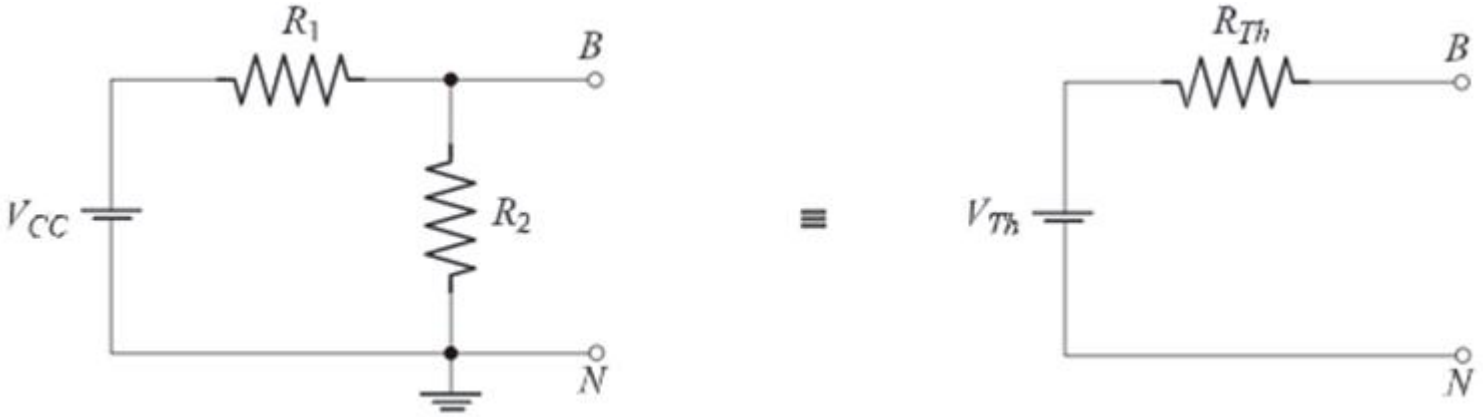
Redraw the input side, we will get



Base circuit

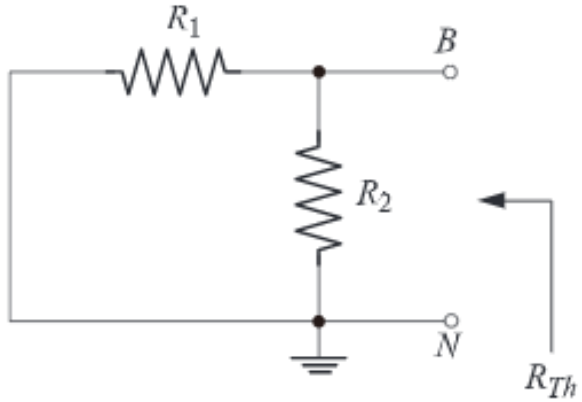
Voltage Divider Bias Configuration: Exact Analysis

Thevenin's Theorem Applied to Voltage-Divider Bias



Thevenin Equivalent Circuit

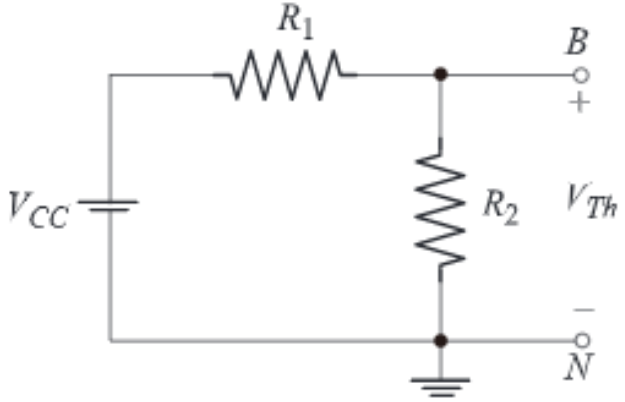
Apply Thevenin's theorem to the circuit left of point B, with V_{CC} replaced by a short to ground and the transistor disconnected from the circuit.



Determination of R_{Th}

$$R_{Th} = R_1 \parallel R_2$$

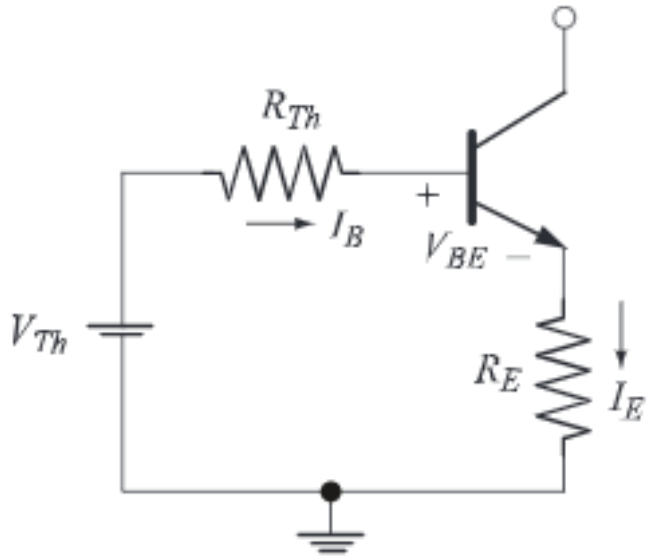
$$R_{Th} = \frac{R_1 R_2}{R_1 + R_2}$$



Determination of V_{Th}

$$V_{Th} = VCC \frac{R_2}{R_1 + R_2}$$

Voltage Divider Bias Configuration: Exact Analysis



Base Circuit with Thevenin Equivalent

Apply KVL to the base circuit we get;

$$V_{Th} - I_B R_{Th} - V_{BE} - I_E R_E = 0$$

$$V_{Th} = I_B R_{Th} + V_{BE} + I_E R_E$$

$$I_E = I_C + I_B$$

$$I_C = \beta I_B$$

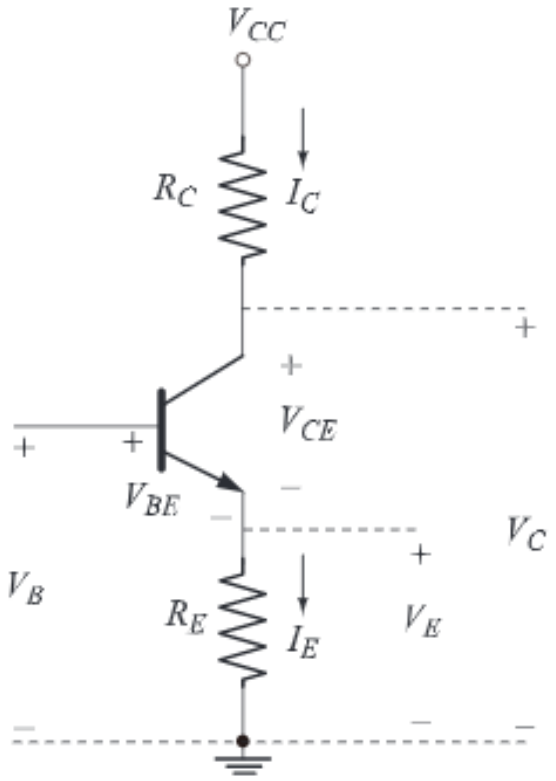
$$I_E = \beta I_B + I_B = (1+\beta) I_B$$

$$V_{Th} = I_B R_{Th} + V_{BE} + (1+\beta) I_B R_E$$

$$V_{Th} - V_{BE} = I_B [R_{Th} + (1+\beta) R_E]$$

$$I_B = \frac{V_{Th} - V_{BE}}{R_{Th} + (1+\beta) R_E}$$

Voltage Divider Bias Configuration: Exact Analysis



Collector Circuit

Apply KVL to the base circuit we get;

$$V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0$$

$$V_{CC} = I_C R_C + V_{CE} + I_E R_E$$

$$I_E = I_C$$

$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$

Voltage across emitter:

$$V_E = I_E R_E$$

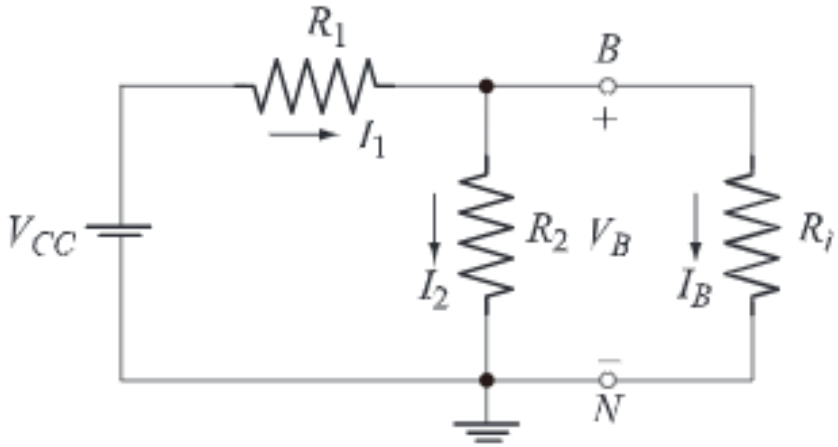
Collector to ground Voltage:

$$V_C = V_{CE} + I_E R_E = V_{CE} + V_E$$

Base to ground Voltage:

$$V_B = V_{BE} + V_E$$

Voltage Divider Bias Configuration: Approximate Analysis



Input Circuit

Apply KCL to the base circuit we get;

$$I_1 = I_2 + I_B$$

$$R_i = (1+\beta)\, R_E \approx \beta R_E, \quad \beta >> 1$$

$$I_B = \frac{V_B}{R_i} \quad and \quad I_2 = \frac{V_B}{R_2}$$

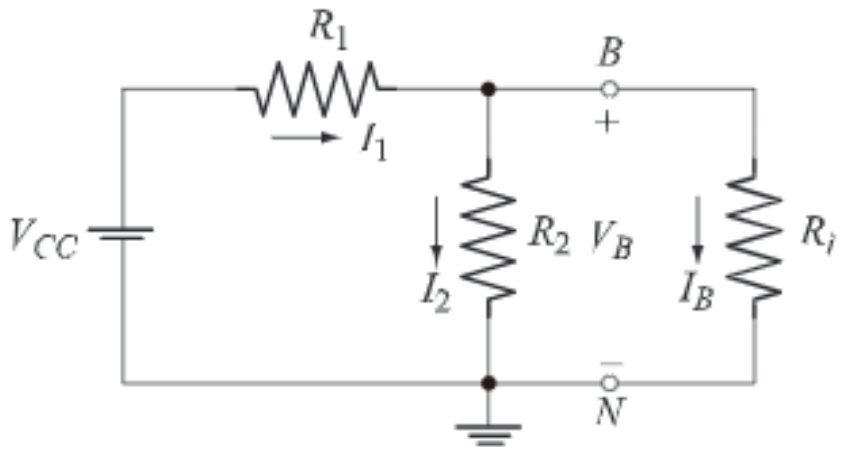
If $R_i = (1+\beta)\, R_E >> 10\, R_2$,

Then $I_B << 0.1 * I_2$

We neglect I_B, then

$$I_1 \approx I_2$$

Voltage Divider Bias Configuration: Approximate Analysis



Input Circuit

Apply KVL to the circuit we get;

$$V_{CC} = I_1R_1 + I_2R_2$$

$$V_{CC} = I_2(R_1+R_2)$$

$$I_2 = \frac{V_{CC}}{R_1 + R_2}$$

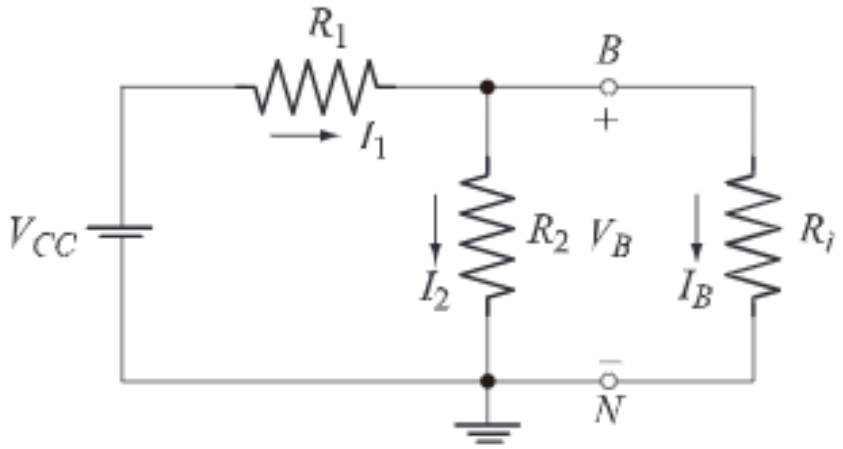
$$V_B = I_2 * R_2$$

$$V_B = \frac{V_{CC}R_2}{R_1 + R_2}$$

$$V_B = V_{BE} + V_E$$

$$V_E = V_B - V_{BE}$$

Voltage Divider Bias Configuration: Approximate Analysis



Input Circuit

Apply KCL to the Collector Circuit circuit we get;

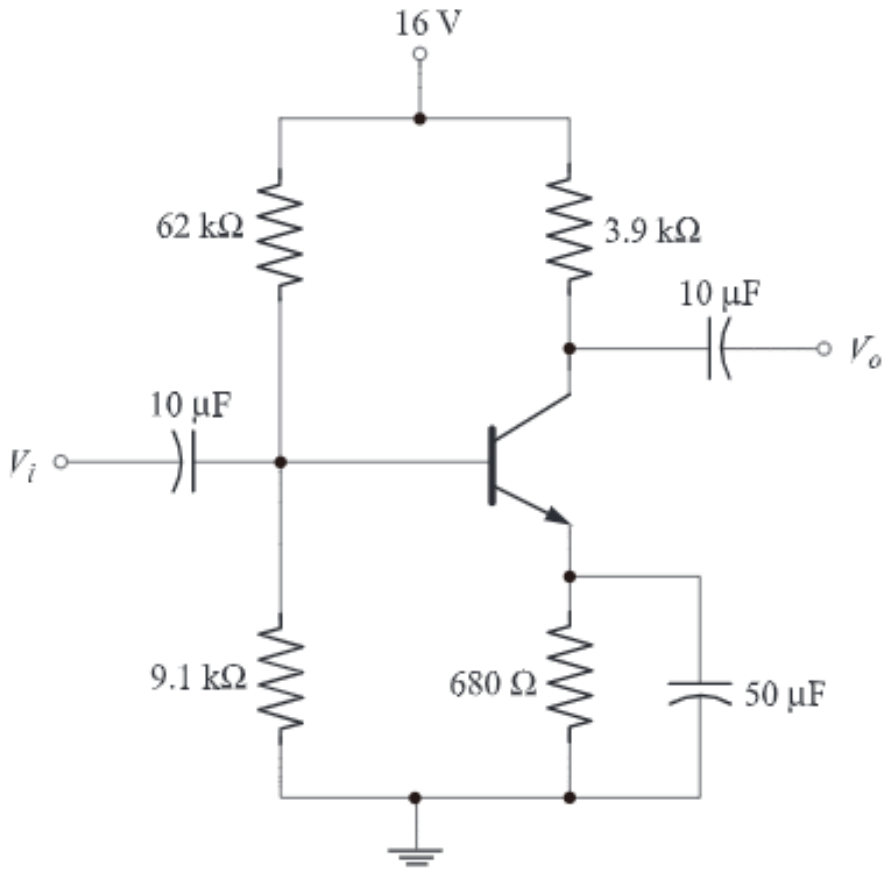
$$I_E = \frac{V_E}{R_E} \quad and \quad IC \approx I_E$$

$$V_{CE} = V_{CC} - I_C R_C - I_E R_E$$

$$V_{CE} = V_{CC} - I_C (R_C + R_E)$$

Voltage Divider Bias Configuration: Numericals

a. Find the quiescent base current, collector current and V_{CE} for the circuit shown using silicon transistor with $V_{BE} = 0.7V$ and $\beta = 80$.
b. Determine the values of collector, emitter and base voltages with respect to ground.
c. Repeat (a) for $\beta = 150$.
d. Draw the dc load line and locate the Q-points corresponding to two 'β' values.



Given:

$V_{CC} = 16V$,
$R_1 = 62k\Omega$,
$R_2 = 9.1k\ \Omega$,
$R_C = 3.9k\ \Omega$,
$R_E = 680\ \Omega$,
$C_1 = C_2 = 10\mu F$, $C_E = 50\mu F$

Voltage Divider Bias Configuration: Numericals

a. Find the quiescent base current, collector current and V_{CE} for the circuit shown using silicon transistor with $V_{BE} = 0.7V$ and $\beta = 80$.

Given:

$V_{CC} = 16V$, $R_1 = 62k\Omega$, $R_2 = 9.1k\ \Omega$, $R_C = 3.9k\ \Omega$, $R_E = 680\ \Omega$, $C_1 = C_2 = 10\mu F$, $C_E = 50\mu F$

$$R_{Th} = \frac{R_1 R_2}{R_1 + R_2}$$

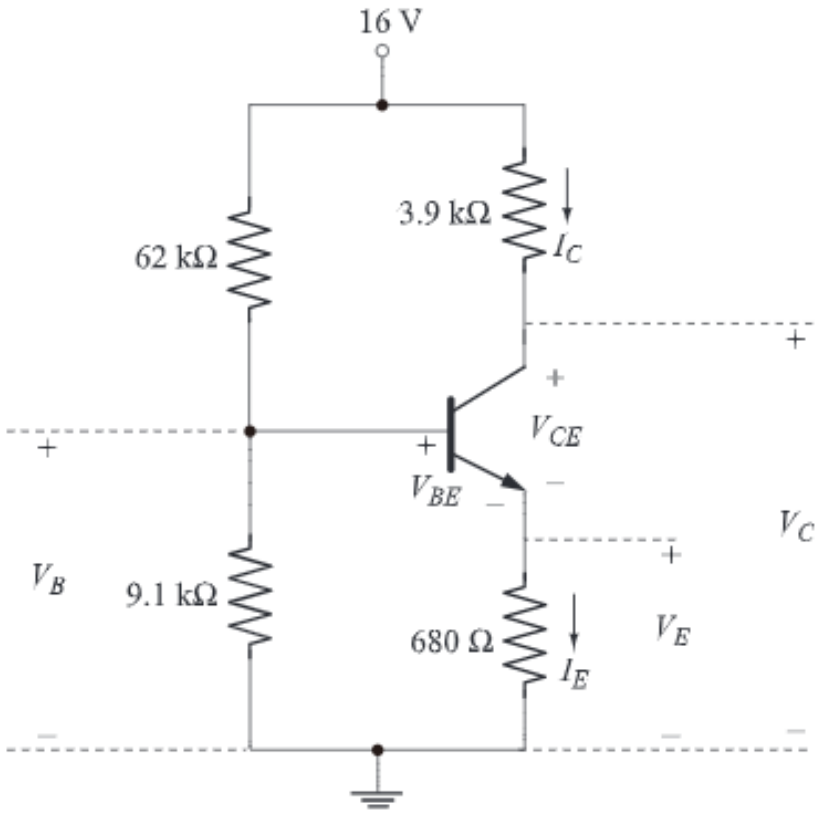
$$R_{Th} = \frac{62k * 9.1k}{62k + 9.1k}$$

$$R_{Th} = 7.94k\Omega$$

$$V_{Th} = V_{CC}\frac{R_2}{R_1 + R_2}$$

$$V_{Th} = \frac{16 * 9.1k}{62k + 9.1k}$$

$$V_{Th} = 2.05V$$



Voltage Divider Bias Configuration: Numericals

Given:

V_{CC} = 16V, R_1 = 62kΩ, R_2 = 9.1k Ω, R_C = 3.9k Ω,
R_E = 680 Ω, C_1 = C_2 = 10μF, C_E = 50μF

$$I_B = \frac{V_{Th} - V_{BE}}{R_{Th} + (1+\beta)R_E}$$

$$I_B = \frac{2.05 - 0.7}{7.94k + (1+80)680}$$

$$I_B = 21.42\mu A$$

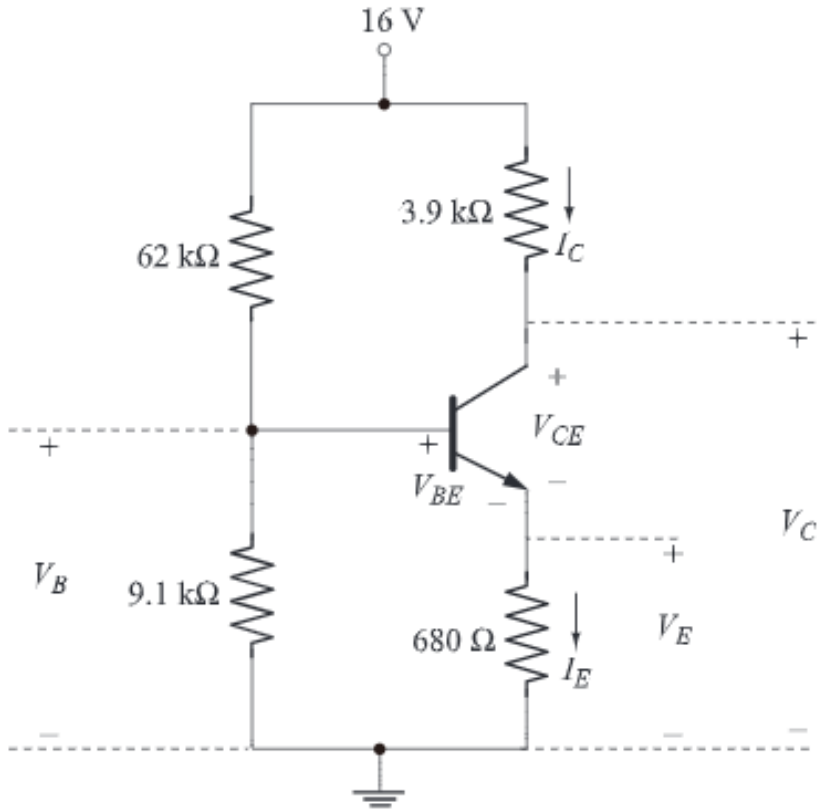
$$I_C = \beta I_B$$

I_C = 80 * 21.42 μ = 1.71 mA

$$V_{CE} = V_{CC} - I_C (R_C + R_E)$$

V_{CE} = 16 – 1.71m(3.9k+680)

V_{CE} = 8.17V



Voltage Divider Bias Configuration: Numericals

Given:

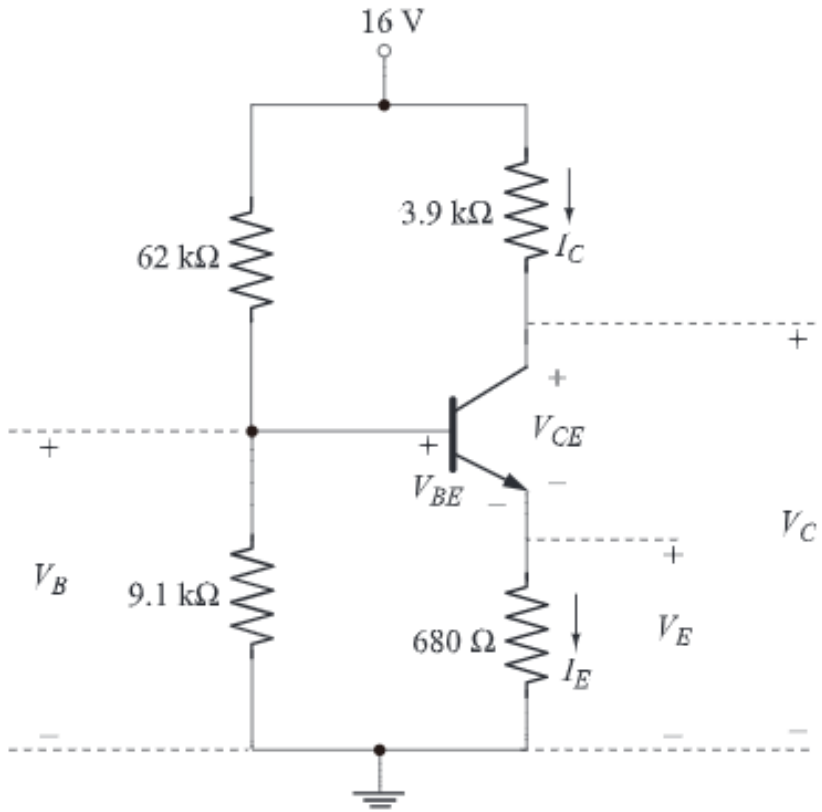
$V_{CC} = 16V, R_1 = 62k\Omega, R_2 = 9.1k\ \Omega, R_C = 3.9k\ \Omega,$
$R_E = 680\ \Omega, C_1 = C_2 = 10\mu F, C_E = 50\mu F$

b. collector, emitter and base voltages with respect to ground.

$V_C = V_{CC} - I_C R_C = 16 - (1.71m * 3.9k) =$ **9.33 V**

$V_E = I_E R_E \approx I_C R_C = (1.71m * 3.9k) =$ **1.16 V**

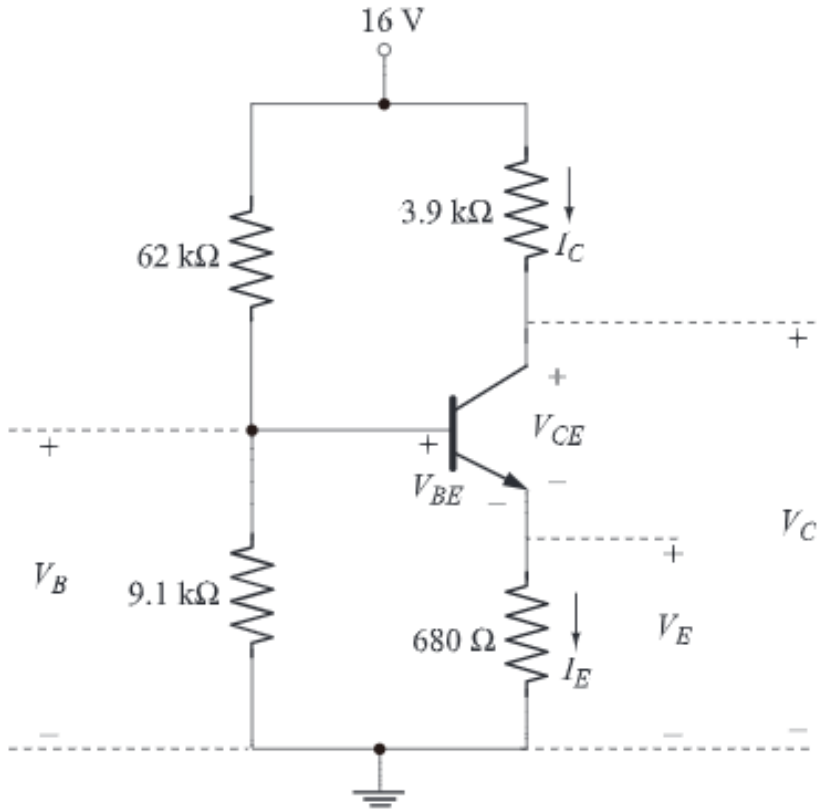
$V_B = V_{BE} + V_E = 0.7 + 1.16 =$ **1.86V**



Voltage Divider Bias Configuration: Numericals

Given:

V_{CC} = 16V, R_1 = 62kΩ, R_2 = 9.1k Ω, R_C = 3.9k Ω,
R_E = 680 Ω, C_1 = C_2 = 10μF, C_E = 50μF



c. For β = 150

$$I_B = \frac{V_{Th} - V_{BE}}{R_{Th} + (1+\beta)R_E}$$

$$I_B = \frac{2.05 - 0.7}{7.94k + (1+150)680}$$

$$I_B = 12.2\mu A$$

$$I_C = \beta I_B$$

$$I_C = 150 * 12.2\ \mu = 1.83\ mA$$

$$V_{CE} = V_{CC} - I_C\,(R_C + R_E)$$

$$V_{CE} = 16 - 1.83m(3.9k + 680)$$

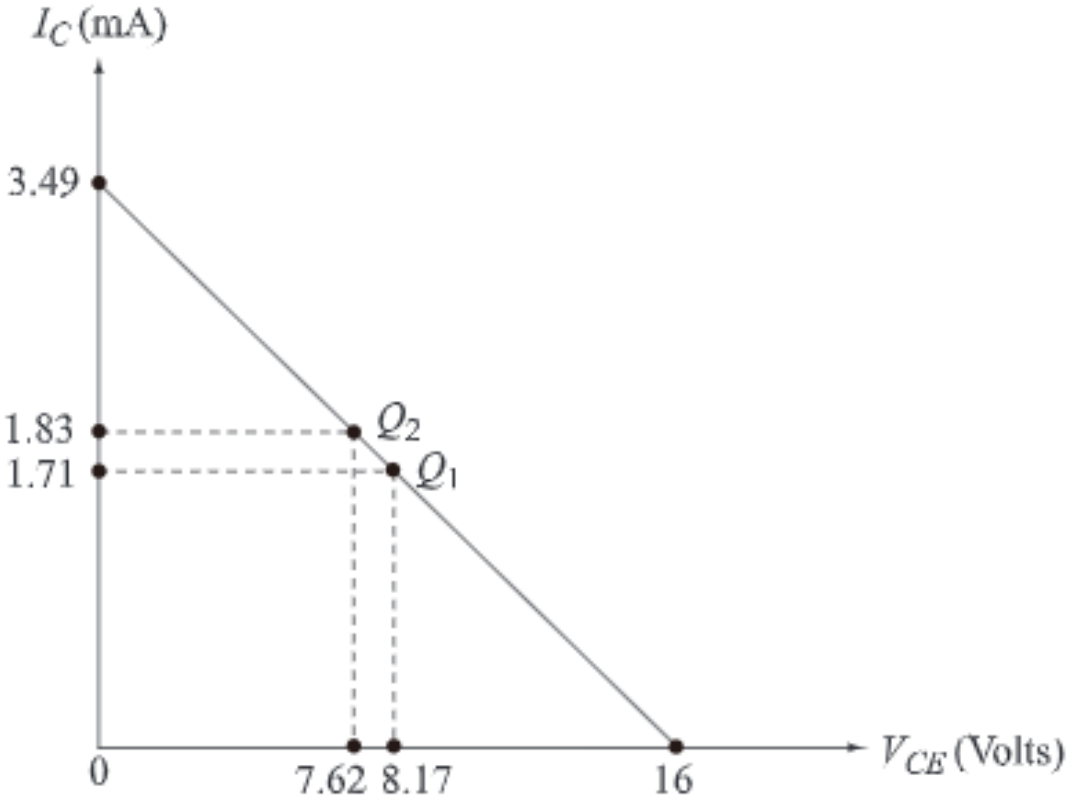
$$V_{CE} = 7.62V$$

Voltage Divider Bias Configuration: Numericals

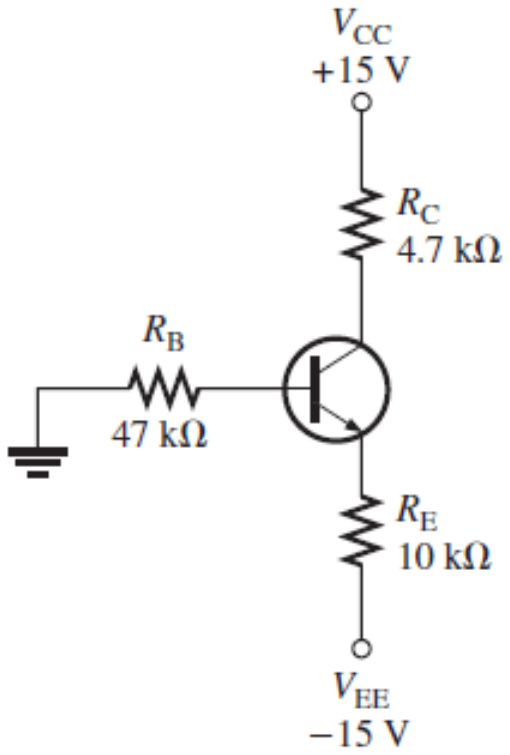
d. DC load line curve

$$I_{C(sat)} = \frac{V_{CC}}{R_C + R_E} = \frac{16}{3.9k + 680} = 3.49mA$$

β	I_{BQ}	I_{CQ}	V_{CEQ}
80	21.42 µA	1.71 mA	8.17 V
150	12.2 µA	1.83 mA	7.62 V



Determine how much the Q-point (I_C, V_{CE}) for the circuit in Figure 5–18 will change if β_{DC} increases from 100 to 200 when one transistor is replaced by another.



For $\beta_{DC} = 100$,

$$I_{C(1)} \cong I_E = \frac{-V_{EE} - V_{BE}}{R_E + R_B/\beta_{DC}} = \frac{-(-15\text{ V}) - 0.7\text{ V}}{10\text{ k}\Omega + 47\text{ k}\Omega/100} = 1.37\text{ mA}$$

$$V_C = V_{CC} - I_{C(1)}R_C = 15\text{ V} - (1.37\text{ mA})(4.7\text{ k}\Omega) = 8.56\text{ V}$$

$$V_E = V_{EE} + I_E R_E = -15\text{ V} + (1.37\text{ mA})(10\text{ k}\Omega) = -1.3\text{ V}$$

Therefore,

$$V_{CE(1)} = V_C - V_E = 8.56\text{ V} - (-1.3\text{ V}) = 9.83\text{ V}$$

For $\beta_{DC} = 200$,

$$I_{C(2)} \cong I_E = \frac{-V_{EE} - V_{BE}}{R_E + R_B/\beta_{DC}} = \frac{-(-15\text{ V}) - 0.7\text{ V}}{10\text{ k}\Omega + 47\text{ k}\Omega/200} = 1.38\text{ mA}$$

$$V_C = V_{CC} - I_{C(2)}R_C = 15\text{ V} - (1.38\text{ mA})(4.7\text{ k}\Omega) = 8.51\text{ V}$$

$$V_E = V_{EE} + I_E R_E = -15\text{ V} + (1.38\text{ mA})(10\text{ k}\Omega) = -1.2\text{ V}$$

Therefore,

$$V_{CE(2)} = V_C - V_E = 8.51\text{ V} - (-1.2\text{ V}) = 9.71\text{ V}$$

The percent change in I_C as β_{DC} changes from 100 to 200 is

$$\%\Delta I_C = \left(\frac{I_{C(2)} - I_{C(1)}}{I_{C(1)}}\right)100\% = \left(\frac{1.38\text{ mA} - 1.37\text{ mA}}{1.37\text{ mA}}\right)100\% = 0.730\%$$

The percent change in V_{CE} is

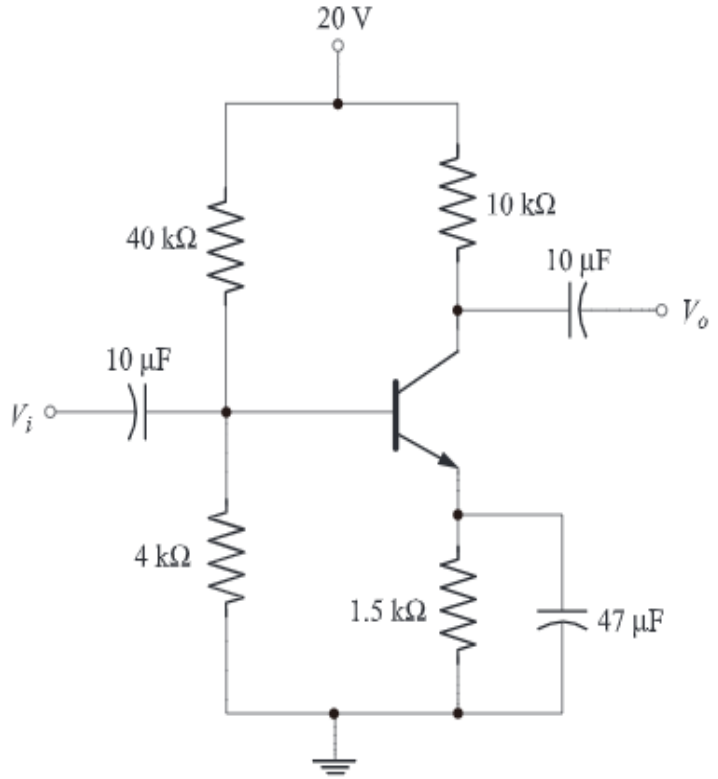
$$\%\Delta V_{CE} = \left(\frac{V_{CE(2)} - V_{CE(1)}}{V_{CE(1)}}\right)100\% = \left(\frac{9.71\text{ V} - 9.83\text{ V}}{9.83\text{ V}}\right)100\% = \mathbf{-1.22\%}$$

Voltage Divider Bias Configuration: Numericals

For the voltage divider bias configuration shown below, Find

a. I_C and V_{CE} using exact analysis
b. I_C and V_{CE} using approximate analysis
c. $I_{C(sat)}$
d. Compare the results obtained in (a) and (b) and comment

Assume silicon transistor with β = 150.



Given:

V_{CC} = 20V,
R_1 = 40kΩ,
R_2 = 4kΩ,
R_C = 10kΩ,
R_E = 1.5k Ω,
$C_1 = C_2$ = 10µF, C_E = 47µF

Voltage Divider Bias Configuration: Numericals

a. I_C and V_{CE} using exact analysis

Given:

V_{CC} = 20V, R_1 = 40kΩ, R_2 = 4k Ω, R_C = 10k Ω,
R_E = 1.5k Ω, C_1 = C_2 = 10μF, C_E = 47μF, V_{BE} = 0.7V

$$R_{Th} = \frac{R_1 R_2}{R_1 + R_2}$$

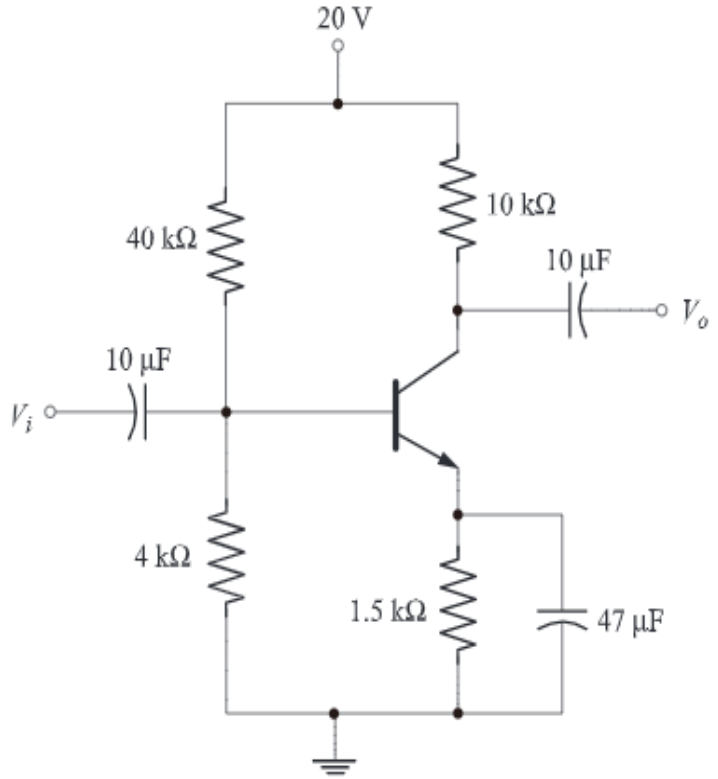
$$R_{Th} = \frac{40k * 4k}{40k + 4k}$$

$$R_{Th} = 3.63k\Omega$$

$$V_{Th} = V_{CC}\frac{R_2}{R_1 + R_2}$$

$$V_{Th} = \frac{20 * 4k}{40k + 4k}$$

$$V_{Th} = 1.82V$$



Voltage Divider Bias Configuration: Numericals

Given:

V_{CC} = 20V, R_1 = 40kΩ, R_2 = 4k Ω, R_C = 10k Ω,
R_E = 1.5k Ω, C_1 = C_2 = 10μF, C_E = 47μF, V_{BE} = 0.7V

$$I_B = \frac{V_{Th} - V_{BE}}{R_{Th} + (1+\beta)R_E}$$

$$I_B = \frac{1.82 - 0.7}{3.63k + (1+150)1.5k}$$

$$I_B = 4.86\mu A$$

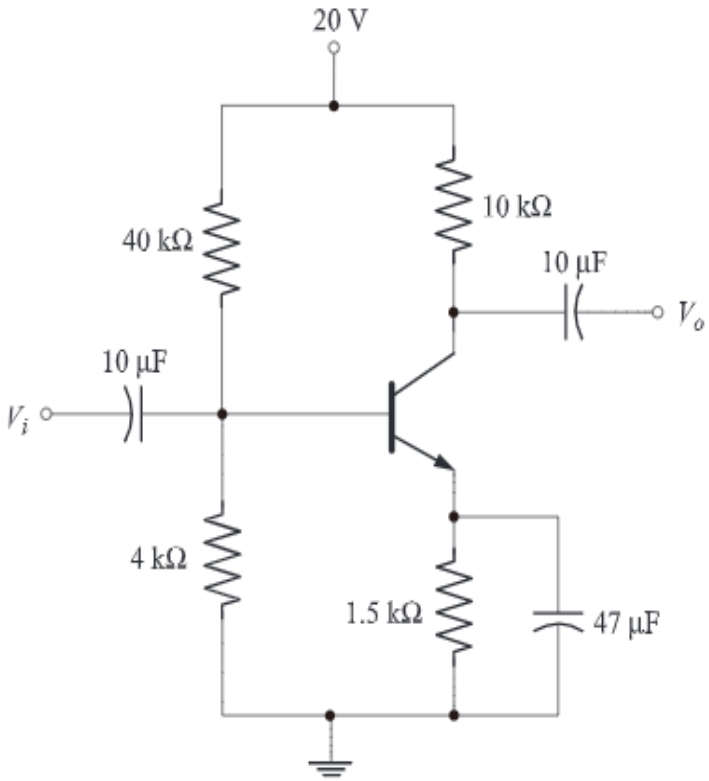
$$I_C = \beta I_B$$

I_C = 150 * 4.86 μ = 0.729 mA

$$V_{CE} = V_{CC} - I_C (R_C + R_E)$$

V_{CE} = 20 – 0.729m(10k+1.5k)

V_{CE} = 11.62V

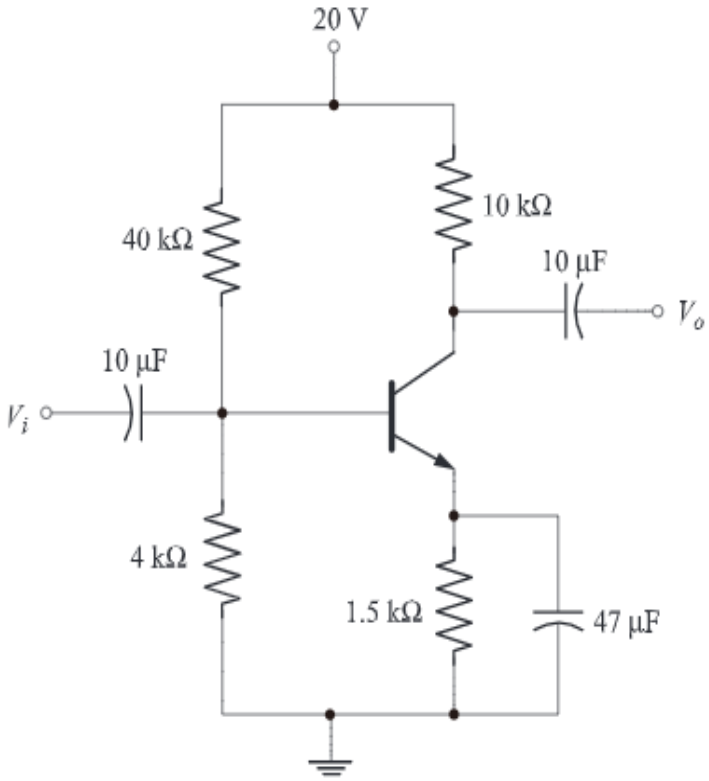


Voltage Divider Bias Configuration: Numericals

b. I_C and V_{CE} using approximate analysis

Given:

V_{CC} = 20V, R_1 = 40kΩ, R_2 = 4k Ω, R_C = 10k Ω,
R_E = 1.5k Ω, C_1 = C_2 = 10μF, C_E = 47μF, V_{BE} = 0.7V



βR_E = 150*1.5k = 225kΩ

$10R_2$ = 10*4k = 40kΩ

Note that $\beta R_E > 10R_2$, hence we can use approximate analysis.

$$V_B = \frac{V_{CC}R_2}{R_1+R_2} = 1.82\ V$$ (Same as V_{Th})

$V_E = V_B - V_{BE}$ = 1.82 – 0.7 = 1.12 V

$$I_E = \frac{V_E}{R_E} = \frac{1.12}{1.5k} = 0.746\ mA$$

Voltage Divider Bias Configuration: Numericals

Given:

V_{CC} = 20V, R_1 = 40kΩ, R_2 = 4k Ω, R_C = 10k Ω,
R_E = 1.5k Ω, C_1 = C_2 = 10μF, C_E = 47μF, V_{BE} = 0.7V

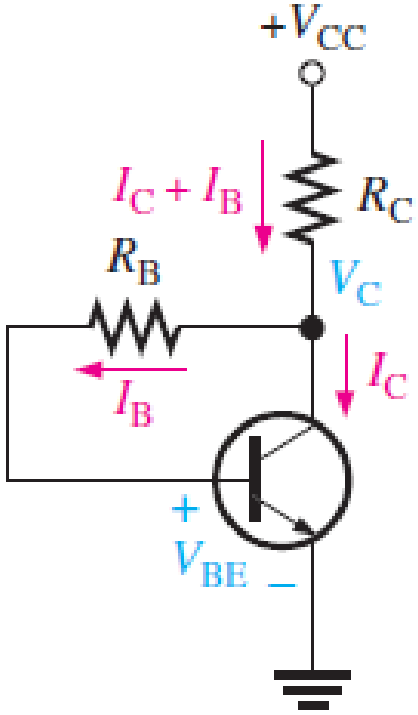
$$I_C \approx I_E$$

$$V_{CE} = V_{CC} - I_C (R_C + R_E) = 20 - 0.746m\ (10k + 1.5k) = 11.42V$$

$$I_{C(sat)} = \frac{V_{CC}}{R_C + R_E} = \frac{20}{10k + 1.5k} = 1.74mA$$

Parameter	*Exact analysis*	*Approximate analysis*
I_C	0.729 mA	0.746 mA
V_{CE}	11.62 V	11.42 V

Collector to Base Bias configuration



It is an improvement over fixed bias method.

In this, biasing resistor is connected between collector and base of the transistor to provide feedback path.

The base resistor RB is connected to the collector rather than to VCC, as it was in the base bias arrangement discussed earlier. The collector voltage provides the bias for the base-emitter junction. The negative feedback creates an "offsetting" effect that tends to keep the Q-point stable. If IC tries to increase, it drops more voltage across RC, thereby causing VC to decrease. When VC decreases, there is a decrease in voltage across RB, which decreases IB. The decrease in IB produces less IC which, in turn, drops less voltage across RC and thus offsets the decrease in VC.

Apply KVL to the base circuit we get;

$$V_{CC} - (I_C + I_B) R_C - I_B R_B - V_{BE} = 0$$

$$V_{CC} = (I_C + I_B) R_C + I_B R_B + V_{BE}$$

$$V_{CC} = (R_B + R_C) I_B + \beta I_B R_C + V_{BE}$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (1+\beta)R_C}$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + \beta R_C}$$

Apply KVL to the Collector circuit we get;

$$V_{CC} - (I_C + I_B) R_C - V_{CE} = 0$$

$$V_{CC} = (I_C + I_B) R_C + V_{CE}$$

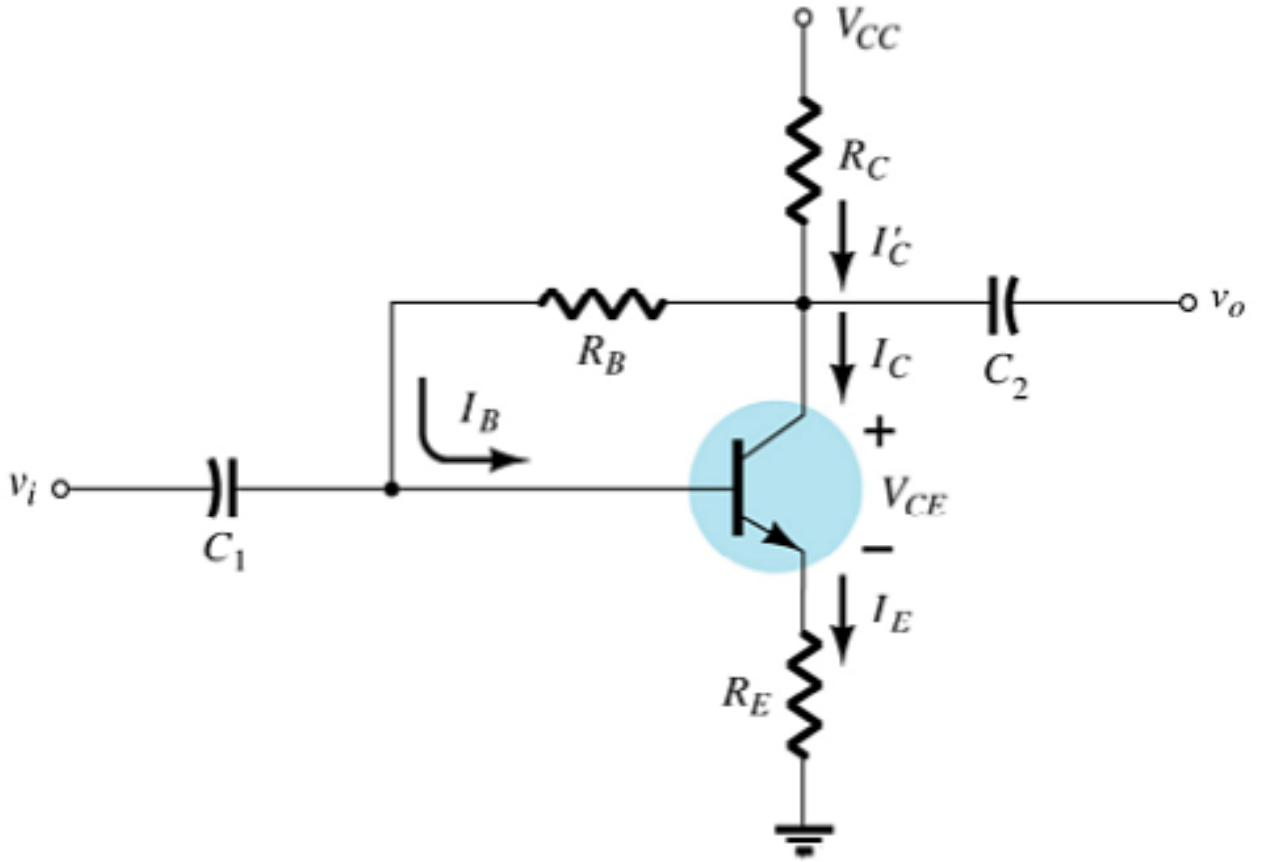
$$V_{CE} = V_{CC} - (I_C + I_B) R_C$$

$I_C = \beta I_B$ **Where** β_{DC} **= dc current gain and** $I_E = I_C + I_B$

Modified DC Bias with voltage feedback

Another way to improve the stability of a bias circuit is to add a feedback path from collector to base.

In this bias circuit the Q-point is only slightly dependent on the transistor beta, β.



Modified DC Bias with voltage feedback

Base-Emitter Loop

From Kirchhoff's voltage law:

$$-V_{CC} + I'_C R_C + I_B R_B + V_{BE} + I_E R_E = 0$$

Where $I_B \ll I_C$:

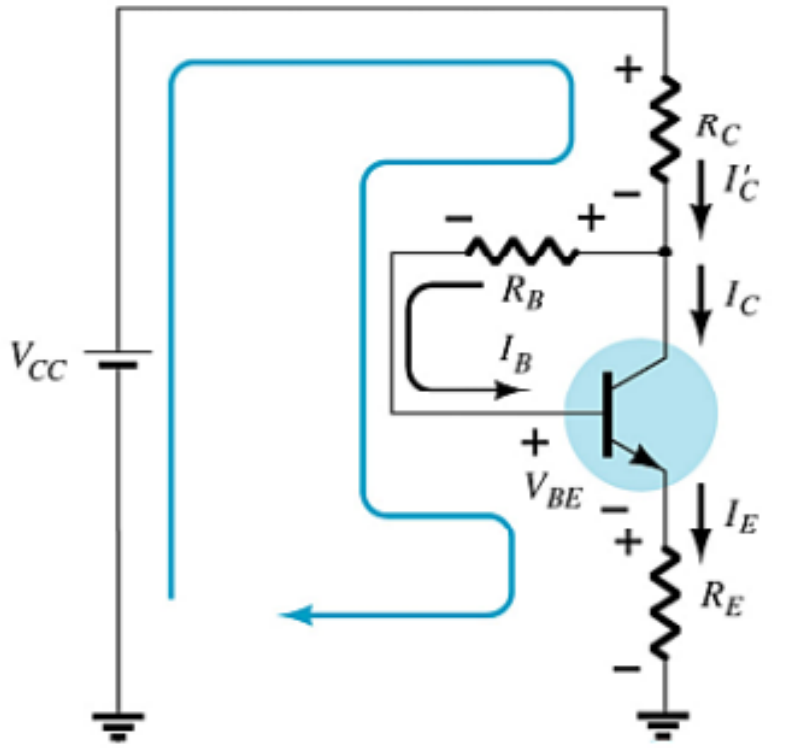
$$I'_C = I_C + I_B \cong I_C$$

Knowing $I_C = \beta I_B$ and $I_E \cong I_C$, the loop equation becomes:

$$V_{CC} - \beta I_B R_C - I_B R_B - V_{BE} - \beta I_B R_E = 0$$

Solving for I_B:

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + \beta(R_C + R_E)}$$



Modified DC Bias with voltage feedback

Collector-Emitter Loop

Applying Kirchoff's voltage law:

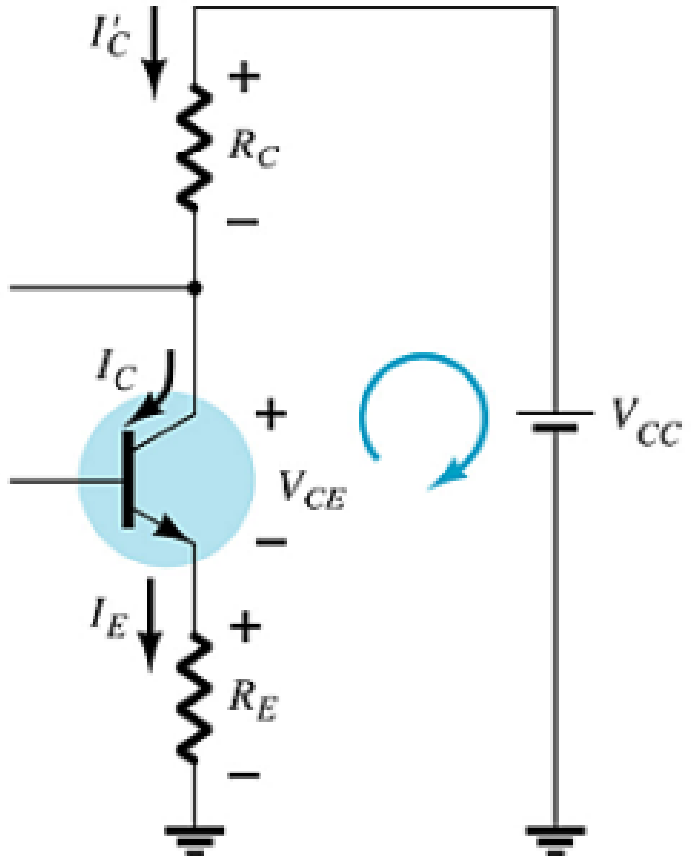
$$I_E + V_{CE} + I'_C R_C - V_{CC} = 0$$

Since $I'_C \cong I_C$ and $I_C = \beta I_B$:

$$I_C(R_C + R_E) + V_{CE} - V_{CC} = 0$$

Solving for V_{CE}:

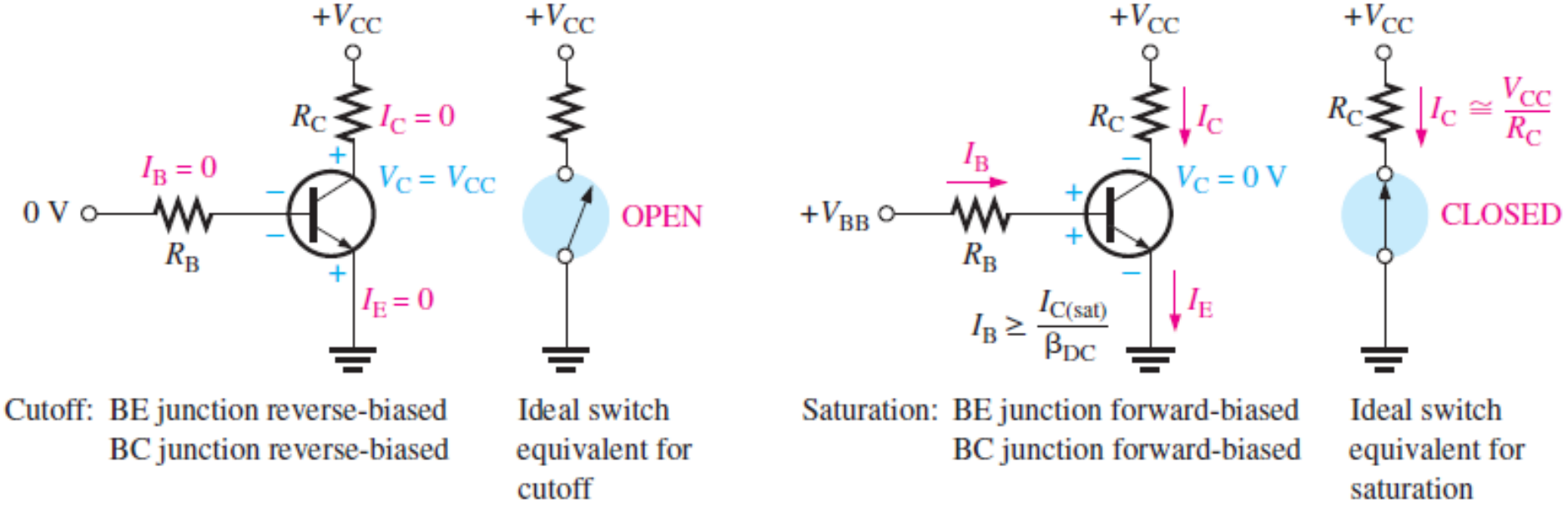
$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$



Transistor Switching Applications

- To operate as switch, the transistor should operate in Cut-off region and Saturation region.
- In cut-off region reverse current flows and is very small hence neglected.
- No current flows through transistor in Cut-off region. The transistor acts as open switch.

Operating Regions	Emitter-Base Junction	Collector-Base Junction	Function
Cut-off region	Reverse Biased	Reverse Biased	OFF Switch
Saturation region	Forward Biased	Forward Biased	ON Switch



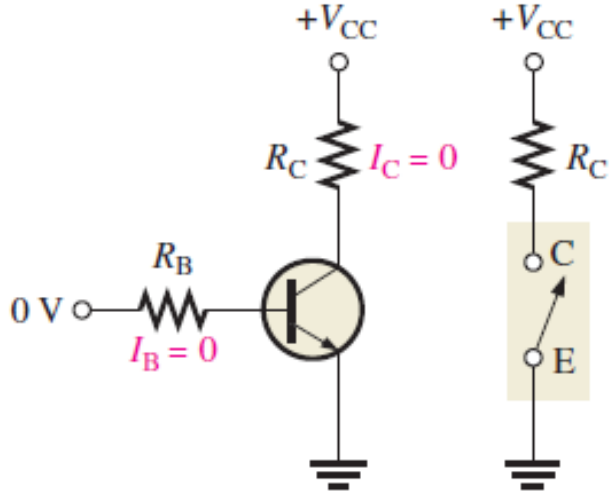
Cutoff — open switch

Saturation — closed switch

Transistor Switching Applications

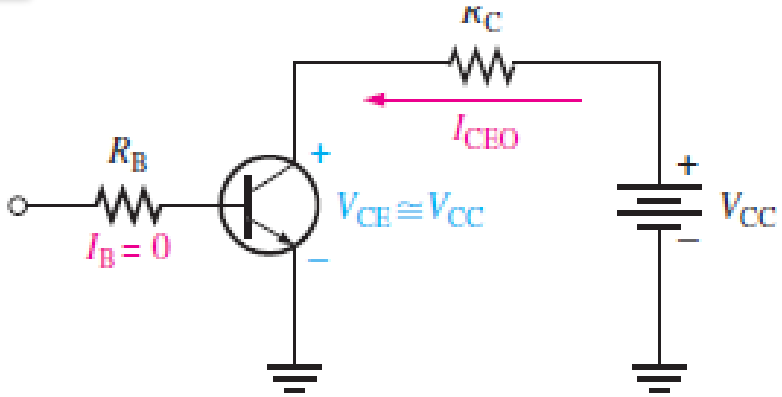
Conditions in Cut-off Region

- To operate as switch, the transistor should operate in **Cut-off region and Saturation region.**
- In cut-off region **reverse current flows** and is **very small** hence neglected.
- No current flows through transistor in Cut-off region. The transistor acts as **open switch.**



(a) Cutoff — open switch

Operating Regions	Emitter-Base Junction	Collector-Base Junction	Function
Cut-off region	Reverse Biased	Reverse Biased	OFF Switch
Saturation region	Forward Biased	Forward Biased	ON Switch

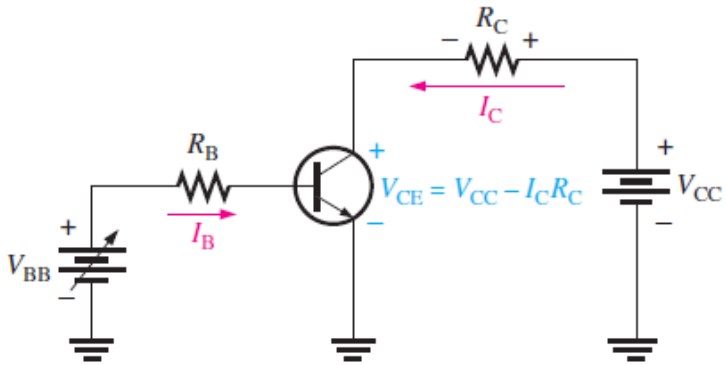


Collector leakage current (I_{CEO}) is extremely small and is usually neglected. so that $V_{CE(cutoff)} = V_{CC}$

Transistor Switching Networks

- **In saturation region the collector current is very large and controlled by external resistance in collector circuit.**
- **V_{CE} is zero in the saturation region. The transistor acts as closed switch.**

Operating Regions	Emitter-Base Junction	Collector-Base Junction	Function
Saturation region	**Forward Biased**	**Forward Biased**	**ON Switch**



- When the base-emitter junction becomes forward-biased and the base current is increased, the collector current also increases ($I_C = \beta I_B$) and V_{CE} decreases as a result of more drop across the collector resistor **($V_{CE} = V_{CC} - I_C R_C$).**

$$I_{C(sat)} = \frac{V_{CC} - V_{CE(sat)}}{R_C}$$

Since VCE(sat) is very small compared to VCC, it can usually be neglected.
The minimum value of base current needed to produce saturation is

$$I_{B(min)} = \frac{I_{C(sat)}}{\beta_{DC}}$$

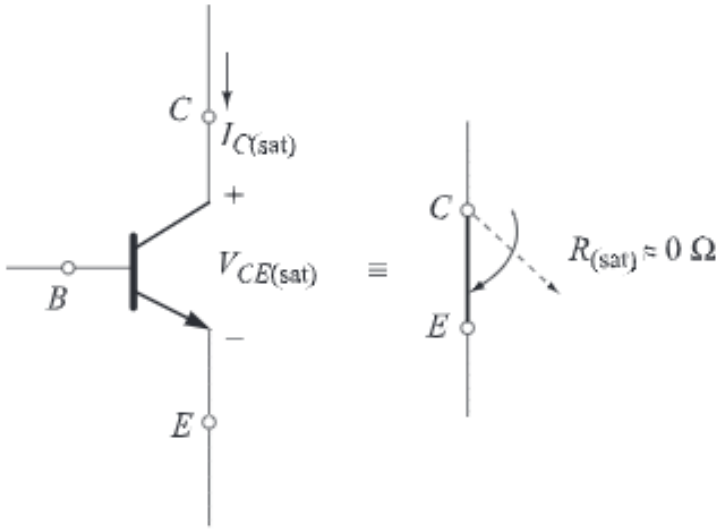
- When V_{CE} reaches its saturation value, **$V_{CE(sat)}$**, the base-collector junction becomes forward-biased and I_C can increase no further even with a continued increase in I_B. At the point of Transistor saturation, the relation **$I_C = \beta I_B$** is no longer valid,

- $V_{CE(sat)}$ for a transistor occurs somewhere below the knee of the collector curves, and it is usually only a few tenths of a volt

Transistor Switching Networks

- In saturation region the collector current is very large and controlled by external resistance in collector circuit.
- V_{CE} is zero in the saturation region. The transistor acts as closed switch.

Operating Regions	Emitter-Base Junction	Collector-Base Junction	Function
Saturation region	Forward Biased	Forward Biased	ON Switch



Transistor Switching Characteristics

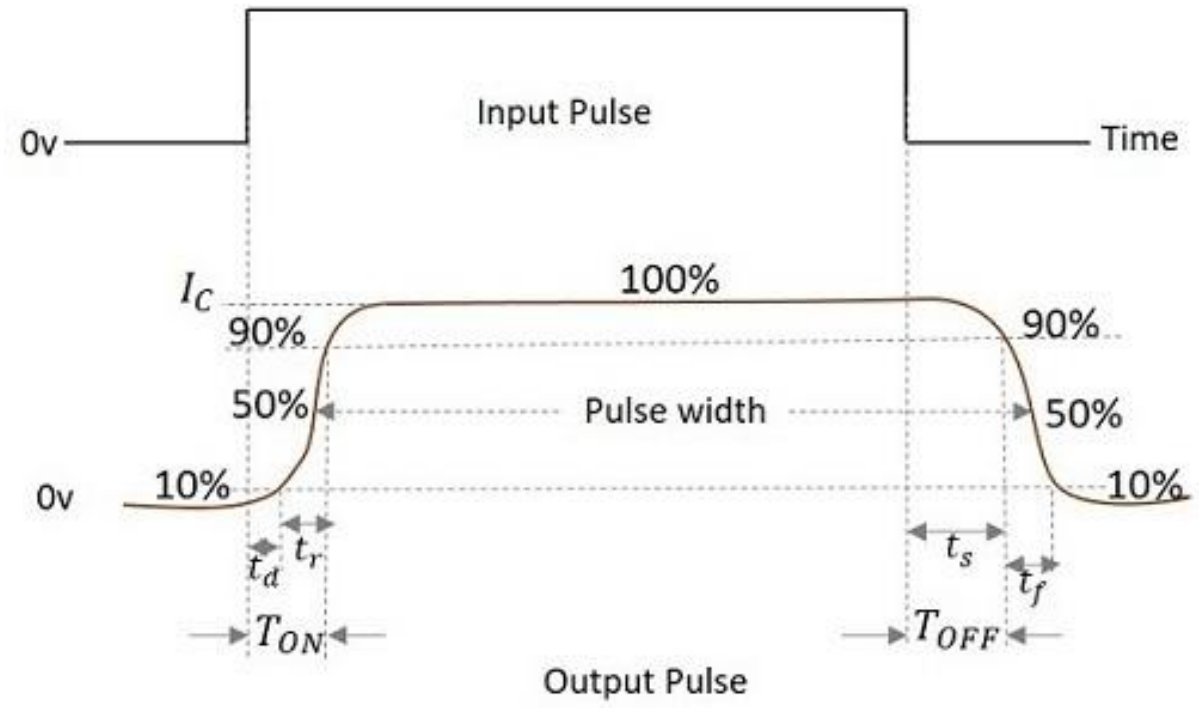
The time between the application of input pulse and commencement of collector current flow is termed as delay time (T_d).

The time required for collector current to reach 90% of its maximum value from 10% level is called rise time (T_r).

$$T_{ON} = T_d + T_r$$

$$T_{OFF} = T_s + T_f$$

The time required for collector current to reduce from 90% level to 10% level is called fall time (T_f).

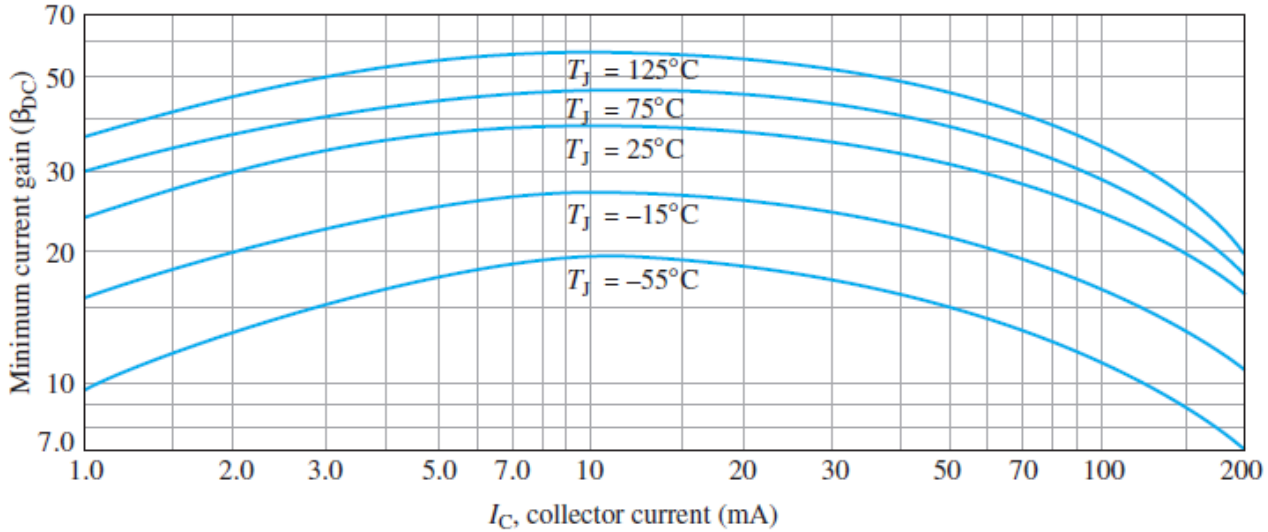


More About β_{DC}, DC Current Gain

The dc current **gain** of a transistor is the ratio of the dc collector current (I_C) to the dc base current (I_B) and is designated dc **beta** (β_{DC}).

$$I_B = \frac{V_{BB} - V_{BE}}{R_B} \quad , I_C = \beta I_B \; , \; I_E = I_C + I_B$$

- β_{DC} is not truly constant but varies with both collector current and with temperature. Keeping the junction temperature constant and increasing I_C causes β_{DC} to increase to a maximum.
- A further increase in I_C beyond this maximum point causes β_{DC} to decrease.
- If I_C is held constant and the temperature is varied, β_{DC} changes directly with the temperature.
- If the temperature goes up, β_{DC} goes up and vice versa. Figure shows the variation of β_{DC} with I_C and junction temperature (T_J) for a typical BJT.



Variation of β_{DC} with I_C for several temperatures

Stability Factors

Stability Factors Indicates degree of change in operating point due to variation in Temperature,

Three Variables which are Temperature Dependent are I_{CO} , β_{DC} V_{BE}

Effects of Temperature on Transistor parameters:

1. **Variation of Reverse Saturation current (Collector leakage current) I_{CO} with temperature (Doubles for 10^0C rise in temperature).**
2. **Variation of DC current gain, β with temperature (Increases with rise in temperature)**
3. **Variation of V_{BE} with temperature (Decreases by 2.5mV for every degree Celsius rise in temperature).**

$$I_C = \beta * I_B + I_{CEO} \quad ; \quad I_B = (V_{CC} - V_{BE})/R_B$$

Three Stability factors are :

$$S(I_{CO}) = \frac{\partial I_C}{\partial I_{CO}} = \frac{\Delta I_C}{\Delta I_{CO}},$$ **β and V_{BE} are constant**

$$S(V_{BE}) = \frac{\partial I_C}{\partial V_{BE}} = \frac{\Delta I_C}{\Delta V_{BE}},$$ **β and I_{CO} are constant**

$$S(\beta) = \frac{\partial I_C}{\partial \beta} = \frac{\Delta I_C}{\partial \beta},$$ **V_{BE} and I_{CO} are constant**

Stability factor (S) is defined as the Variation / rate of change of collector current(Ic) with respect to the reverse saturation current(Ico), keeping β and VBE constant

Stability Factors : General Expression for S(Ico):

Stability factor (S) is defined as the Variation (rate of change of) collector current(Ic) with respect to the reverse saturation current(Ico), keeping β and VBE constant

$$S = \frac{dIc}{dIco} \text{ at constant } \beta \text{ and } V_{BE}. \qquad \text{------(1)}$$

$$Ic = \beta IB + (1+\beta)Ico \qquad \text{----(1)}$$

Differentiate this equation with respect to 'Ic', consider β as a constant(see definition of S).

$$\frac{d}{dIc}Ic = \frac{d}{dIc}(\beta IB + (1+\beta)Ico) \qquad \text{-------(2)}$$

$$1 = \beta\frac{dIB}{dIc} + (1+\beta)\frac{dIco}{dIc}$$

$$1 = \beta\frac{dIB}{dIc} + \frac{(1+\beta)}{S}$$

From this, write equation for Stability factor, S

$$\therefore S = \frac{(1+\beta)}{1-\beta\frac{dIB}{dIc}} \qquad \text{----(3)}$$

Stability Factors

General Expression for $S(I_{CO})$:

$$I_C = I_{CEO} + \beta * I_B$$

$$I_C = (1+\beta) I_{CO} + \beta * I_B$$

$$S(I_{CO}) = \frac{\partial I_C}{\partial I_{CO}} = \frac{\Delta I_C}{\Delta I_{CO}}$$

$$1 = (1+\beta)\frac{\partial I_{CO}}{\partial I_C} + \beta \frac{\partial I_B}{\partial I_C}$$

$$(1+\beta)\frac{\partial I_{CO}}{\partial I_C} = 1 - \beta \frac{\partial I_B}{\partial I_C}$$

$$S(I_{CO}) = \frac{\partial I_C}{\partial I_{CO}} = \frac{(1+\beta)}{1 - \beta \frac{\partial I_B}{\partial I_C}}$$

$$1 - \beta \frac{\partial I_B}{\partial I_C} \gg 1 + \beta$$

$$\frac{\partial I_B}{\partial I_C} \ll -1 \Rightarrow \left| \frac{\partial I_B}{\partial I_C} \right| \gg 1$$

Stability Factors: Fixed Bias Configuration

Stability factor: $S(I_{CO})$:

$$S(I_{CO}) = \frac{\partial I_C}{\partial I_{CO}} = \frac{(1+\beta)}{1-\beta\frac{\partial I_B}{\partial I_C}}$$

$$S(I_{CO}) = \frac{\partial I_C}{\partial I_{CO}} = \frac{\Delta I_C}{\Delta I_{CO}}$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

$$I_B \approx \frac{V_{CC}}{R_B}$$

$$\frac{\partial I_B}{\partial I_C} = 0$$

$$S(I_{CO}) = (1+\beta)$$

Stability factor: $S(V_{BE})$:

$$S(V_{BE}) = \frac{\partial I_C}{\partial V_{BE}} = \frac{\Delta I_C}{\Delta V_{BE}}$$, β and ICO are constant

$$V_{CC} = I_B R_B + V_{BE}$$

$$V_{BE} = V_{CC} - I_B R_B$$

$$V_{BE} = V_{CC} - (I_C/\beta) R_B$$

Differentiating w.r.t. V_{BE}, keeping β constant

$$1 = 0 - \frac{R_B}{\beta}\frac{\partial I_C}{\partial V_{BE}}$$

$$S(V_{BE}) = \left(-\frac{\beta}{R_B}\right)$$

Stability Factors: Fixed Bias Configuration

Stability factor: S(β):

$$S(\beta) = \frac{\partial I_C}{\partial \beta} = \frac{\Delta I_C}{\partial \beta}$$, V_{BE} and ICO are constant

$$I_C = \frac{\beta}{R_B}[V_{CC} - VBE]$$

Let $I_C = I_{C1}$, $\beta = \beta_1$, at Temperature T_1

$I_C = I_{C2}$, $\beta = \beta_2$, at Temperature T_2

$$I_{C1} = \frac{\beta_1}{R_B}[V_{CC} - VBE]$$

$$I_{C2} = \frac{\beta_2}{R_B}[V_{CC} - VBE]$$

$$\frac{I_{C_2}}{I_{C_1}} - 1 = \frac{\beta_2}{\beta_1} - 1$$

$$\frac{I_{C_2} - I_{C_1}}{I_{C_1}} = \frac{\beta_2 - \beta_1}{\beta_1}$$

$$\frac{\Delta I_C}{I_{C_1}} = \frac{\Delta \beta}{\beta_1}$$

$$S(\beta) = \frac{\Delta I_C}{\Delta \beta} = \frac{I_{C_1}}{\beta_1}$$

Stability Factors: Emitter Stabilized Bias Configuration

Stability factor: $S(I_{CO})$:

$$S(I_{CO}) = \frac{\partial I_C}{\partial I_{CO}} = \frac{(1+\beta)}{1-\beta\frac{\partial I_B}{\partial I_C}}$$

$$S(I_{CO}) \approx 1 + \frac{R_B}{R_E}$$

Stability factor: $S(V_{BE})$:

$$S(V_{BE}) = \frac{\partial I_C}{\partial V_{BE}} = \frac{\Delta I_C}{\Delta V_{BE}}$$, β and ICO are constant

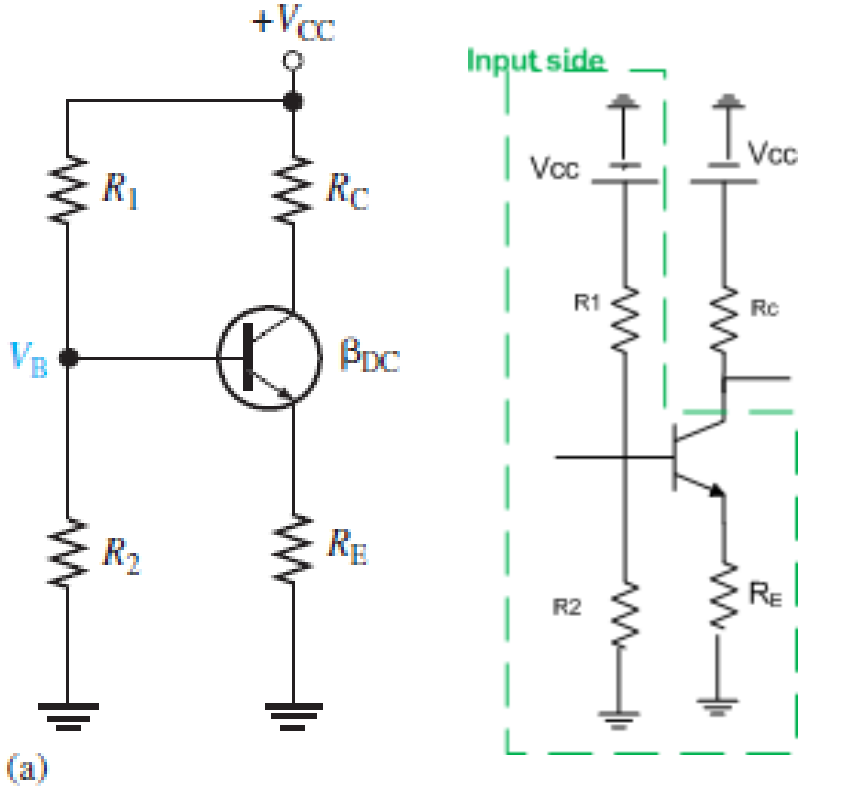
$$S(V_{BE}) = \frac{\partial I_C}{\partial V_{BE}} = \frac{-\beta}{R_B + (1+\beta)R_E}$$

Stability factor: S(β):

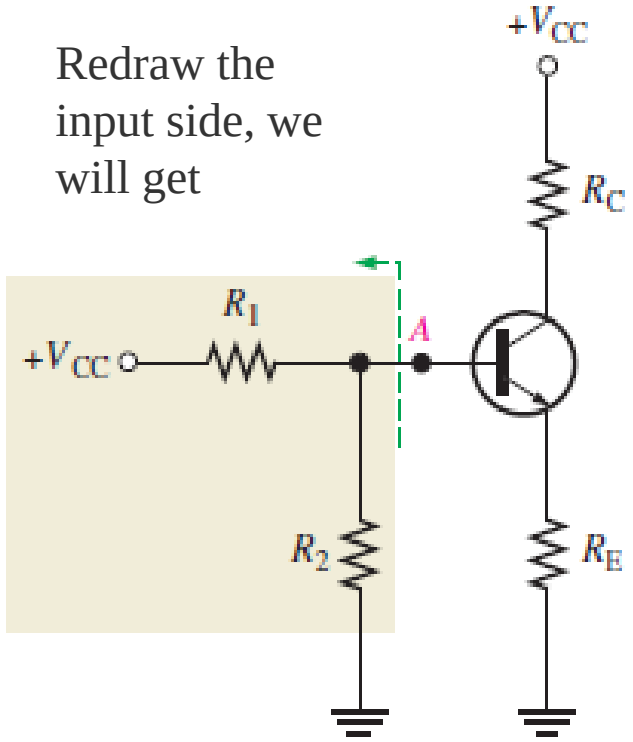
$$S(\beta) = \frac{\partial I_C}{\partial \beta} = \frac{\Delta I_C}{\partial \beta}$$, V_{BE} and ICO are constant

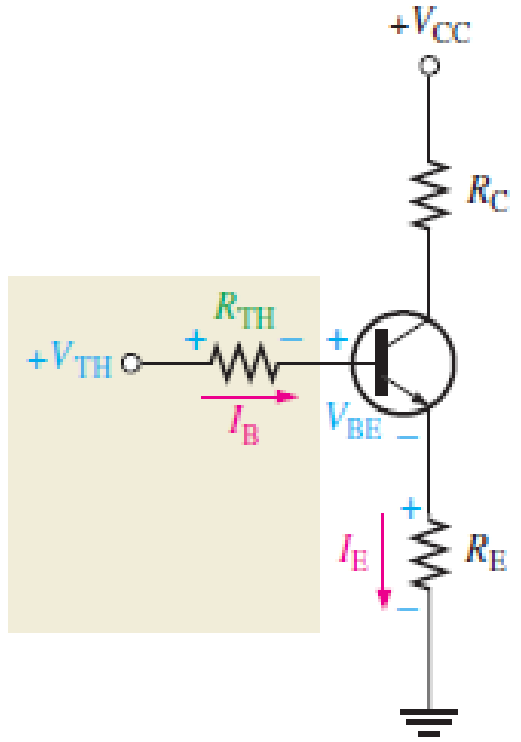
$$S(\beta) = \frac{\Delta I_C}{\Delta \beta} = \frac{I_{C_1}\left(1+\frac{R_B}{R_E}\right)}{\beta_1\left(1+\beta_2+\frac{R_B}{R_E}\right)}$$

Stability Factors: Voltage Divider Bias Configuration



Redraw the input side, we will get





The voltage at point *A* with respect to ground is

$$V_{TH} = \left(\frac{R_2}{R_1 + R_2}\right) V_{CC}$$

$$R_{TH} = \frac{R_1 R_2}{R_1 + R_2}$$

Applying Kirchhoff's voltage law around the equivalent base-emitter loop gives

$V_{TH} - V_{RTH} - V_{BE} - V_{RE} = 0$

$V_{TH} = I_B R_{TH} + V_{BE} + (I_B + I_c) R_E$ ----(1) Differentiate equation (1) with respect to Ic (take V_{BE} and V_{TH} as a constants).

Stability Factors: Voltage Divider Bias Configuration

$$S(I_{CO}) = \frac{\partial I_C}{\partial I_{CO}} = \frac{(1+\beta)}{1-\beta\frac{\partial I_B}{\partial I_C}}$$

$V_{TH} = I_B R_{TH} + V_{BE} + (I_B + I_c)R_E$ ----(1)

Differentiate equation (1) with respect to Ic (take V_{BE} and V_{TH} as a constants).

$$0 = \frac{dI_B}{dI_c}R_{TH} + \frac{dI_B}{dI_c}R_E + R_E$$ re-arranging we will get,

$$\frac{dI_B}{dI_c} = \frac{-R_E}{R_{TH}+R_E}$$ --------(2) Put this in equ for 'S'.

$$S = \frac{1+\beta}{1+\beta\frac{R_E}{R_{TH}+R_E}}$$ -------(3) take denominator and re-arrange as

$$S = \frac{1+\beta}{1+\beta\frac{1}{((R_{TH}/R_E)+1)}}$$ ------- multiply denominator and numerator by $(R_{TH} / R_E) + 1$

$$S = \frac{[1+\beta][(R_{TH}/R_E)+1]}{(R_{TH}/R_E)+1+\beta}$$ ---------- (4)

Stability Factors: Voltage Divider Bias Configuration

Stability factor: $S(V_{BE})$:

$$S(V_{BE}) = \frac{\partial I_C}{\partial V_{BE}} = \frac{\Delta I_C}{\Delta V_{BE}}$$, β and ICO are constant

$I_C = (1+\beta)I_{CO} + \beta * I_B$ ----(1)

By writing Equation (1) in terms of I_B, We get

$$I_B = \frac{I_C - (1+\beta)Ico}{\beta}$$

$V_{TH} = I_B R_{TH} + V_{BE} + (I_B + I_c)R_E$ ----(2)

$V_{BE} = V_{TH} - (R_E + R_B)I_B - R_E I_C$ ----(3)

Now Substituting I_B in Equation (3), We get

$$V_{BE} = V_{TH} - (R_E + R_B)\left[\frac{I_C - (1+\beta)Ico}{\beta}\right] - R_E I_C \quad \text{----(3)}$$

$$S(V_{BE}) = \frac{\partial I_C}{\partial V_{BE}} = \frac{-\beta}{R_{Th} + (\beta+1)R_E}$$

Differentiate equation (3) with respect to V_{BE} (take I_{CO} and β as a constants).

Stability Factors: Voltage Divider Bias Configuration

Stability factor: $S(I_{CO})$:

$$S(I_{CO}) = \frac{\partial I_C}{\partial I_{CO}} = \frac{(1+\beta)}{1-\beta\frac{\partial I_B}{\partial I_C}}$$

$$S(I_{CO}) = (\beta+1)\frac{\left[1+\frac{R_{Th}}{R_E}\right]}{(\beta+1)+\frac{R_{Th}}{R_E}}$$

Stability factor: $S(V_{BE})$:

$$S(V_{BE}) = \frac{\partial I_C}{\partial V_{BE}} = \frac{\Delta I_C}{\Delta V_{BE}}$$, β and ICO are constant

$$S(V_{BE}) = \frac{\partial I_C}{\partial V_{BE}} = \frac{-\beta}{R_{Th}+(\beta+1)R_E}$$

Stability factor: S(β):

$$S(\beta) = \frac{\partial I_C}{\partial \beta} = \frac{\Delta I_C}{\partial \beta}$$, V_{BE} and ICO are constant

$$S(\beta) = \frac{I_{C_1}\left[1+\frac{R_{Th}}{R_E}\right]}{\beta_1\left[1+\beta_2+\frac{R_{Th}}{R_E}\right]}$$

Stability Factors: Voltage Divider Bias Configuration

For the voltage divider bias circuit, find I_C, V_B, V_E, R_1 and $S(I_{CO})$.
$R_2 = 5.6k\Omega$, $R_C = 4.7k\ \Omega$, $R_E = 1.2k\ \Omega$, $V_{CC} = 18V$, $V_C = 12V$, $V_{BE} = 0.7V$ and $\beta = 100$

a. Collector current, I_C

$$V_C = V_{CC} - I_C R_C$$

$$I_C = \frac{V_{CC} - V_C}{R_C}$$

$$I_C = \frac{18 - 12}{4.7k} = 1.276mA$$

b. Base Voltage, V_B

$$V_B = V_{BE} + I_E R_E = V_{BE} + (I_C + I_B)R_E = V_{BE} + (I_C + I_C/\beta)R_E$$

$$V_B = 0.7 + \left(1.267m + \frac{1.267m}{100}\right)1.2k = 2.246\text{V}$$

Stability Factors: Voltage Divider Bias Configuration

For the voltage divider bias circuit, find I_C, V_B, V_E, R_1 and $S(I_{CO})$.
$R_2 = 5.6k\Omega$, $R_C = 4.7k\ \Omega$, $R_E = 1.2k\ \Omega$, $V_{CC} = 18V$, $V_C = 12V$, $V_{BE} = 0.7V$ and $\beta = 100$

c. V_E

$$V_E = V_B - V_{BE}$$

$$V_E = 2.246 - 0.7 = 1.546V$$

d. R_1

$$V_B = \frac{V_{CC}\,R_2}{R_1 + R_2}$$

$$R_1 = \frac{V_{CC}\,R_2}{V_B} - R_2$$

$$R_1 = \frac{18 * 5.6k}{2.246} - 5.6k = 39.28k\Omega$$

e. $S(I_{CO})$

$$R_B = R_1 \,\|\, R_2 = 39.28k \,\|\, 5.6k = 4.9k\Omega$$

$$S(ICO) = \frac{(1+\beta)}{1 + \frac{\beta R_E}{R_E + RB}}$$

$$S(ICO) = \frac{(1+100)}{1 + \frac{100 * 1.2k}{1.2k + 4.9k}} = 4.885$$

THANK YOU