ATME COLLEGE OF ENGINEERING

13th KM Stone, Bannur Road, Mysore - 570 028

DEPARTMENT OF ELECTRICAL & ELECTRONICS ENGINEERING

NOTES

Course Title : Digital Logic Circuits

Course CODE: BEE306A

SEMESTER: III

Academic Year - 2023-24

INSTITUTIONAL VISION AND MISSION

VISION:

- Development of academically excellent, culturally vibrant, socially responsible and globally competent human resources.

MISSION:

- To keep pace with advancements in knowledge and make the students competitive and capable at the global level.
- To create an environment for the students to acquire the right physical, intellectual, emotional and moral foundations and shine as torchbearers of tomorrow's society.
- To strive to attain ever-higher benchmarks of educational excellence.

Department Vision and Mission

Vision:

To create Electrical & Electronics Engineers who excel to be technically competent and fulfill the cultural and social aspirations of the society.

Mission:

- To provide knowledge to students that builds a strong foundation in the basic principles of electrical engineering, problem solving abilities, analytical skills, soft skills and communication skills for their overall development.
- To offer outcome based technical education.
- To encourage faculty in training & development and to offer consultancy through research & industry interaction.

Program Educational Objectives (PEOs)

PEO1:

To produce competent and ethical Electrical and Electronics Engineers who will exhibit the necessary technical and managerial skills to perform their duties in society

PEO2:

To make students continuously acquire and enhance their technical and socio-economic skills

PEO3:

To allow students to embark on R&D activities leading to offering solutions and excel in various career paths.

PEO4:

To produce quality engineers who have the capability to work in teams and contribute to real time projects

Program Outcomes (POs)

Engineering Graduates will be able to:

PO1: Engineering Knowledge: Apply the knowledge of mathematics, science, engineering fundamentals and an engineering specialization to the solution of complex engineering problems.

PO2: Problem Analysis: Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.

PO3: Design / Development of solutions: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.

PO4: Conduct investigations of complex problems: Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.

PO5: Modern tool usage: Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.

PO6: The engineer and society: Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.

PO7: Environment and sustainability: Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.

PO8: Ethics: Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.

PO9: Individual and team work: Function effectively as an individual and as a member or leader in diverse teams, and in multidisciplinary settings.

PO10: Communication: Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.

PO11: Project management and finance: Demonstrate knowledge and understanding of the engineering management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.

PO12: Life-long learning: Recognize the need for and have the preparation and ability to engage in independent and lifelong learning in the broadest context of technological change.

Program Specific Outcomes (PSOs)

The students will develop an ability to produce the following engineering traits:

PSO1:Apply the concepts of Electrical & Electronics Engineering to evaluate the performance of power systems and also to control industrial drives using power electronics

PSO2: Demonstrate the concepts of process control for Industrial Automation, design models for environmental and social concerns and also exhibit continuous self- learning

Digital Logic Circuit

			Academic Year: 2024-2025				
Department: Electrical and Electronics Engineering							
Course Code	Course Title	Core/Elective	Prerequisite	Contact Hours			Total Hrs/ Sessions
				L	T	P	
BEE306A	**Digital Logic Circuit**	**Elective**	**Basic Electronics**	**3**	**-**	**2**	**40 theory**

Topics Covered as per Syllabus

Module-1

Definition of combinational logic, canonical forms, Generation of switching equations from truth tables, Karnaugh maps-3,4,5 variables, Incompletely specified functions (Don‘t care terms) Simplifying Max term equations, Quine-McCluskey minimization technique, Quine-McCluskey using don‘t care terms, Reduced prime implicants Tables.

Module-2

General approach to combinational logic design, Decoders, BCD decoders, Encoders, digital multiplexers, Using multiplexers as Boolean function generators, Adders and subtractors, Cascading full adders, Look ahead carry, Binary comparators

Module-3

Basic Bistable elements, Latches, Timing considerations, The master-slave flip-flops (pulsetriggered flip-flops): SR flip-flops, JK flip-flops, Edge triggered flip- flops, Characteristic equations

Module-4

Registers, binary ripple counters, synchronous binary counters, Counters based on shift registers, Design of a synchronous counter, Design of a synchronous mod-n counter using clocked T, JK, D and SR flip-flops.

Module-5

Mealy and Moore models, State machine notation, Synchronous Sequential circuit analysis, Construction of state diagrams, counter design.

Memories: Read only and Read/Write Memories, Programmable ROM, EPROM, Flash memor**y.**

List of Text Books

“Digital Logic Applications and Design” by John M Yarbrough, 2011 edition.
“HDL Programming (VHDL and Verilog)” by Nazeih M. Botros, 1 st Edition
“Digital Principles and Design “, Donald D Givone, Tata McGraw Hill Edition,2002.

List of Reference Books

“Logic Design” by RD Sudhaker Samuel

List of URLs, Text Books, Notes, Multimedia Content, etc: https://www.youtube.com/watch?v=VnZLRrJYa2I

MODULE 4

Registers and Counters

Structure

- Registers,
- Counters-Binary Ripple Counter, Synchronous Binary counters, Counters based on Shift Registers,
- Design of a Synchronous counters, Design of a Synchronous Mod-N counters using clocked JK FlipFlops
- Design of a Synchronous Mod-N counter using clocked D, T, or SR Flip-Flops.
- Outcome
- Future Readings

Objevtive

- Data storage elements
- Designing of flip flops
- Design of synchronous Mod N for all the flip flops

Registers

- Register is a group of Flip-Flops.
- It stores binary information 0 or 1.
- It is capable of moving data left or right with clock pulse.
- Registers are classified as
    - Serial-in Serial-Out
    - Serial-in parallel Out
    - Parallel-in Serial-Out

- Parallel-in parallel Out

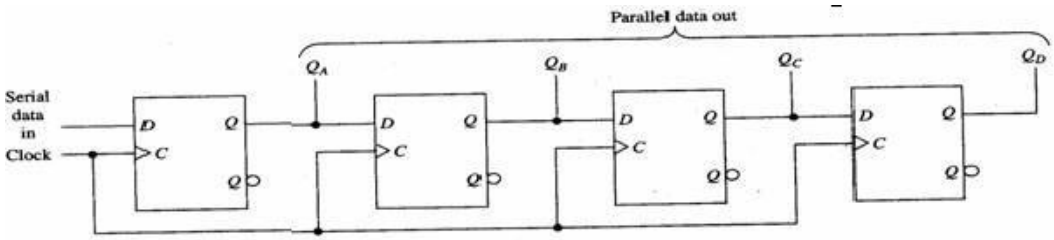


Fig. : Serial-In, Parallel-Out Unidirectional Shift Register

Parallel-in Unidirectional Shift Register

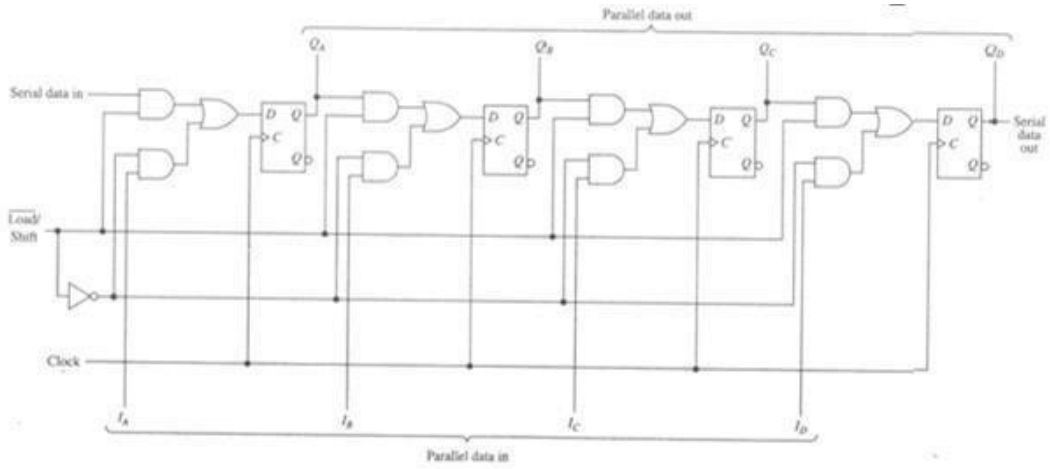
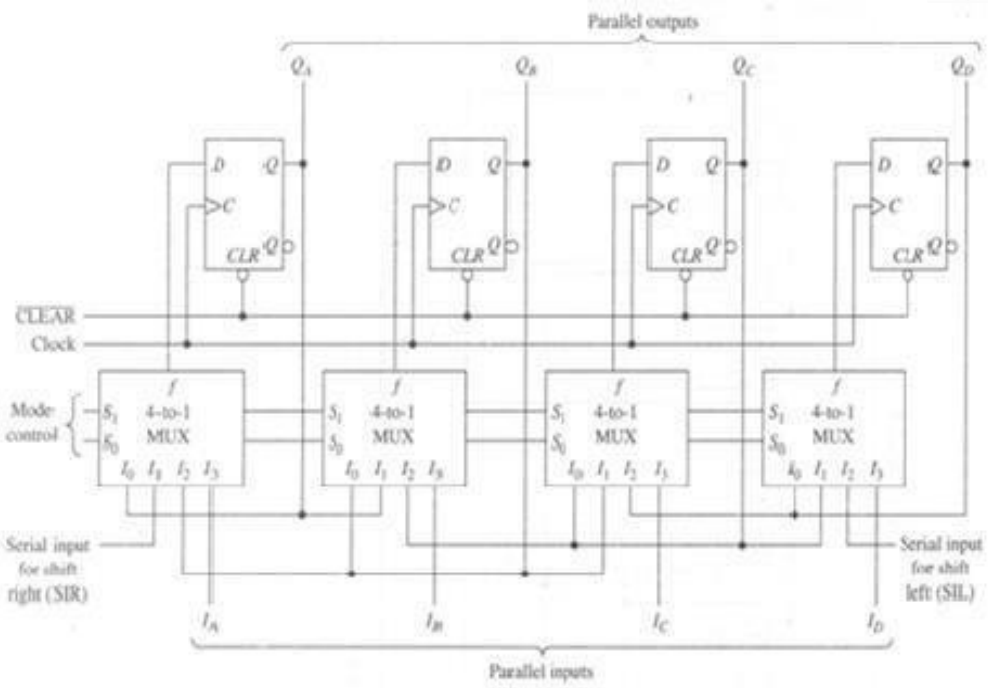


Fig. : Parallel-in Unidirectional Shift Register

- Parallel input data is applied at $I_A I_B I_C I_D$.
- Parallel output $Q_A Q_B Q_C Q_D$.
- Serial input data is applied to A FF.
- Serial output data is at output of D FF.
- $\bar{L}$/Shift is common control input.
- $\bar{L}$/S = 0, Loads parallel data into register.
- $\bar{L}$/S = 1, shifts the data in one direction.

Universal Shift Register



Select lines S_1	S_0	Register operation
0	0	Hold
0	1	Shift right
1	0	Shift left
1	1	Parallel load

- Bidirectional Shifting.
- Parallel Input Loading.
- Serial-Input and Serial-Output.
- Parallel-Input and Serial-Output.
- Common Reset Input.
- 4:1 Multiplexer is used to select register operation.

Counters-Binary Ripple Counter, Synchronous Binary counters, Counters based on Shift Registers

- Counter is a register which counts the sequence in binary form.
- The state of counter changes with application of clock pulse.
- The counter is binary or non-binary.
- The total no. of states in counter is called as modulus.
- If counter is modulus-n, then it has n different states.
- State diagram of counter is a pictorial representation of counter states directed by arrows in graph.

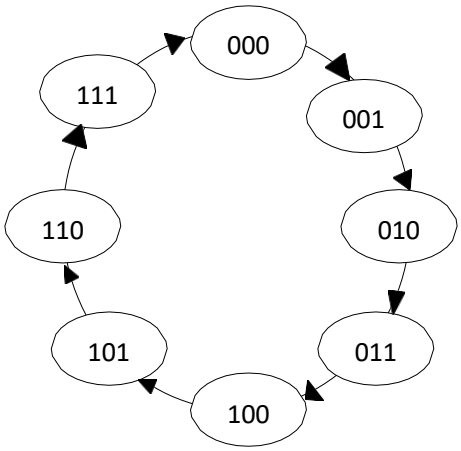
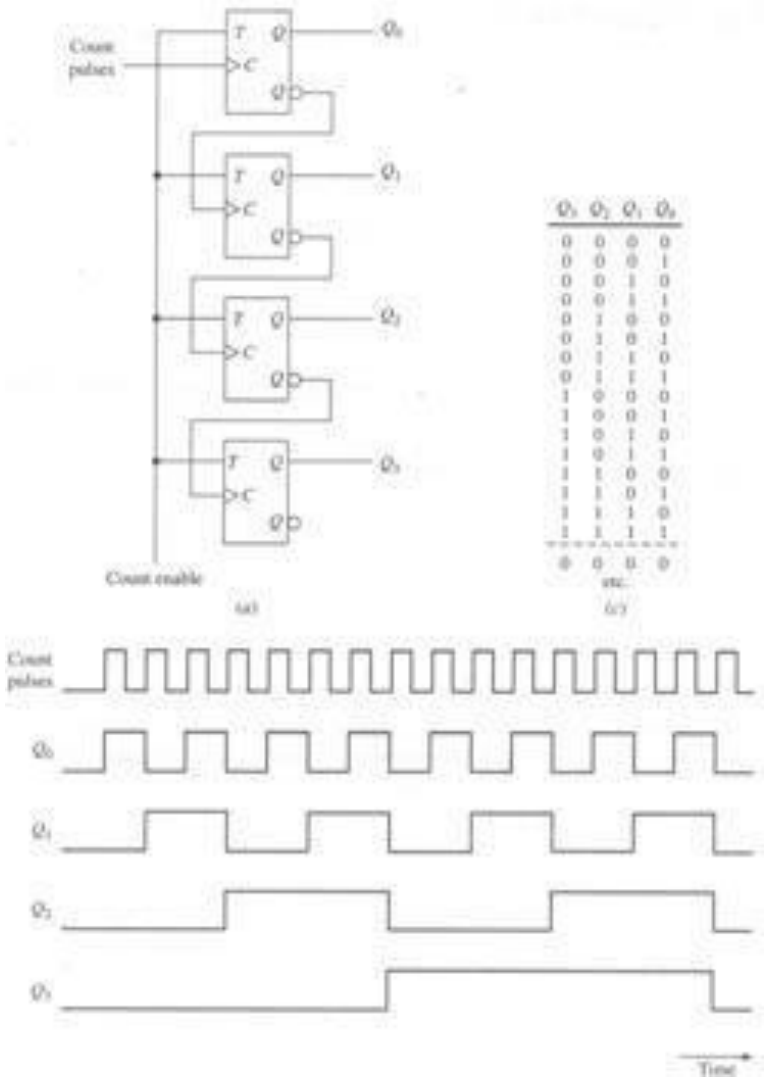


Fig. State diagram of mod-8 counter

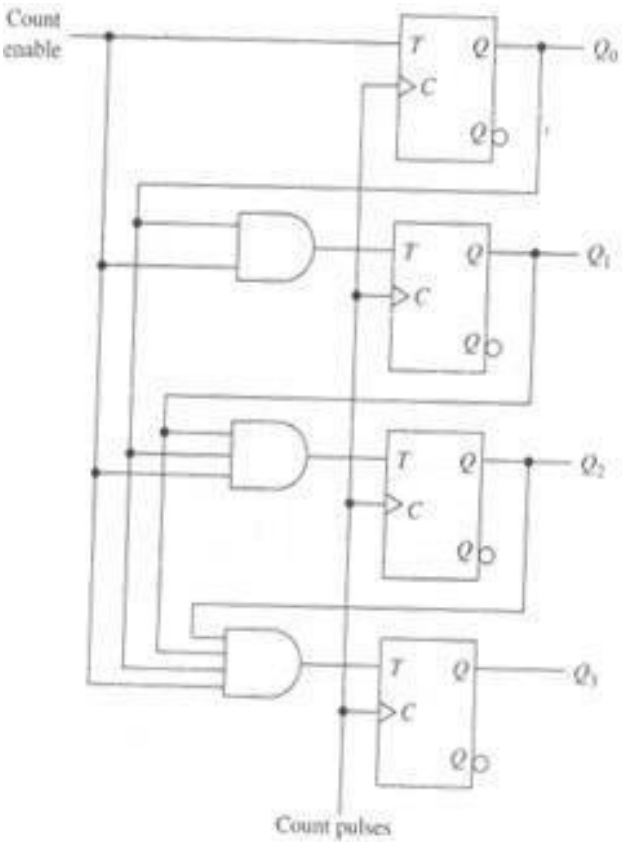
4-bit Binary Ripple Counter :

- All Flip-Flops are in toggle mode.
- The clock input is applied.
- Count enable = 1.
- Counter counts from 0000 to 1111.

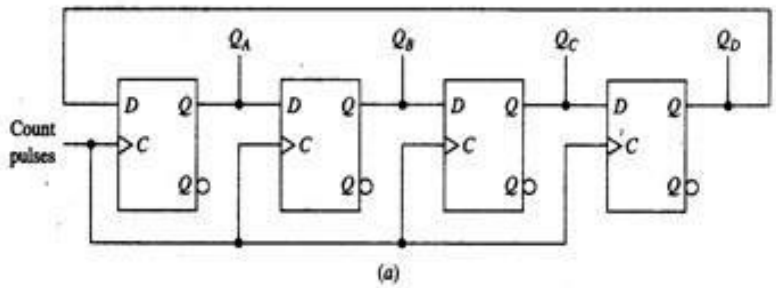


Synchronous Binary Counter :

- The clock input is common to all Flip-Flops.
- The T input is function of the output of previous flip-flop.
- Extra combination circuit is required for flip-flop input.



Counters Based on Shift Register

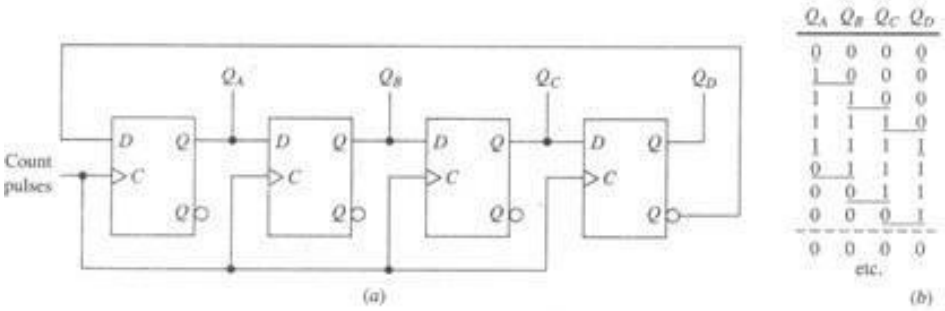


Mod-4 Ring Counter

- The output of LSB FF is connected as D input to MSB FF.
- This is commonly called as Ring Counter or Circular Counter.
- The data is shifted to right with each clock pulse.
- This counter has four different states.

- This can be extended to any no. of bits.

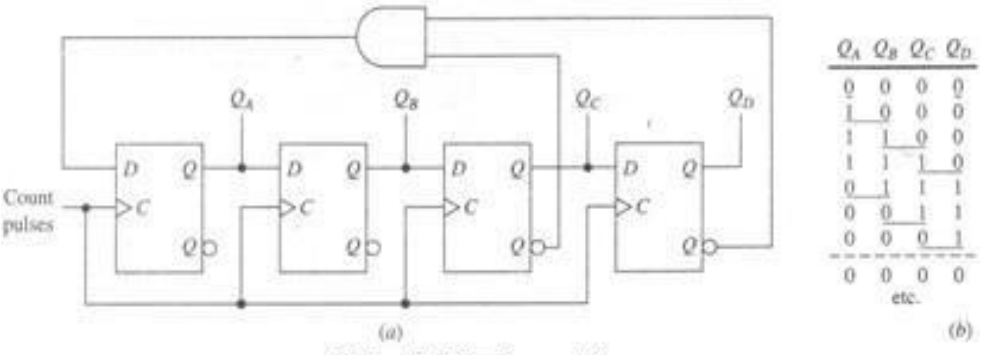
Twisted Ring Counter or Johnson Counter



Mod-8 Johnson Counter

- The complement output of LSB FF is connected as D input to MSB FF.
- This is commonly called as Johnson Counter.
- The data is shifted to right with each clock pulse.
- This counter has eight different states.
- This can be extended to any no. of bits.

Mod-7 Twisted Ring Counter



Mod-7 Ring Counter

- The D input to MSB FF is $\overline{Q_D}.\overline{Q_C}$
- The counter follows seven different states with application of clock input.
- By changing feedback different counters can be obtained.

Design of a Synchronous counters, Design of a Synchronous Mod-N counters using clocked JK Flip Flops

The clock input is common to all Flip-Flops.

Any Flip-Flop can be used.

For mod-n counter 0 to n-1 are counter states.

The excitation table is written considering the present state and next state of counter.

The flip-flop inputs are obtained from characteristic equation.

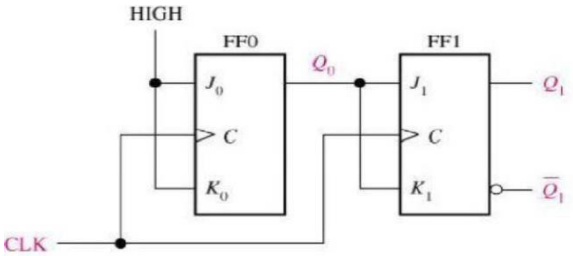
By using flip-flops and logic gate the implementation of synchronous counter is obtained.

Difference between Asynchronous and Synchronous Counter :

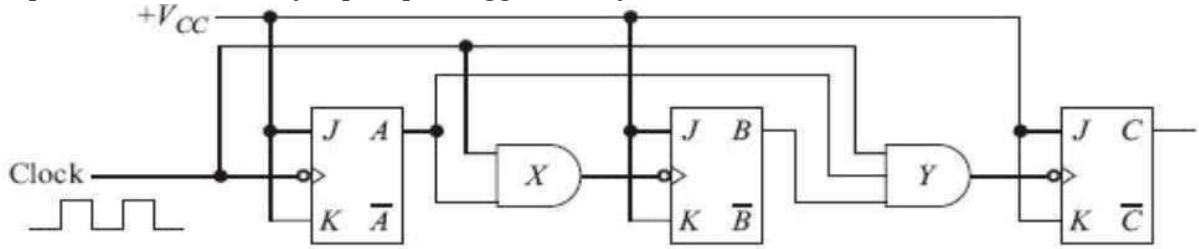
Asynchronous Counter	Synchronous Counter
1. Clock input is applied to LSB FF. The output of first FF is connected as clock to next FF.	1. Clock input is common to all FF.
2. All Flip-Flops are toggle FF.	2. Any FF can be used.
3. Speed depends on no. of FF used for n bit . $f_{max} = \frac{1}{n \times t_p}$	3. Speed is indepenSdent of no. of FF used. $f_{max} = \frac{1}{t_p}$
4. No extra Logic Gates are required.	4. Logic Gates are required based on design.
5. Cost is less.	5. Cost is more.

Design of a Synchronous Mod-N counter using clocked D, T, or SR Flip-Flops.

2Bit binary synchronous counter



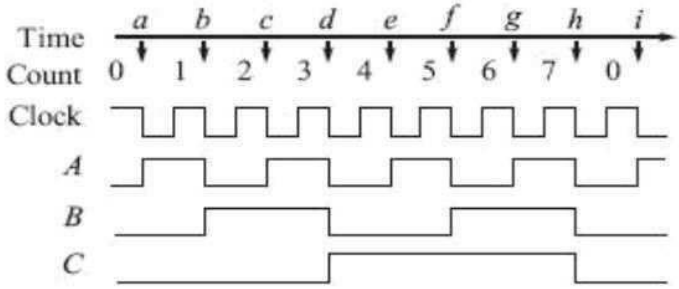
The flip-flop delay time and possibility of glitches are overcome by the use of a synchronous ornparallel counter. Every flip-flop is triggered in synchronism with the clock



(a)

C	B	A	Count
0	0	0	0
0	0	1	1
0	0	0	2
0	0	0	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7
0	0	0	0

(b)



(c)

Outcome

- Student will knoe the necessity of flip flops and its importance
- Design flip flops based on the characteristic equations.
- Will be able to design N Mod Synchronous counter

Future Readings

http://nptel.ac.in/courses/117105080/

https://www.youtube.com/watch?v=VnZLRrJYa2I

“Logic Design” by RD Sudhaker Samuel

“Digital Logic Applications and Design” by John M Yarbrough, 2011 edition