ATME COLLEGE OF ENGINEERING

13th KM Stone, Bannur Road, Mysore - 570 028

DEPARTMENT OF ELECTRICAL & ELECTRONICS ENGINEERING

NOTES

Course Title : Digital Logic Circuits

Course CODE: BEE306A

SEMESTER: III

Academic Year - 2023-24

INSTITUTIONAL VISION AND MISSION

VISION:

- Development of academically excellent, culturally vibrant, socially responsible and globally competent human resources.

MISSION:

- To keep pace with advancements in knowledge and make the students competitive and capable at the global level.
- To create an environment for the students to acquire the right physical, intellectual, emotional and moral foundations and shine as torchbearers of tomorrow's society.
- To strive to attain ever-higher benchmarks of educational excellence.

Department Vision and Mission

Vision:

To create Electrical & Electronics Engineers who excel to be technically competent and fulfill the cultural and social aspirations of the society.

Mission:

- To provide knowledge to students that builds a strong foundation in the basic principles of electrical engineering, problem solving abilities, analytical skills, soft skills and communication skills for their overall development.
- To offer outcome based technical education.
- To encourage faculty in training & development and to offer consultancy through research & industry interaction.

Program Educational Objectives (PEOs)

PEO1:

To produce competent and ethical Electrical and Electronics Engineers who will exhibit the necessary technical and managerial skills to perform their duties in society

PEO2:

To make students continuously acquire and enhance their technical and socio-economic skills

PEO3:

To allow students to embark on R&D activities leading to offering solutions and excel in various career paths.

PEO4:

To produce quality engineers who have the capability to work in teams and contribute to real time projects

Program Outcomes (POs)

Engineering Graduates will be able to:

PO1: Engineering Knowledge: Apply the knowledge of mathematics, science, engineering fundamentals and an engineering specialization to the solution of complex engineering problems.

PO2: Problem Analysis: Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.

PO3: Design / Development of solutions: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.

PO4: Conduct investigations of complex problems: Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.

PO5: Modern tool usage: Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.

PO6: The engineer and society: Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.

PO7: Environment and sustainability: Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.

PO8: Ethics: Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.

PO9: Individual and team work: Function effectively as an individual and as a member or leader in diverse teams, and in multidisciplinary settings.

PO10: Communication: Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.

PO11: Project management and finance: Demonstrate knowledge and understanding of the engineering management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.

PO12: Life-long learning: Recognize the need for and have the preparation and ability to engage in independent and lifelong learning in the broadest context of technological change.

Program Specific Outcomes (PSOs)

The students will develop an ability to produce the following engineering traits:

PSO1:Apply the concepts of Electrical & Electronics Engineering to evaluate the performance of power systems and also to control industrial drives using power electronics

PSO2: Demonstrate the concepts of process control for Industrial Automation, design models for environmental and social concerns and also exhibit continuous self- learning

Digital Logic Circuit

			Academic Year: 2024-2025				
Department: Electrical and Electronics Engineering							
Course Code	Course Title	Core/Elective	Prerequisite	Contact Hours			Total Hrs/ Sessions
				L	T	P	
BEE306A	**Digital Logic Circuit**	**Elective**	**Basic Electronics**	**3**	**-**	**2**	**40 theory**

Topics Covered as per Syllabus

Module-1

Definition of combinational logic, canonical forms, Generation of switching equations from truth tables, Karnaugh maps-3,4,5 variables, Incompletely specified functions (Don‘t care terms) Simplifying Max term equations, Quine-McCluskey minimization technique, Quine-McCluskey using don‘t care terms, Reduced prime implicants Tables.

Module-2

General approach to combinational logic design, Decoders, BCD decoders, Encoders, digital multiplexers, Using multiplexers as Boolean function generators, Adders and subtractors, Cascading full adders, Look ahead carry, Binary comparators

Module-3

Basic Bistable elements, Latches, Timing considerations, The master-slave flip-flops (pulsetriggered flip-flops): SR flip-flops, JK flip-flops, Edge triggered flip- flops, Characteristic equations

Module-4

Registers, binary ripple counters, synchronous binary counters, Counters based on shift registers, Design of a synchronous counter, Design of a synchronous mod-n counter using clocked T, JK, D and SR flip-flops.

Module-5

Mealy and Moore models, State machine notation, Synchronous Sequential circuit analysis, Construction of state diagrams, counter design.

Memories: Read only and Read/Write Memories, Programmable ROM, EPROM, Flash memor**y.**

List of Text Books

“Digital Logic Applications and Design” by John M Yarbrough, 2011 edition.
“HDL Programming (VHDL and Verilog)” by Nazeih M. Botros, 1 st Edition
“Digital Principles and Design “, Donald D Givone, Tata McGraw Hill Edition,2002.

List of Reference Books

“Logic Design” by RD Sudhaker Samuel

List of URLs, Text Books, Notes, Multimedia Content, etc: https://www.youtube.com/watch?v=VnZLRrJYa2I

MODULE 5

Fundamentals of Sequential Design and Design of Advanced Sequential Machines

Structure

- Objevtive
- Introduction
- Mealy and Moore models
- State machine notation
- synchronous sequential circuit analysis and design.
- Construction of state Diagrams
- Outcome
- Future Readings

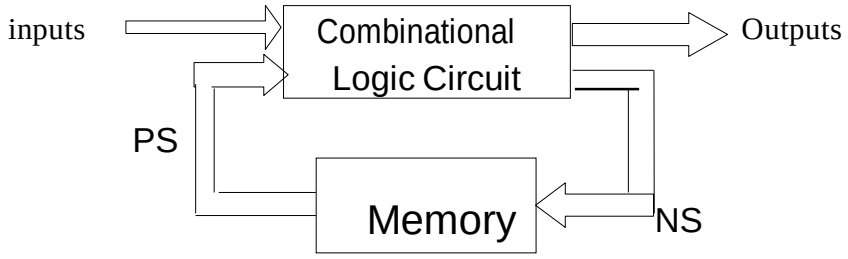
Objevtive

- To know about different models of a system and differentiate between them
- Designing of sequential circuit
- Designing of sequential circuit based on problem statement

Introduction

Definition :

In sequential networks, the outputs are function of present state and present external inputs. Present state simply called as states or past history of circuit. The existing inputs and present state for sequential circuit determines next state of networks.



Model of Sequential Network

Types of Sequential Network :

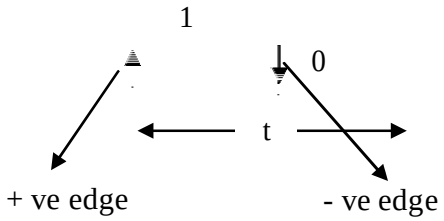
1. **Asynchronous Sequential Network :** The changes in circuit depends on changes in inputs depending on present state. But the change in memory state is not at given instant of time but depending on input.
2. **Synchronous Sequential Network :** Output depends on present state and present inputs at a given instant of time. So timing sequence is required. So memory is allowed to store the changes at given instant of time.

Structure and Operation of Clocked Synchronous Sequential Circuit :

In synchronous sequential circuit, the network behavior is defined at specific instant of time associated with special timing. There is master clock which is common to all FFs that is used in memory element. Such circuits are called as clocked synchronous

sequential circuit.

Clock : Clock is periodic waveform with one positive edge and one negative edge during each period.



This clock is used for network synchronization

Basic Operation of Clocked Synchronous Sequential Circuit

Q indicates all present state of FF.

Q+ indicates next state of FF in

network. X indicates all external

inputs.

Q+ = f(x,Q) This is next state of network.

Z indicates output signal of sequential networks.

Z = g(X,Q)

Mealy and Moore models

The structure shown in given figure is called as Mealy Model or Mealy Machine.

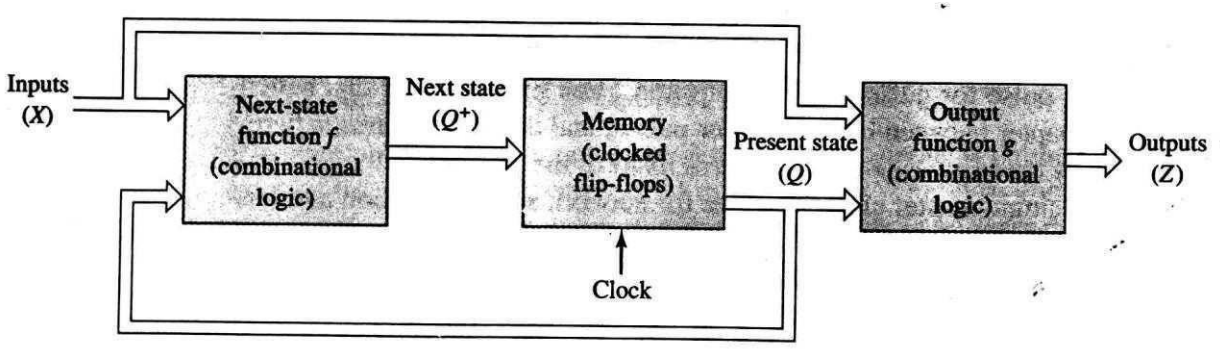


Figure 7.3 Mealy model of a clocked synchronous sequential network.

There are two types of finite state machines that generate output −

- Mealy Machine
- Moore machine

Mealy Machine

A Mealy Machine is an FSM whose output depends on the present state as well as the present input.

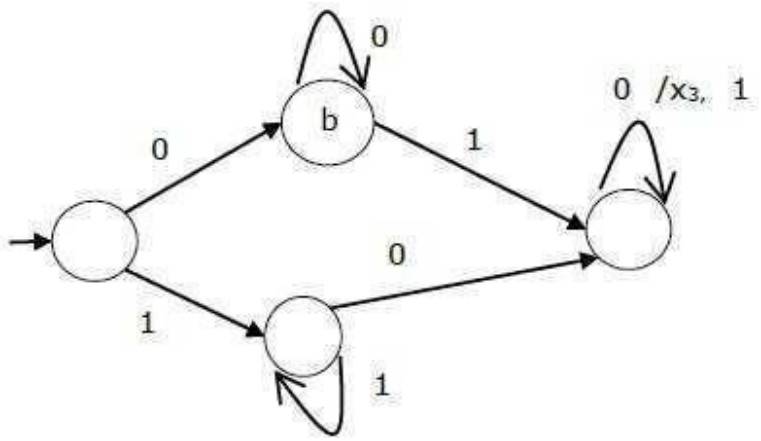
It can be described by a 6 tuple $(Q, \sum, O, \delta, X, q_0)$ where −

- **Q** is a finite set of states.
- $\sum$ is a finite set of symbols called the input alphabet.
- **O** is a finite set of symbols called the output alphabet.
- **δ** is the input transition function where $\delta: Q \times \sum \rightarrow Q$
- **X** is the output transition function where $X: Q \times \sum \rightarrow O$
- **q_0** is the initial state from where any input is processed ($q_0 \in Q$).

The state table of a Mealy Machine is shown below −

Present state	Next state			
	input = 0		input = 1	
	State	Output	State	Output
→ a	b	x_1	c	x_1
b	b	x_2	d	x_3
c	d	x_3	c	x_1
d	d	x_3	d	x_2

The state diagram of the above Mealy Machine is −



Moore Machine

Moore machine is an FSM whose outputs depend on only the present state.

A Moore machine can be described by a 6 tuple (Q, ∑, O, δ, X, q_0) where −

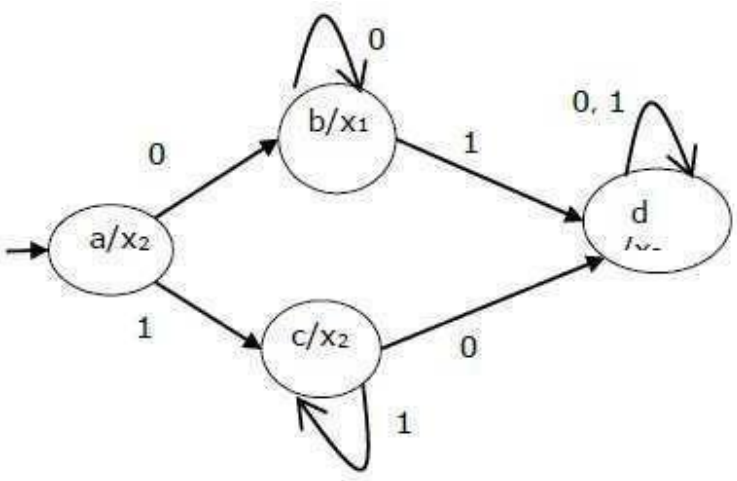
- **Q** is a finite set of states.
- ∑ is a finite set of symbols called the input alphabet.
- **O** is a finite set of symbols called the output alphabet.
- **δ** is the input transition function where δ: Q × ∑ → Q
- **X** is the output transition function where X: Q → O
- **q_0** is the initial state from where any input is processed (q_0 ∈ Q).

The state table of a Moore Machine is shown below −

Present state	Next State		Output
	Input = 0	Input = 1	
→ a	b	c	x_2
b	b	d	x_1

c	c	d	x_2
d	d	d	x_3

The state diagram of the above Moore Machine is −

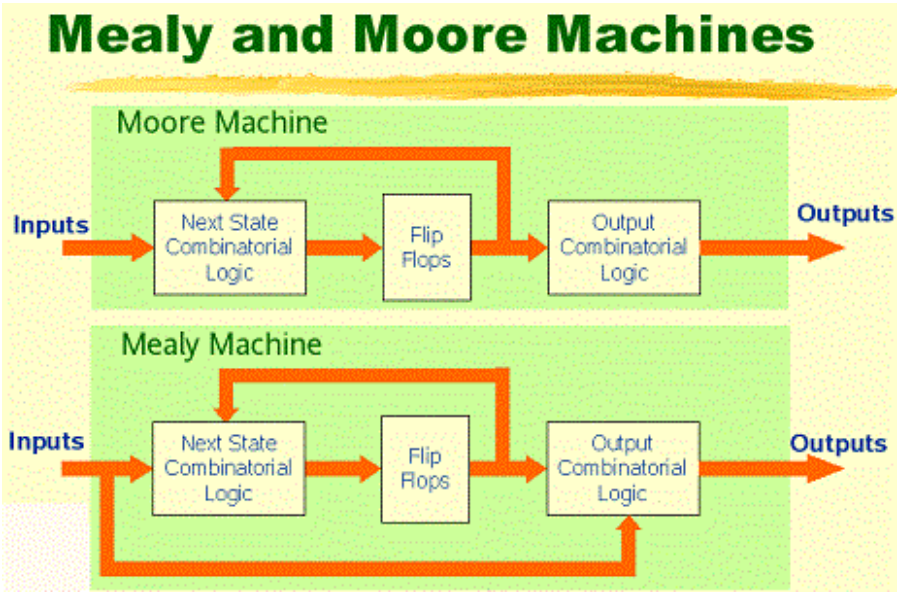


Mealy Machine vs. Moore Machine

The following table highlights the points that differentiate a Mealy Machine from a Moore Machine.

Mealy Machine	Moore Machine
Output depends both upon present state and present input.	Output depends only upon the present state.
Generally, it has fewer states than Moore Machine.	Generally, it has more states than Mealy Machine.
Output changes at the clock edges.	Input change can cause change in output change as soon as logic is done.

Mealy machines react faster to inputs	In Moore machines, more logic is needed to decode the outputs since it has more circuit delays.



Block Diagram of Mealy and Moore Machines

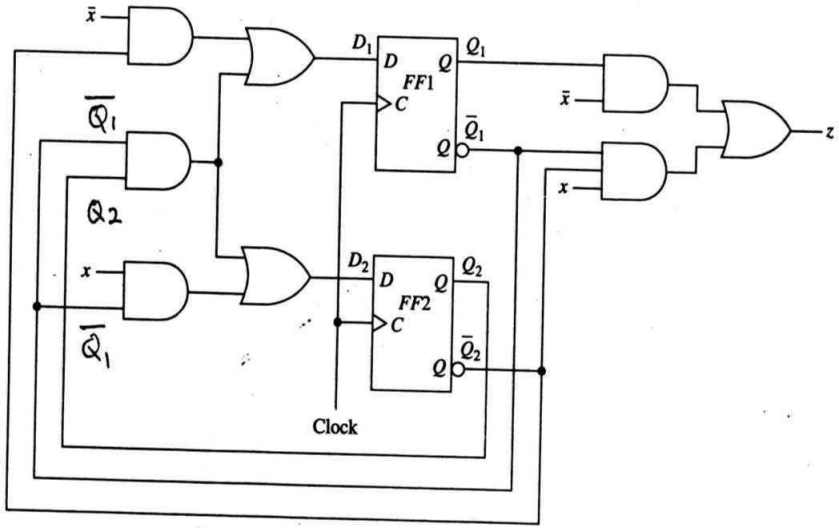
Difference between Mealy Model and Moore Model of Synchronous Sequential Circuit

Mealy Model : In Mealy Model the next state is function of external inputs and present state. The output is also function of external inputs and present state. The memory state changes with master clock.

$Q+ = f(X,Q)$ $Z = g(X,Q)$

Moore Model : In Moore Model the next state is function of external inputs and present state. But the output is function of present state. It is not dependent on external inputs. The no. of FFs required to implement circuit is more compared with Mealy Model,

$Q+ = f(X,Q)$ $Z = g(Q)$

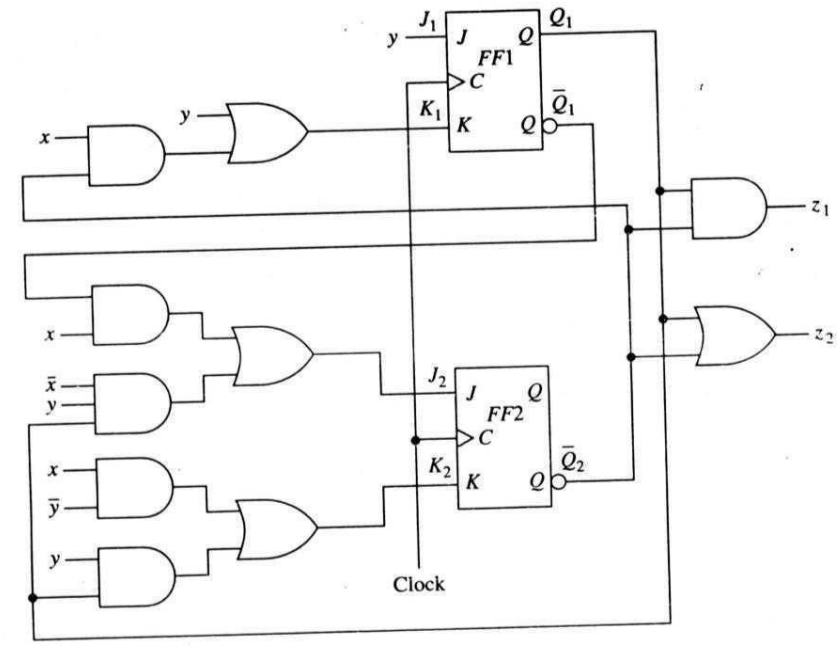


Logic Diagram for Mealy Network

$$D1 = \bar{x}\bar{Q}\bar{2} + \bar{Q}\bar{1}\bar{Q}\bar{2}$$

$$D2 = x\bar{Q}\bar{1} + \bar{Q}\bar{1}Q2$$

$$Z = \bar{x}Q1 + Q1\,Q2\,x$$



Logic Diagram for Moore Network

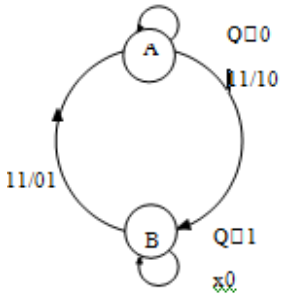
Transition Tables :

Instead of using algebraic equations for next state and outputs of sequential network, it is more convenient and useful to express the information in tabular form. The Transition Table or State Transition Table or State Table is the tabular representation of the transition and output equations. This table consist of Present State, Next State, external inputs and output variables. If there are n state variables then 2n rows are present in state table.

State machine notation

Input Variables : External input variables to sequential machine as inputs.
Output Variables : All variables that exit from the sequential machine are output variables.
State : State of sequential machine is defined by the content of memory, when memory is realized by using FFs.
Present State : The status of all state variable i.e. content of FF for given instant of time t is called as present state.
Next State : The state of memory at t+1 is called as Next state.
State Diagram : State diagram is graphical representation of state variables represented by circle. The connection between two states represented by lives with arrows and also indicates the excitation input and related outputs.
Output Variables : All variables that exit from the sequential machine are output variables.

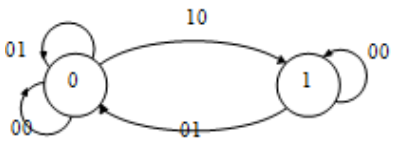
synchronous sequential circuit analysis and design.



State diagram of J-K FF

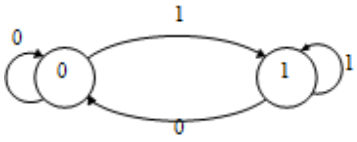
Application Table of JK FF

PS	NS	FF input	
Q	Q+	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0



State diagram of SR FF

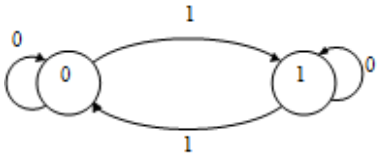
PS	NS	FF i/p	
Q	Q+	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0



State diagram of D FF

Application Table of D FF

PS	NS	FF i/p
Q	Q+	D i/p
0	0	0
0	1	1
1	0	0
1	1	1



State diagram of T FF

Application Table of FF

PS	NS	FF i/p
Q	Q+	T i/p
0	0	0
0	1	1
1	0	1
1	1	0

Transition table for Mealy Network

Present state (Q_1Q_2)	Next state $(Q_1^+Q_2^+)$		Output (z)	
	Input (x)		Input (x)	
	0	1	0	1
00	10	01	0	1
01	11	11	0	0
10	10	00	1	0
11	00	00	1	0

$$Q_1^+ = \bar{x}\bar{Q}_2 + \bar{Q}_1 Q_2 , \qquad Q_1^+ = D_1$$

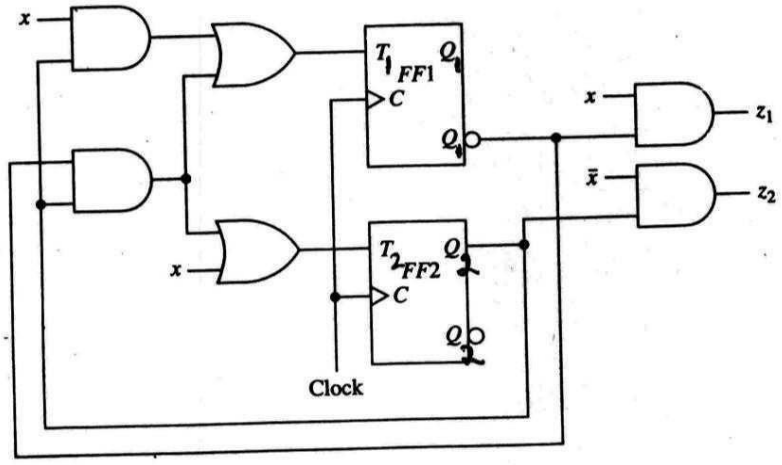
$$Q_2^+ = x\bar{Q}_1 + \bar{Q}_1 Q_2 , \qquad Q_2^+ = D_2$$

$$Z = \bar{x}Q_1 + \bar{Q}_1\bar{Q}_2 x$$

Transition table for Moore Network

PS(Q1Q2)	NS(Q1+,Q2+)				O/p (Z1Z2)
	I/p XY				
	00	01	10	11	
00	00	10	01	11	01
01	01	11	00	11	00
10	10	01	00	00	11
11	11	00	10	00	01

$$Z_1 = \overline{Q_2}Q_1\,,\ Z_2 = Q_1 + \overline{Q_2},\quad J_1 = y$$
$$K_1 = \overline{Q_2}x + y,\ J_2 = \overline{Q_1}\,\mathrm{x} + \overline{\mathrm{x}}\mathrm{y}Q_1\,,\ K_2 = x\overline{y} + y\overline{Q_1},$$



Synchronous Sequential Circuit

$$T_1 = xQ_2 + \overline{Q_1}Q_2,\quad Q_1^{+} = T_1 \oplus \mathrm{Q}_1$$
$$T_2 = x + \overline{Q_1}Q_2\,,\qquad Q_2^{+} = T_2 \oplus \mathrm{Q}_2$$
$$Z_1 = x\overline{Q_1},\qquad\qquad Z_2 = \overline{\mathrm{x}}Q_2$$

Construction of state Diagrams

State Tables :

State table consist of PS, NS and output section. The PS and NS of state tables are obtained by replacing the binary code for each in the transition table by newly defined symbol. The output section is identical to output section of transition table.

Symbols for state can be S1, S2, S3,……Sn or A, B, C, D, E….

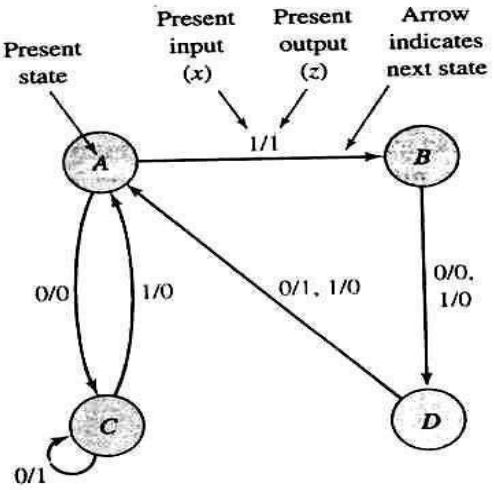
State table for Mealy Machine

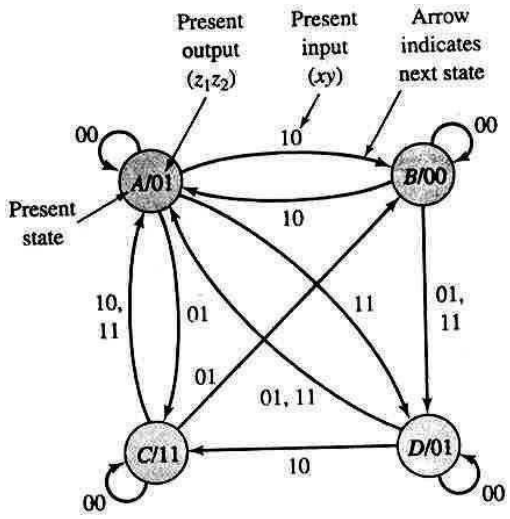
PS	NS		O/p Z	
00 – A	C	B	0	1
01 – B	D	D	0	0
10 – C	C	A	1	0
11 – D	A	A	1	0

State Diagram :

It is graphical representation of state tables. Each state of network is represented by labeled node.

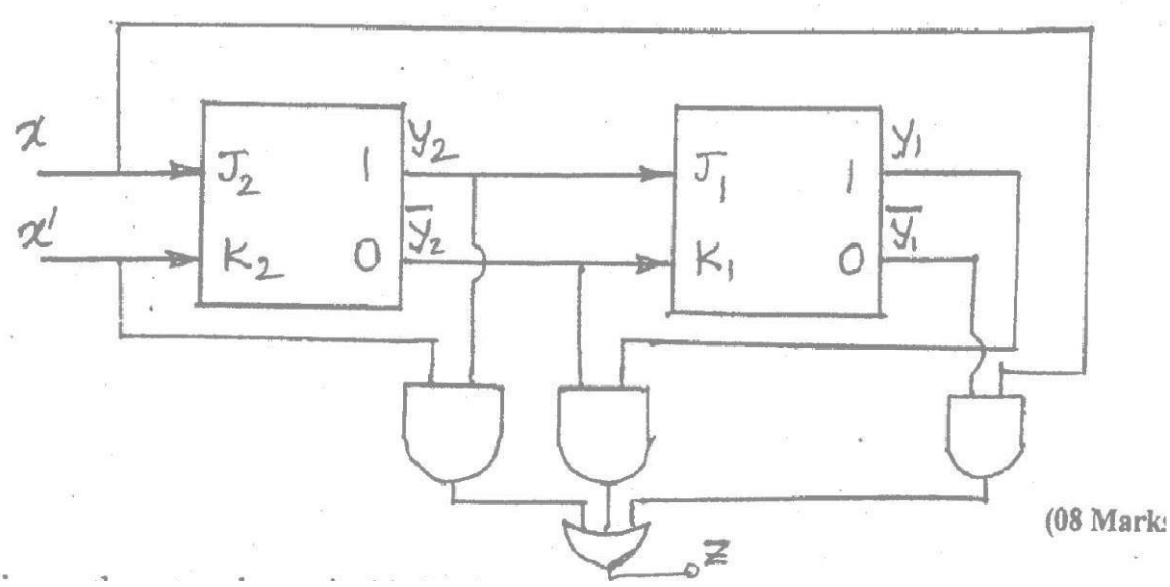
Directed branches connect the nodes to indicate transition between states. The directed branches are labeled according to the values of external input variable that permit transition. The output of sequential network is also entered in state diagram. In case of Moore Network state diagram, thE values of input for output is not written.





State diagram for Mealy Network

P1:



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Analysis of Synchronous Circuit

The given circuit in above figure is Mealy Network and the output is function of input variable and PS of FF. The analysis of above circuit is as follows.

The Excitation and Output Function

$$Z = \bar{x}y_2 + y_1\overline{y_2} + x\overline{y_1}$$

$$J_2 = x, \quad K_2 = \bar{x}, \quad J_1 = y_2, \quad K_1 = \overline{y_2}$$

By substituting the FF inputs in characteristic equation, the next state of FF is obtained in terms of PS of FF and external input.
The characteristic equation of JK FF is

$$Q^+ = J\overline{Q} + \overline{K}Q$$

$$Q_1^+ = J_1\overline{Q_1} + \overline{K_1}Q_1 = Q_2$$
$$Q_2^+ = J_2\overline{Q_2} + \overline{K_2}Q_2 = x$$

The Excitation Table

PS Q2 Q1 (y2 y1)	Excitation input J2 K2 / J1 K1 x=0, 1	x=0, 1	Output Z x=0, x=1
0 0	0 1	0 1	1 1
0 1	0 1	0 1	0 0
1 0	0 1	1 0	1 1
1 1	0 1	1 0	2 0

$J_1 = y_2 = Q_2, \quad K_1 = \overline{y_2} = \overline{Q_2}$
$J_2 = x, \quad K_2 = \overline{x}, \quad Z = \overline{x}y_2 + \overline{y_2}\,\overline{y_1} + x\overline{y_1}$
When $x = 0, \; z = y_2 + \overline{y_1}$ *and When* $x = 1, \quad z = \overline{y_1}$

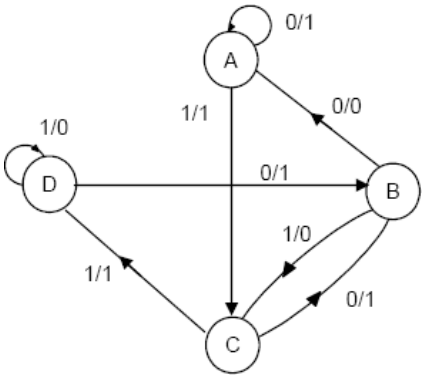
State Table

PS			NS						O/p Z	
			x = 0			x = 1				
Q2 (y2)	Q1 (y1)	state	Q2+	Q1+	state	Q2+	Q1+	state	X=0	X=1
0	0	A	0	0	A	1	0	C	1	1
0	1	B	0	0	A	1	0	C	0	0
1	0	C	0	1	B	1	1	D	1	1
1	1	D	0	1	B	1	1	D	1	0

Q1+ = Q2 = y2
Q2+ = x

$$if \;\; x = 0, \;\; z = y_2 + \overline{y_1}$$
$$if \;\; x = 1, \quad z = \overline{y_1}$$

State diagram



ABCD Represnts present state

Outcome

- **Will know difference between Milley and Moore model type of sequential circuits**
- **To write state diagram for sequential circuit or vice versa.**

4.9Future Readings

http://nptel.ac.in/courses/117105080/

https://www.youtube.com/watch?v=VnZLRrJYa2I

"Logic Design" by RD Sudhaker Samuel

"Digital Logic Applications and Design" by John M Yarbrough, 2011 edition