DEPARTMENT OF ELECTRICAL & ELECTRONICS ENGINEERING

Lesson Plan &Work-done Diary for AY: 2024-25, ODD Semester

	Course with Code: Digital Logic Circuits / BEE306A				Faculty: Mrs. Swathi C A		Semester & Section: III	
Class No.	**Date planned (DD/MM)**	**Topics to be covered**	**TLP Planned**	**Class No.**	**Date of Conduction (DD/MM)**	**Topics Covered**	**TLP Executed**	**Remarks if any deviation**
	MODULE-1							
1		Introduction	ICT					
2		**Principles of Combinational Logic:** Definition of combinational logic	ICT					
3		Canonical forms	ICT					
4		Generation of switching equations from truth tables	ICT					
5		Boolean Theorems & rules	Chalk & Talk					
6		Simplification of Boolean expressions	Chalk & Talk					
7		Karnaugh map rules & regulations	Chalk & Talk					
8		Karnaugh maps-3,4,5 variables	Chalk & Talk					
9		Incompletely specified functions (Don‘t care terms)	Chalk & Talk					
10		Quine-McCluskey minimization technique	Chalk & Talk					
11		Quine-McCluskey using don‘t care terms	Chalk & Talk					
12		Reduced prime implicants Tables	Chalk & Talk					

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	MODULE-2							
13		**Analysis and Design of Combinational logic:** General approach to combinational logic design	Chalk & Talk					
14		Decoders and BCD decoders	Chalk & Talk					
15		Encoders	Chalk & Talk					
16		Digital multiplexers	Chalk & Talk					
17		Using multiplexers as Boolean function generators	Chalk & Talk					
18		Adders and subtractors	Chalk & Talk					
19		Cascading full adders	Chalk & Talk					
20		Look ahead carry, Binary comparators	Chalk & Talk					

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	MODULE-3						
21		**Flip-Flops:** Basic Bistable elements	Chalk & Talk				
22		Latches, Timing considerations	Chalk & Talk				
23		The master-slave flip-flops	Chalk & Talk				
24		SR flip-flops, JK flip-flops	Chalk & Talk				
25		Edge triggered flip- flops	Chalk & Talk				
26		Characteristic equations	Chalk & Talk				

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	MODULE 4						
27		**Flip-Flops Applications:** Registers	Chalk & Talk				
28		binary ripple counters, synchronous binary counters	Chalk & Talk				
29		Counters based on shift registers	Chalk & Talk				
30		Design of a synchronous counter	Chalk & Talk				
31		Design of a synchronous mod-n counter using clocked T Flip Flop	Chalk & Talk				
32		Design of a synchronous mod-n counter using clocked JK Flip Flop	Chalk & Talk				
33		Design of a synchronous mod-n counter using clocked D Flip Flop	Chalk & Talk				
34		Design of a synchronous mod-n counter using clocked SR Flip Flop	Chalk & Talk				

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	MODULE 5						
35		**Sequential Circuit Design:** Mealy and Moore models	Chalk & Talk				
36		State machine notation	Chalk & Talk				
37		Synchronous Sequential circuit analysis	Chalk & Talk				
38		Construction of state diagrams	Chalk & Talk				
39		counter design	Chalk & Talk				
40		Memories: Read only and Read/Write Memories, Programmable ROM, EPROM, Flash memory	Chalk & Talk				

	Activity	Planned	Actual	Remarks
1	Theory Classes	41		
2	Assignments/Quizzes/ Self study	08 (Descriptive - 03 SRS – 05)		
3	Tutorials/ Extra classes	-		
4	Internal Assessments	03		
5	ICT based Teaching (% of usage in Curriculum)	23%(9/40)		
Planning			**Execution**	
Faculty Signature:			**Faculty Signature:**	
HOD Signature:			**HOD Signature:**	